A high performance PIN diode design in 0.25µm SiGe HBT process

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Abstract

In this paper, the physical structure, application areas, and design details of PIN diodes highlighted from the literature are summarized. Moreover, the YITAL 0.25µ SiGe HBT process compatible PIN diode to be used in X-Band transmitter/receiver circuits and monolithic microwave integrated circuit applications is designed using TCAD design tools. Additionally, effects of PIN diode geometry to its performance are also addressed. The anode area of the designed PIN is 16 µm^2 with square geometry. In addition to above studies, it is suggested to use of guard ring, deep trench isolation, and also a boron implantation under the bottom of each deep trench isolation well due to their positive effects on diode isolation parameters. Some important SPICE parameters are also extracted from the designed PIN diode using the completed DC and AC simulations. The related simulation results and calculations are also given in the paper together with discussions and future works.

1. Introduction

PIN diode is a semiconductor device that runs as a variable resistor in RF frequencies and microwave applications. The value of this RF resistance can only be defined when the diode is forward biased. PIN diodes are widely used as switching devices for RF signals [1], [2]. They don't add any distortion to the signal while controlling the RF signal level in switching and attenuation type of applications [3]. One of the most important features of PIN diodes is that they show relatively low value of turn on resistance even under low bias conditions. Due to these properties, they can be used to switch high level RF currents. As an example, while a PN rectifier diode requires at least 1 A bias current to be able to convey 1 A of RF current across it, a PIN diode can do this job under 50 mA of DC bias current [4].

PIN diodes are used in high voltage rectifiers, RF switches attenuators and even in photo detectors. The usage of a single antenna in both transmitter and receiver, phase array radars, variable gain RF amplifiers (VGAs), and Single Pole Single Throw (SPST) or Single Pole Double Throw (SPDT) switching circuits can be shown as good examples of RF switching and attenuation applications of PIN diodes. In the literature, several PIN diode design examples can be found to be used in same purposes, such as [5], [6], [7], [8], [9], [10] and [11].

The rest of the paper is organized as follows: the physical structure, electrical models and principles of operation of PIN diodes are presented in section 2. Additionally, there is a brief comparison of PIN and PN junction diodes. In section 3, some design rules of PIN diodes, fabrication steps and electrical analysis of a specific PIN diode, which is designed in Semiconductor Research Laboratory of Turkey (YITAL), so called the YITAL PIN diode, are presented. TCAD simulation results are also shown in some figures and also some important SPICE parameters extracted are also given. Finally, in section 4, this paper concludes with the research summary and future works.

2. Physical structure and principles of PIN diode

PIN diodes consist of three different semiconductor layers respectively P (p region), I (intrinsic or low doped region) and N (n region) as shown in Figure 1 [1]. In PIN diodes, P and N regions are highly doped to reduce the parasitic resistances and to form ohmic contacts. But semiconductor structure of I region can vary in a large scale, depending on applications. This I region determines the PIN diode's unique properties [3]. PIN diodes can be biased in two different ways like PN junction diodes. When it is forward biased, the small signal model has a forward series resistance (Rs) and parasitic inductance (L) as shown in Figure 2 [3]. When the PIN diode is reverse biased, the small signal model has PIN diode capacitance (Ct), parallel (shunt) resistance (Rp) and parasitic inductance (L) as shown in Figure 3 [3].

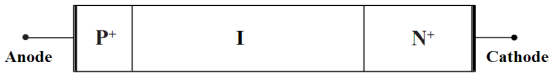

Fig. 1. PIN diode structure

Fig. 2. Small signal model of PIN diode under forward bias

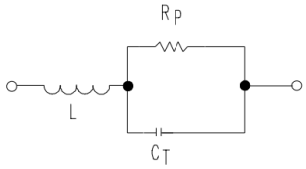

Fig. 3. Small signal model of PIN diode under reverse bias

In forward bias condition, electrons and holes leave the P and N regions and begin to fill inside the I region. Before the recombination of these carriers, they stay inside the I region for a finite time. So the resistance of the I region reduces [3]. The amount of the charges (Q) in the I region is dependent on forward bias current (If) and minority carrier lifetime (τ) as in the equation below:

$$Q = If.\tau \quad (1)$$

The series resistance of forward biased PIN diode is inversely proportional to Q and is calculated from the equation below:

$$R_S = \frac{W^2}{(\mu n + \mu p).Q} = \frac{W^2}{(\mu n + \mu p).If.\tau} \quad (2)$$

In this equation, W is the width of the PIN diode, μn and μp are the electron and hole mobilities. Rs seems to be independent to PIN diode area, but in real, it is dependent because τ is dependent to the area and the width of PIN diode. This is caused by edge recombination effects [3].

PIN diodes and PN junction diodes can be compared with some brief sentences:

1) Since PIN diode requires the usage of thinner wafer as compared to PN diode, its switching property is much better.
2) The reverse bias voltage applied to a PIN diode covers the complete I region.
3) PIN diodes have lower forward resistances under low forward bias currents.
4) PIN diodes can be used in switching circuits because they have very low resistances in microwave frequencies.
5) PIN diodes have higher breakdown voltages, so, they enable to control large RF signals.
6) PIN diodes have smaller junction capacitances.
7) They can be considered as unique components since they don't contain any majority carriers in I region [3].
8) They have the same principles from operation point of view. However, the only difference is related to the depletion region part. If there is no charge in the depletion region, they can behave as a good insulator.
9) PIN diodes work faster than PN diodes due to the electrical field covering entire I region. So PIN diodes become much more convenient devices for RF circuits.

3. Design details of PIN diode

The main purpose in PIN diode design is to reduce the insertion loss as much as possible while improving the isolation [12]. To achieve this purpose, the I region is required to be carefully designed for the best performance of the PIN diode. The I region must have high resistivity, low impurity and good crystal quality to achieve long lifetime. The I region's geometry is also an important design parameter. The minority carrier lifetime increases as the PIN diode's perimeter to area ratio (P/A) reduces [4]. Because, on the surfaces, surface recombination processes become dominant to bulk recombination processes [6], [13]. Therefore it is extremely important for geometrical optimization of PIN diode design to keep P/A ratio at minimum levels as long as the fabrication process allows. That means increased life time. When the minority carrier life time becomes longer, more minority carriers are stored in the I region. As a result, RF power control becomes possible [6].

P/A ratio becomes minimum when the anode geometry is circular. But some difficulties related to etching processes limit the fabrication of the devices with circular geometries. So, in the literature, PIN diodes are firstly appeared in square geometry in most of the literature. Secondly, octagonal anode structures can be encountered in the literature.

The PIN diode in this study has some constraints since it is fabricated by using steps in 0.25μ SiGe Heterojunction Bipolar Transistor (HBT) processes. Most of the fabrication steps are same for HBT and PIN diode. Base layer, collector layer and the buried layer of the HBT are P^+ anode, I and N^+ cathode layers respectively. This device structure is vertical which has some advantages when compared to lateral PIN diode configurations [8].

For the YITAL PIN diode, as a beginning, square anode geometry is preferred because of ease of TCAD simulations. P+ and N+ regions are designed as highly doped to get good ohmic contacts and to reduce Rs when the PIN diode is forward biased. The I region is lightly doped region to improve PIN diode isolation. The doping profile of the YITAL PIN diode is shown in Figure 4 as a result of Tsupreme4 process simulation program. From the surface through the substrate, the green line shows 10^{19} cm^{-3} of boron doped anode, the yellow line shows $2x10^{15}$ cm^{-3} of phosphorous doped intrinsic region and the purple line shows approximately 10^{20} cm^{-3} of arsenic doped cathode. The other green line on (0, +) of x axis shows the boron doped substrate of the processed wafer.

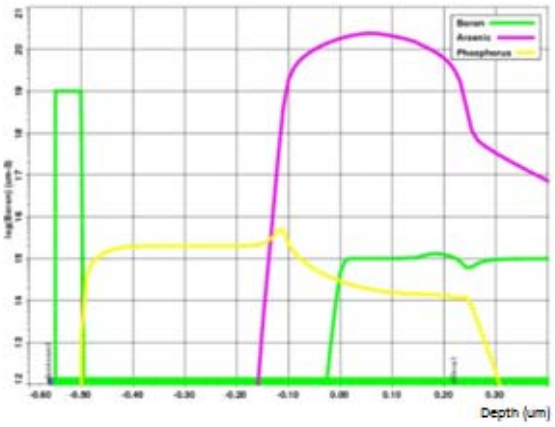

Fig. 4. Doping profile of the YITAL PIN diode

3.1. Fabrication steps

The major process steps of the YITAL PIN diode in the 0.25μ SiGe HBT process are listed in order as follows:

1. The buried layer is formed with a heavy ion implantation (170 keV energy and $5x10^{15}$ cm^{-2} dose) and a drive in process on 10^{15} cm^{-3} boron doped silicon substrate. This layer is the N+ (cathode) layer of the PIN diode.
2. 10^{15} cm^{-3} phosphorous doped 0.5 μ width epitaxial layer is grown on the buried layer. This process is implemented with RPCVD (Reduced Pressure Chemical Vapor Deposition) technique, by which high quality of silicon crystal with minimum defects can be obtained.

3. Deep Trench Isolation (DTI) step follows the epitaxial growth. Thanks to Deep Reactive Ion Etch (DRIE) technology to be able to do that. This layer is for electrical isolation of the PIN diode but requires the formation of 7μ depth of trenches with nearly 85° side wall angles.

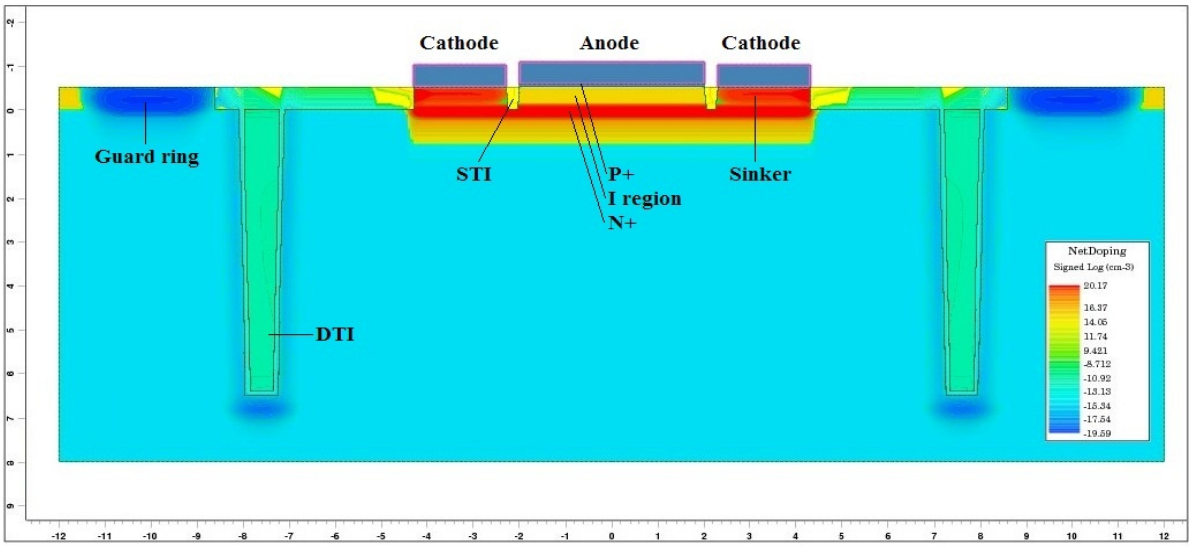

Fig. 5. Net doping in the cross section view of the YITAL PIN diode

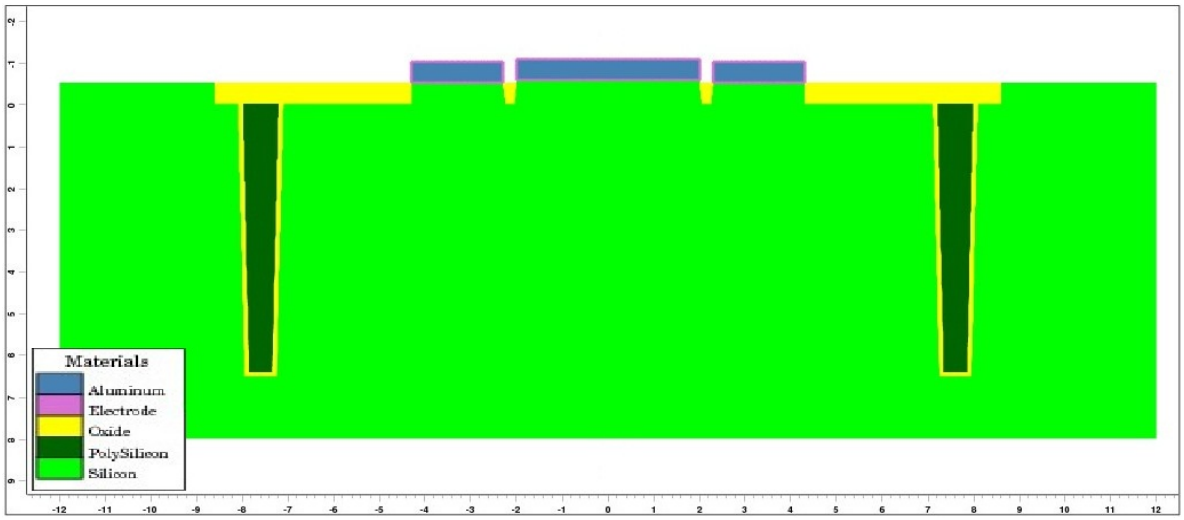

Fig. 6. Cross section view of the YITAL PIN diode's materials

4. To improve the isolation, concentration of 10^{17} cm^{-3} boron is implanted to form a p type region in the bottom of the DTI trenches. This p type region behaves as a pair of diodes which anodes are conducted to each other and block the leakage currents.
5. DTI trenches are filled with a thin thermal silicon dioxide at first and then filled with polysilicon.
6. Shallow Trench Isolation (STI) is processed with DRIE to decrease the capacitances between the anode and the cathode. STI trench has 0.5 μ depth.
7. STI trenches are filled with silicon dioxide.
8. A sinker implantation (150 keV energy and $5x10^{15}$ cm^{-2} dose phosphorous) is implemented to connect the contacts to the buried layer with low resistivity as much as possible.
9. Again, a p type region is made around the DTI trenches; this p type region is called as guard ring. The guard ring blocks the leak currents on surfaces and helps to get better isolation values.
10. A SiGe layer with 10^{19} cm^{-3} boron doping is growth with RPCVD technique. This layer is P+ (anode) region of the PIN diode.
11. Lastly, to obtain good ohmic contacts with low parasitic resistivity, aluminum metallization processes are applied.

It is important to note that only main fabrication steps of the YITAL PIN diode fabrication are listed above. Whereas, in 0.25μ SiGe HBT processes, more than 100 fabrication steps are required during real fabrication. It is also interesting to note that the entire 0.25μ SiGe HBT process requires more than 300 fabrication steps.

The fabrication process of the YITAL PIN diode is simulated using Taurus TSUPREM4 tool. The net doping profile and materials used in cross section view are shown in Figure 5 and Figure 6, respectively.

3.2. Electrical analyses

The electrical behavior of PIN diode is simulated by Taurus TDEVICE and Sentaurus SDEVICE programs. The I-V characteristic of the PIN diode is given in Figure 7. The built-in potential is approximately 0.9 V. Breakdown voltage is determined by Avalanche Breakdown Analysis (ABA) method shown in Fig. 8, which is around 17 V. AC characteristics of the PIN diode is also simulated for up to 10 GHz to extract the capacitance and admittance curves as given in Figure 9 and Figure 10, respectively. As mentioned earlier, the anode area of the PIN diode is only 4x4μm^2; therefore the junction capacitance of the diode is calculated as 6 fF. Due to small anode area, 0.9 V of forward biased PIN diode's RF resistance is calculated as 390 Ω which is not low enough. This resistance value will be decreased to more reasonable values under higher forward bias voltages.

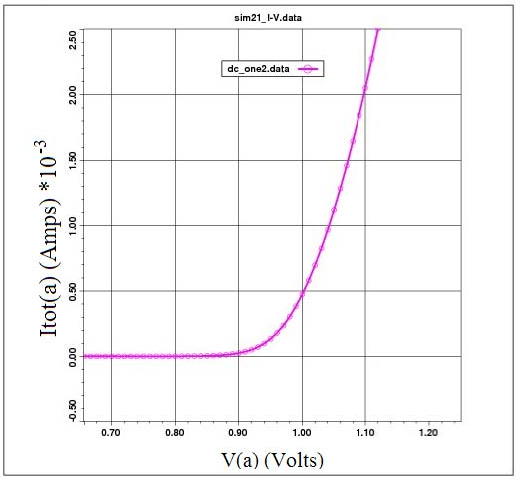

Fig. 7. I-V characteristics of the YITAL PIN diode after TCAD electrical simulations

Table 1. Parameter extraction results

Parameter name	Symbol	SPICE keyword	Value	Unit
Saturation current	Is	IS	$8x10^{-16}$	A
Emission coefficient	n	N	1.05	-
Parasitic resistance	Rs	RS	4	Ω
Breakdown voltage	BV	BV	17	V
Breakdown current	IBV	IBV	$8x10^{-13}$	A
Zero bias junction capacitance	Cd(0)	CJ0	$4x10^{-15}$	F
Built-in potential	Vbi	VJ	0.87	V

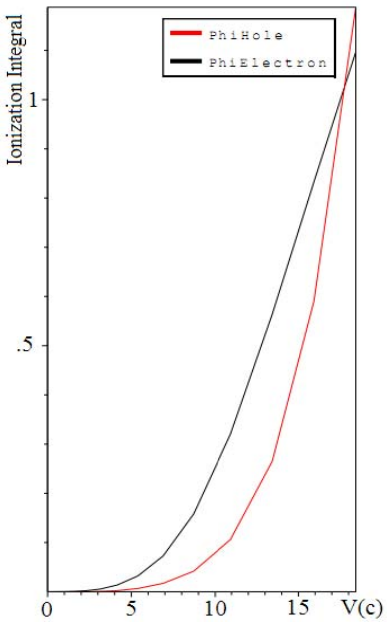

Fig. 8. Average breakdown analysis result of the YITAL PIN diode after TCAD electrical simulations

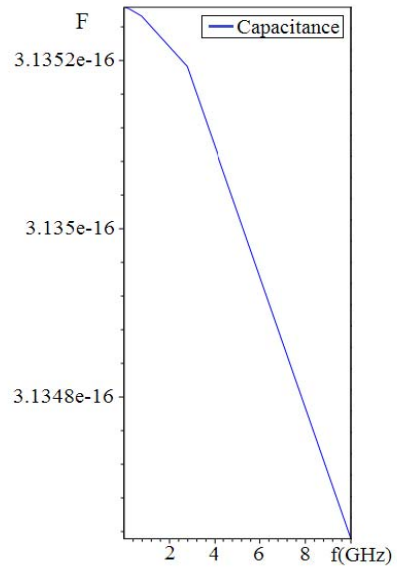

Fig. 9. Capacitance curve of the YITAL PIN diode after TCAD electrical simulations

Some important SPICE model parameters are also extracted from the simulation results and using related well-known solid-state device physics equations from the literature such as [1], [14]. Table 1 includes the SPICE model parameters of the designed PIN which are currently obtained successfully. A performance comparison table is given in Table 2. However, performance analyses on microwave application circuits have not been completed yet. Therefore insertion loss and isolation loss values have not been included in Table 2 yet.

Table 2. Comparison table

Reference work	Fabrication technology	Area µm2	Thickness µm	Insertion Loss dB	Isolation Loss dB	Frequency range GHz	Scientific contribution	Bias current and RON	Anode geometry
[6]	0.18µ Si-Ge BiCMOS	50	-------	0.69	27-9.7	2-18	Geometry effects, (P/A ratio), reverse biased parasitic diode	2mA	Octagonal (0.4dB improvement when compared to square geometry)
[7]	0.18µ Si-Ge BiCMOS	6.25	-------	1	42-19	2-16	Geometry effects, (P/A ratio)	2mA 2.001Ω	Octagonal geometry
[8]	0.13µ Si-Ge BiCMOS	9	<8	0.5-1	50-17	5-60	Guard ring and DTI usage, area optimization with respect to I region thickness	--------	Square geometry
[15]	0.18µ Jazz Si-Ge BiCMOS	50	1.8	1.09	39-13.67	0-18	Guard ring and DTI usage, square anode structure in Jazz process, P/A ratio	-------	Square geometry
This work	Si-Ge HBT	16	0,5	---	---	2-12	Guard ring and DTI usage, Geometry effects, P/A ratio, Si-Ge compatible PIN design	---	Square geometry

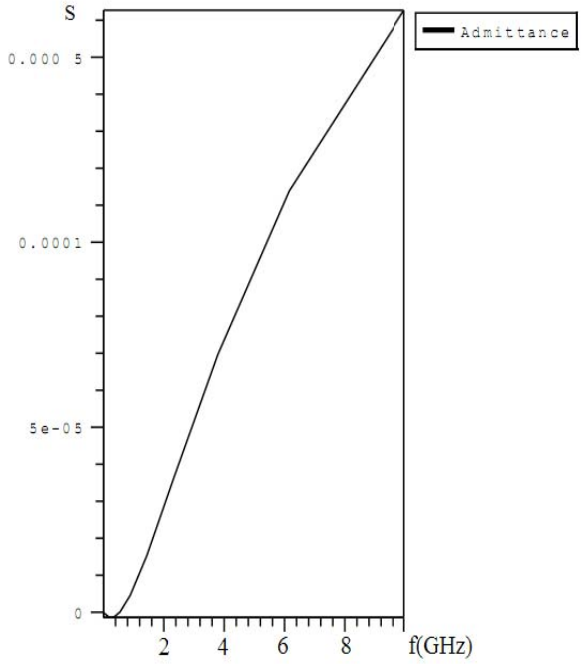

Fig. 10. Admittance curve of the YITAL PIN diode after TCAD electrical simulations

4. Conclusions

In conclusion, PIN diodes and their design principles are examined in detail. A detailed literature review has been done before going through the design process of the PIN diode. The process and electrical simulations were done and important SPICE model parameters belonging to the designed PIN diode were extracted.

As a future work, the real fabrication of the proposed PIN diode in the YITAL 0.25µ SiGe HBT process has been projected. Moreover, it has also been projected that the PIN diode will be used in some example microwave circuits such as SPST or SPDT switching circuits, or in design of a voltage gain amplifier (VGA) circuit which includes SiGe HBTs as well.

5. Acknowledgement

The authors would like to thank to Dr. Aziz Ulvi Caliskan and Sema Imrahorilyas from Semiconductor Research Laboratory of Turkey for hosting this research.

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