MOS only oscillator using adder and subtractor circuits

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Abstract

In this paper an NMOS based sinusoidal oscillator is presented. The circuit is constructed with voltage-mode (VM) NMOS-based analog adder and subtractor circuits which respectively perform V_1+V_2 and V_1-V_2 operations on the input voltages. The most important feature of the proposed circuits is their extremely simple structures containing only twelve NMOS transistors (six for the adder, six for the subtractor). Another significant advantage of the proposed circuits is that no external passive components are being used. The post-layout simulations of the proposed oscillator circuit have been executed using TSMC 0.25 µm process parameters with ±1.25 V power supply voltage.

1. Introduction

Oscillator circuits are widely used in communication circuits, instrumentation, measurement, etc. There are many oscillator circuits available in the literature using various active elements [1-11]. For example in [1] a sinusoidal oscillator using two current controlled current differencing transconductance amplifiers (CCCDTAs) as active elements and two grounded capacitors is presented. Similarly, other active elements such as second generation current conveyors (CCIIs), operational transconductance amplifiers (OTAs), differential voltage current conveyors (DVCCs) etc, have been used to construct sinusoidal oscillators [2-11]. All of the above mentioned oscillator circuits require passive elements such as resistors and capacitors which increase the power consumption and the silicon area in integrated circuit (IC) fabrication.

In this work, a new sinusoidal oscillator circuit using only one adder and one subtractor circuit [12] as active elements is presented. The most important feature of the circuit is that no passive element is required. However an external capacitor can be added to change the oscillation frequency. It is interesting to observe that the topology of the mutative 4-port, introduced in [12], augmented by two simple external feedback paths between its ports creates an oscillator in addition to many applications demonstrated in [12] and [13].

The paper is organized as follows. The proposed oscillator circuit and its analyses are given in Section 2. Simulation results of the proposed circuits are presented in Section 3. Finally, some concluding remarks are discussed in Section 4.

2. Proposed Oscillator Circuit

The symbol for the analog adder and subtractor circuits are shown in Fig. 1 and Fig. 2, respectively. The input terminals of the adder (V_{1a},V_{2a}) and subtractor (V_{1s},V_{2s}) circuits exhibit high impedance while the output terminals (V_a,V_s) exhibit low impedance. The ideal input-output relations of the adder and subtractor circuits are:

$$V_{oa} = V_{1a} + V_{2a} \quad (1)$$

$$V_{os} = V_{1s} - V_{2s} \quad (2)$$

together with I_{1a}=I_{2a}=I_{1s}=I_{2s}=0.

In the non-ideal case the expressions take the form:

$$V_{oa} = k_1 V_{1a} + k_2 V_{2a} \quad (3)$$

$$V_{os} = k_3 V_{1s} - k_4 V_{2s} \quad (4)$$

here k_i (i=1,2,3,4) is the non-ideality coefficient of the adder and subtractor circuits depending on the threshold voltages and aspect ratios of the transistors. A detailed analysis of the non-ideality coefficients is given in [12].

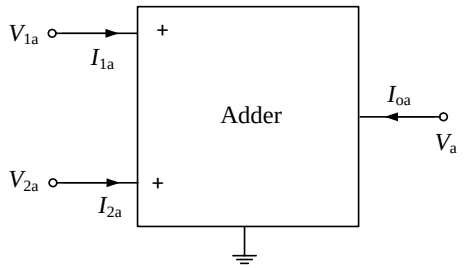

Fig. 1. Symbol of the analog adder circuit

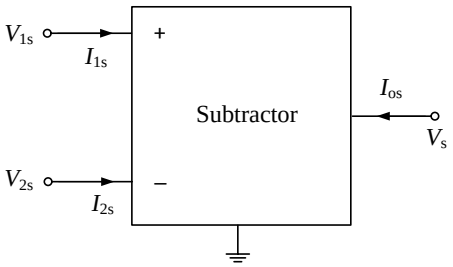

Fig. 2. Symbol of the analog subtractor circuit

A. The Proposed MOS only Oscillator

The proposed MOS only oscillator circuit constructed with an analog adder and a subtractor is given in Fig. 3. In order to find the theoretical operating frequency of the oscillator, simplified equivalent circuits of the subtractor and adder blocks including the feedback connections between the ports are shown respectively in Fig. 4 and Fig. 5.

In Fig.4 and Fig.5 R_{os} and R_{oa} represent the output resistances and, C_s and C_a are the equivalent parasitic capacitances at the output nodes of the subtractor and adder circuits. Replacing Fig. 4 and Fig. 5 in Fig. 3, the matrix state equation in (7) can be derived:

$$C_s \frac{dV_{os}}{dt} = \frac{V_{os}-V_{oa}-V_{os}}{R_{os}} = \frac{-V_{oa}}{R_{os}} \quad (5)$$

$$C_a \frac{dV_{oa}}{dt} = \frac{V_{os}+V_{oa}-V_{oa}}{R_{oa}} = \frac{V_{os}}{R_{oa}} \quad (6)$$

$$\frac{d}{dt}\begin{bmatrix} V_{oa} \\ V_{os} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C_a R_{oa}} \\ \frac{-1}{C_s R_{os}} & 0 \end{bmatrix} \begin{bmatrix} V_{oa} \\ V_{os} \end{bmatrix} \quad (7)$$

The eigenvalues $\lambda_{1,2}$ of the matrix in (7), are:

$$\lambda_{1,2} = \pm j\sqrt{C_s C_a R_{oa} R_{os}} \quad (8)$$

and the operating frequency of the oscillator is obtained as:

$$f = \frac{1}{2\pi\sqrt{C_s C_a R_{oa} R_{os}}} \quad (9)$$

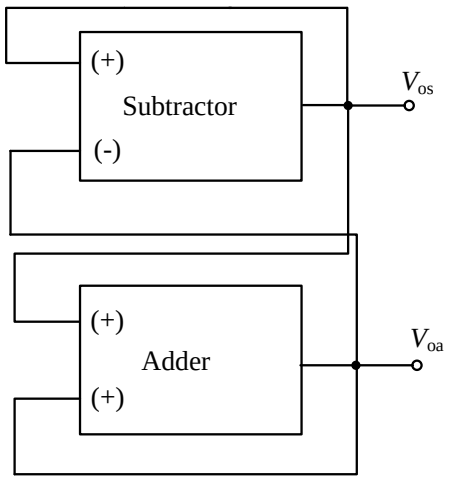

Fig. 3. Oscillator circuit

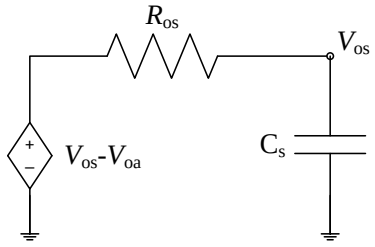

Fig. 4. Equivalent circuit of the subtractor block.

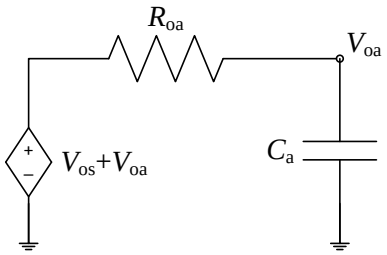

Fig. 5. Equivalent circuit of the adder block.

B. Tunable Oscillator Circuit

The proposed MOS only oscillator circuit can be frequency tuned by connecting an external capacitor to either the output node of the adder or the subtractor circuits. If a capacitor *C* is connected to the output port of the adder, from an equation similar to (7) derived in part *A*. the operating frequency of the tunable oscillator is obtained as:

$$f = \frac{1}{2\pi\sqrt{C_s(C_a+C)R_{oa}R_{os}}} \quad (10)$$

Similarly if the external capacitor *C* is connected to the output port of the subtractor the operating frequency of the tunable oscillator is again obtained as:

$$f = \frac{1}{2\pi\sqrt{(C_s+C)C_a R_{oa} R_{os}}}. \quad (11)$$

3. Simulation results of the oscillators

The schematic of the proposed oscillator circuit is shown in Fig. 6. In Fig. 6 V_{1s}, V_{2s} show the inputs of the subtractor and V_{1a} and V_{2a} show the inputs of the adder circuit. The dimensions of the MOS transistors in Fig. 6. are given in Table 1. The output resistances of the subtractor and adder blocks are found as:

$$R_{os} \cong \frac{1}{g_{m3s}} \quad (12)$$

and

$$R_{oa} \cong \frac{1}{g_{m5a}} \quad (13)$$

respectively. Here g_{m3s} and g_{m5a} are the transconductances of the transistors M_{3s} and M_{5a} respectively.

For theoretical results the output resistors in Fig. 6 are calculated as R_{os}=2.2 kΩ and R_{oa}=2 kΩ from expressions (12) and (13). The parasitic capacitors C_s=73 fF and C_a=71 fF are obtained from the post-layout simulation. Using these resistor and capacitor values the operating frequency is obtained as 1050 MHz from expression (9).

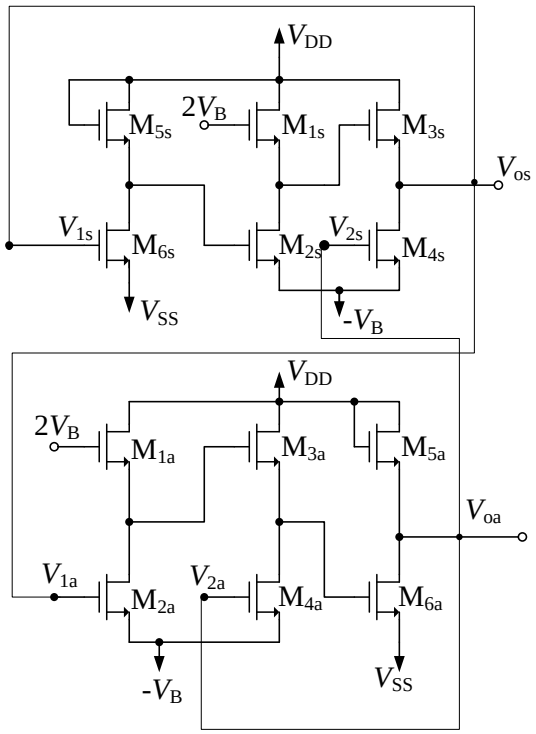

Fig. 6. The schematic of proposed oscillator circuit.

Table 1. Dimensions of MOS transistors for oscillator circuit

Transistors	W[µm]	L[µm]
M_{1a}, M_{2a}, M_{3a}, M_{4a}	1	0.5
M_{5a},M_{6a}	30	0.5
M_{1s}, M_{2s}, M_{5s},M_{6s}	1	0.5
M_{3s}, M_{4s}	30	0.5

The output waveform resulting from the post layout simulation of the circuit in Fig. 6 is given in Fig. 7. The simulation results of the oscillator circuit show oscillations at 1000 MHz; so, the theoretical and simulation results are in a very good agreement.

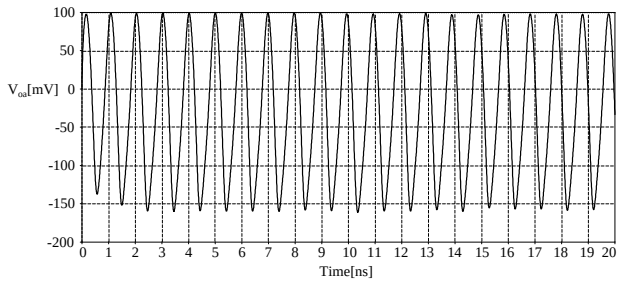

Fig. 7. Simulation result of the oscillator circuit

An external capacitor C=60 fF is connected to the output node of the adder circuit. The theoretical operating frequency of the tuned oscillator is obtained as 750MHz from the expression (10). The simulation result of the tuned oscillator show oscillations at 770MHz as shown in Fig. 8. Thus theoretical and simulation results are again in a good agreement.

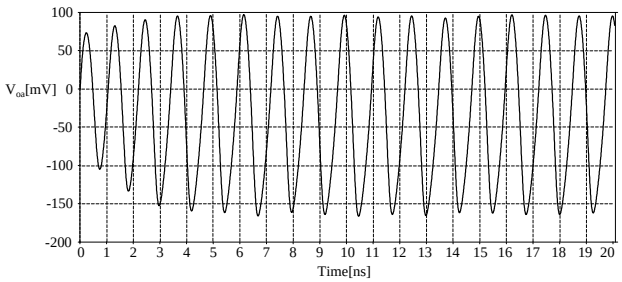

Fig. 8. Simulation result of the oscillator with external capacitor

4. Conclusions

In this paper using the recently introduced the generalized mutator 4-port built with an adder and a subtractor block [12], a new realization for an oscillator has been presented. With this oscillator application in addition to previously demonstrated ones such as mutator, inverter, gyrator, filter etc. circuits [12,13] the universality of the 4-port is being clearly established.

By connecting an external capacitor to the output of the adder or the subtractor circuit the oscillation frequency of the proposed oscillator can be tuned. Post-layout simulations of the proposed circuit are done with SPICE using TSMC 0.25 µm process technology parameters. Comparisons of SPICE simulated versus theoretical values are also presented which show a very good agreement.

5. References

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