

# Comparison of SPWM Technique and Selective Harmonic Elimination Using Genetic Algorithm

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## Abstract

A comparison of sinusoidal pulse width modulation (SPWM) and selective harmonic elimination (SHE) in a multicell DC/AC converter is presented. The genetic algorithm finds the existence optimal solution set of switching angles for each required harmonic profile. The dc links of each full bridge cell are supplied by individual high frequency DC-DC isolation stages which are connected in parallel considering the dc input of the total system. Furthermore, the cells which are operated in an interleaved SPWM mode or SHE mode are connected in series, so that the desired output of a multilevel inverter is synthesized by the low voltage level output of each cell. Conclusions about the effectiveness of the proposed converter are supported by analysis and simulation results.

## 1. Introduction

Multicell multilevel inverter systems have been well known for many years for medium-voltage/high-power applications in order to reduce the required blocking voltage of the power semiconductor devices. Multilevel inverter technology is based on the synthesis of the AC voltage from several voltage levels on the DC bus [1]-[3]. However, by considering modern low-voltage power switches and integrated gate driver stages, multicell topologies have become attractive [4].

For the applications mentioned, the converters have to be designed with very high efficiency and reliability. A common topology for this converter is adopting line-frequency transformers for isolation between dc input and ac output, as shown in Fig. 1(a). This results in high reliability because no semiconductor devices are connected directly to the load. The significant drawback of all topologies using a line-frequency transformer is given by the impact of the transformer on the total efficiency and on the weight and cost of the system. In order to avoid the bulky transformer and/or to increase power density and efficiency, an alternative topology with high-frequency transformer was proposed in [5]. In this topology a dc-dc system feeding the dc link of a full-bridge dc/ac converter is connected directly to the load, as shown in Fig. 1(b).

In this paper, the control of the ac output voltage is achieved by SPWM technique and SHE using genetic algorithm (GA). The SPWM technique which works with high switching frequency has many number of switching in one period of the fundamental output voltage. On other hand, the SHE technique, which works with low switching frequency, generally performs two number of switching during half cycle of the fundamental output voltage to generate a staircase waveform.

Available techniques for selective harmonic elimination include iterative methods, such as the Newton-Raphson method

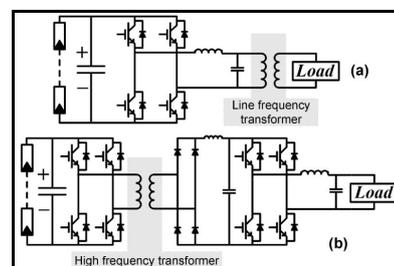
[6], and elimination by the theory of resultant [7]. Iterative methods mainly depend on the initial guess which makes a divergence problem especially for high numbers of inverter levels. Both techniques are complicated and time consuming [8].

The GA is a well-known search method to find near-optimal solutions and has been employed in optimal control problems [9]. In this paper, the GA is used to perform the study of the SHE technique. Then, the comparison between the SPWM and SHE is performed.

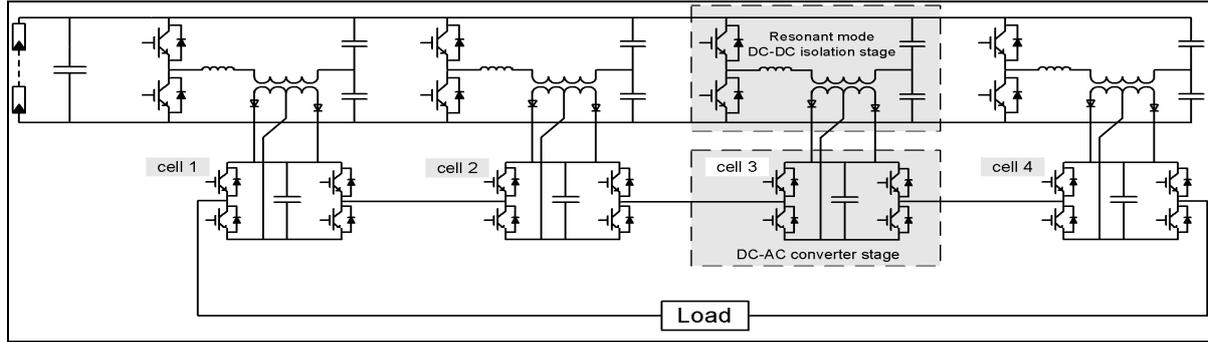
## 2. Series Resonant dc/dc Isolation Stage

The series-resonant topology has been chosen for the isolation stage due to the expected high efficiency of it. According to Fig. 2, each cell consists of a high-frequency series resonant isolation stage that feeds the dc link of a full-bridge inverter. Because of the series arrangement of the inverter stages, they can be realized in the same semiconductor technology as the isolation stages, i.e., application of low-voltage switches. The isolation stage is implemented using a capacitive coupled half-bridge converter operated in a constant-frequency series-resonant mode which results in low on-state losses and switching losses. In other words, switching frequencies higher than the natural frequency of the resonant network makes continuous conduction mode which has zero-current zero-voltage turn-on. While switching frequencies lower than the natural frequency of the resonant network, makes discontinuous conduction mode which has zero-current turn-on, zero-current turn-off. So, high efficiency based on the zero-current/zero-voltage turn-on/turn-off of the power switches is achieved. Consequently, the dc link voltage of each DC/AC stage varies directly according to the dc input voltage of the total system.

In the following, the characteristics of the stationary operation are expressed. Circuit diagram of the series-resonant converter is illustrated in Fig. 3(a). In this circuit, a center-tapped secondary winding is used for the designed converter



**Fig. 1.** Basic circuit topology of a solar-powered converter with: a) Full-bridge and line-frequency isolation transformer; b) DC/DC converter with high-frequency isolation transformer and full-bridge DC/AC converter.



**Fig. 2.** Basic circuit topology of the proposed DC/AC multicell converter based on high-frequency resonant-mode DC–DC isolation stages feeding interleaved SPWM-mode DC/AC cells connected in series on the AC output ( $N = 4$  cells).

which results in having only a single diode forward voltage drop as compared to bridge rectification. The corresponding equivalents circuit of Fig. 3(a) is shown in Figs. 3(b) and 3(c). Based on the analysis of circuit shown in Fig. 3(a), the natural frequency  $f_0$  and characteristic impedance  $Z_0$  of the series resonant network are:

$$f_0 = \frac{1}{2\pi\sqrt{2LC}} = \frac{1}{2\pi\sqrt{2 \times 5\mu\text{H} \times 1\mu\text{F}}} = 50 \text{ kHz} \quad (1)$$

$$Z_0 = \sqrt{\frac{L}{2C}} = \sqrt{\frac{5\mu\text{H}}{2 \times 1\mu\text{F}}} = 1.6 \Omega, \quad (2)$$

### 2.1. Switching Frequency Higher Than the Natural Frequency

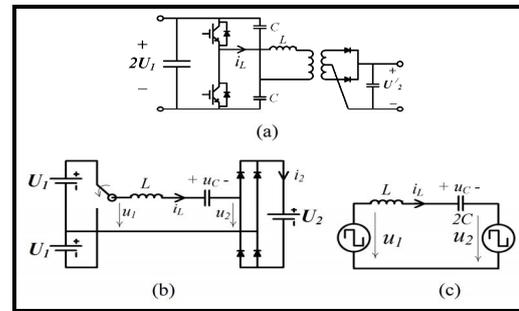
The system is characterized by four different states defined by the polarities of the input voltage  $U_1$  and reflected secondary voltage  $U_2$ . The polarity of  $U_1$  is defined by the control circuit and the polarity of  $U_2$  is given by the direction of the resonant current  $i_L$ . The four possible states are shown in Table 1, from *A* to *D*.

For state *A*, voltages  $U_1$  and  $U_2$  show equal direction and small difference voltage  $\Delta U = U_1 - U_2$  is applied to the LC series impedance. Because the system operates with a switching frequency  $f_S$  higher than natural frequency  $f_0$ , the input voltage changes its polarity at instant 1, as shown Fig. 4(a), due to the turn-off of the high-side switch, before  $i_L$  becomes zero. Consequently, the system transits to state *B* where the voltage  $-(U_1 + U_2)$  causes a high rate of current reduction. At instant 2, Fig. 4 (a), the current  $i_L$  becomes negative, the current in the rectifier diodes commutates and  $U_2$  again shows equal (i.e., negative) polarity, as shown in state *C* of Table-1. Then the low-side switch turns off at instant 3, Fig. 4 (a), before  $i_L$  becomes zero. Consequently, the system transits to state *D* where the  $U_1 + U_2$  causes a high rate of current increasing. So, a full cycle completes at instant 4, Fig. 4 (a). At instants 2, 4, there is zero current-zero voltage (ZC-ZV) turn on.

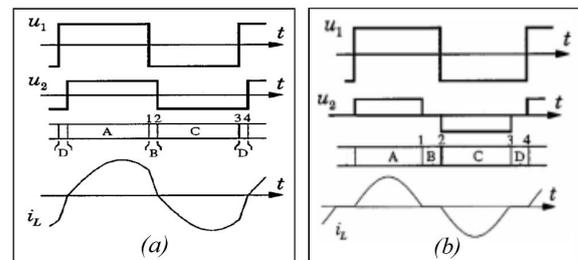
### 2.2. Switching Frequency Lower Than the Natural Frequency

In this condition, the system is characterized by four different

states based on the polarities of the input voltage  $U_1$  and reflected secondary voltage  $U_2$ , as listed in Table 2, from *A* to *D*. For state *A*, voltages  $U_1$  and  $U_2$  show equal direction and small difference voltage  $\Delta U = U_1 - U_2$  is applied to the LC series impedance. Because the system operates with a switching frequency  $f_S$  lower than the natural frequency  $f_0$  ( $T_S > T_0$ ), the current  $i_L$  becomes zero at instant 1, Fig. 4. (b), before the input voltage changes its polarity due to  $T_S > T_0$ . Consequently, the system transits to state *B*, which during interval 1 to 2, i.e.  $\Delta t = (T_S - T_0)/2$ , the current  $i_L$  is zero, as shown in Fig. 4(b). The circuit changes to state *C* at instant 2, and in this instant the low-side switch turns on and the current  $i_L$  becomes negative, so the small difference voltage  $\Delta U = -(U_1 - U_2)$  is applied to the LC series impedance. At instant 3, the current  $i_L$  becomes zero before the input voltage changes its polarity due to  $T_S > T_0$ . Because of using the

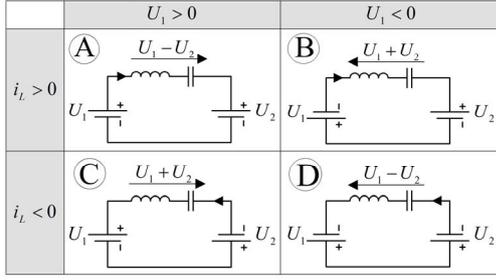


**Fig. 3.** Circuit diagram of: a) series-resonant converter; b), and c) corresponding equivalent circuits.

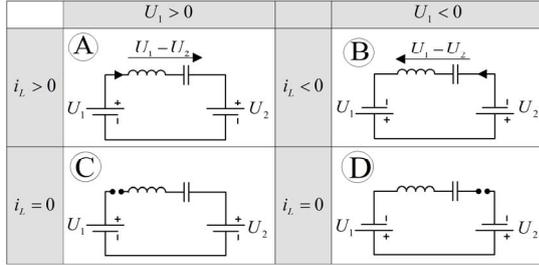


**Fig. 4.** Time behavior of the series-resonant converter: a)  $f_S > f_0$ ; b)  $f_S < f_0$ .

**Table 1.** Operating states of series resonant dc/dc isolation stage



**Table 2.** Operating states of series resonant dc/dc isolation stage



isolation transformer (high-frequency), the current of secondary winding is lagging to the current of primary winding ( $i_L$ ); so, it has small positive value when the current of primary winding ( $i_L$ ) becomes zero. As result, the direction of current  $i_L$  can not be changed and the high-side anti parallel diode can not be turned on at instant 1, immediately. After short period of time while the current of secondary winding becomes zero, the high-side anti parallel diode can not be turned on spontaneously. Consequently, the system transits to state *D* which during interval 3 to 4, i.e.  $\Delta t = (T_S - T_0)/2$ , the current  $i_L$  is zero, as shown in Fig. 4(b). So, a full cycle completes at instant 4. At instants 1, 3, there is ZC turn off and at instants 2, 4, there is ZC turn on.

Fig. 5 illustrates that by increasing the  $P_{out}$ , the ratio of the  $U_2/U_1$  ( $U_1 = 50V$ ) is decreased for  $f_s \gg f_0$ , but it is almost constant for  $f_s \leq f_0$ . So, it is realized that by increasing  $f_s$ , the mentioned DC-DC isolation stage can not perform in high output power and the dc link voltage decreases proportional to the load current, i.e., the converter shows a quasi-ohmic output impedance.

Figs. 6 and 7 show the efficiency and  $P_{loss}$  of 4-cell series resonant, Fig. 2, versus  $P_{out}$  and  $f_s$ . According to these figures the proposed DC-DC isolation stage has a good efficiency and by increasing  $f_s$ , efficiency decreases and the system can not perform in high output power.

### 3. Multicell dc/ac Converter

The control of DC/AC multicell converter is performed by SPWM technique, and SHE technique. The methods are described in sections 3.1 and 3.2, respectively.

#### 3.1. Interleaved SPWM Technique

The detailed analysis of the multicell class-D switch-mode amplifier is presented in [10]. The advantage of the multicell topology with the individual switching cells operating in an interleaved SPWM mode is that the output voltage ripple is

reduced by a factor of  $N$  ( $N$  is number of cells). By application of a second-order LC output filter, the output voltage ripple across the filtering capacitor is reduced by  $N^3$  according to [10]. For example, for  $N = 4$ , the ripple is reduced by a factor of 64 as compared to a single-cell topology, given in Fig. 1(b). This makes it possible to operate the system at a comparatively low SPWM switching frequency. Therefore, in the following simulation, the switching frequency is chosen  $f_s = 1.9kHz$ . Due to the 1:1 voltage transfer ratio of the DC-DC converter, the same type of power switches, as used for the isolation stage, can be adopted for power stages of the DC/AC converter.

Output voltage of multicell topology controlled by SPWM and load current, as well as, dc links voltages are illustrated in Figs. 8 and 9, respectively.

Fig. 10 shows the spectrum frequency of output voltage with THD of 13%. Fig. 11 displays THD of the output voltage versus variation of the output power. It worth mentioning that by increasing the switching frequency of series resonant network and  $P_{out}$ , the THD of output voltage increases, especially for  $f_s = 85kHz$ . Because by increasing the output power, dc links voltage ripples increase which causes in growing up the output voltage THD.

According to Fig. 12 which displays  $E_{out}(rms)$  versus output power variation, by increasing the output power, the proposed topology can not generate the fixed output voltage at switching frequencies higher than the natural frequency ( $f_0 = 50kHz$ ) of the resonant network because dc links voltages collapse severely by increasing the output power at those switching frequencies, according to Fig. 5.

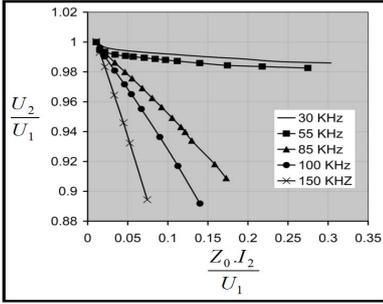
#### 3.2. Selective Harmonic Elimination Technique

In this subsection, control of the multilevel inverter is performed by the SHE technique. This technique depends on solving a series of trigonometric equations which are obtained from the Fourier expansion of the inverter output voltage. The solution is the switching angles that will put specific low order frequency components equal to zero while controls the fundamental frequency component.

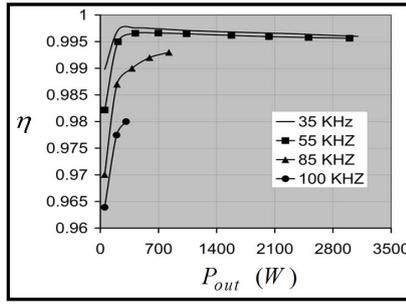
Fig. 13 shows a typical symmetric and stepped voltage waveform synthesized by a  $2S+1$  level inverter, where  $S$  is the number of switching angles and the number of DC sources. For equal dc sources ( $V_{dc}$ ), the Fourier series expansion of the output voltage waveform, shown in Fig. 13, is:

$$E_{out}(\omega) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{n\pi} \begin{bmatrix} \cos(n\theta_1) + \\ \cos(n\theta_2) + \\ \vdots \\ \cos(n\theta_S) \end{bmatrix} \times \sin(n\omega t) \quad (3)$$

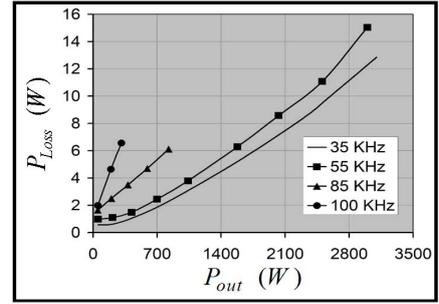
Ideally, with a given desired fundamental voltage  $V_1$ , it is possible to determine the switching angles  $\theta_1, \theta_2, \dots, \theta_S$ , so that  $E_{1out}(\omega) = V_1 \sin(\omega t)$ , and specific harmonics are equal to zero. It has been proved that to control the fundamental output voltage and eliminate  $S-1$  harmonics,  $S$  equations are needed. For example, a 9-level inverter can control the fundamental component and eliminate the amplitudes of three harmonics. The switching angles can be found by solving the following equations:



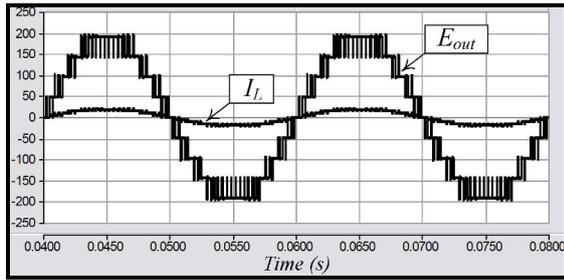
**Fig. 5.** Output characteristic of the series resonant converter for natural frequency  $f_0 = 50\text{kHz}$ .



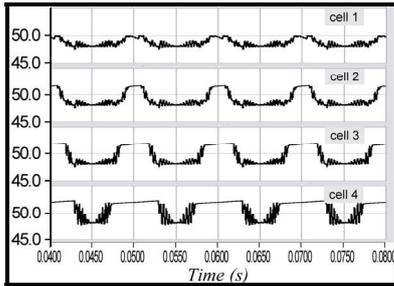
**Fig. 6.** Efficiency of the DC-DC isolation stages.



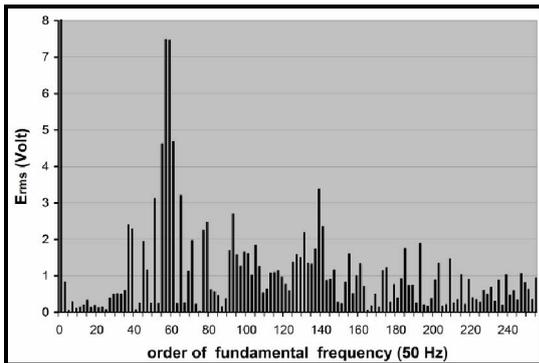
**Fig. 7.** Power losses of the DC-DC isolation stages.



**Fig. 8.** SPWM ac output voltage (Volt) and load current (Ampere).



**Fig. 9.** dc links voltages (Volt).



**Fig. 10.** Frequency spectrum of ac output voltage by using the SPWM technique ( $E_{1,rms} = 136\text{V}$ ).

$$\begin{cases} \cos(\theta_1) + \cos(\theta_2) + \dots + \cos(\theta_S) = m \\ \cos(n\theta_1) + \cos(n\theta_2) + \dots + \cos(n\theta_S) = 0, \quad n = 5, 7, 11 \end{cases} \quad (4)$$

where  $m = (\pi V_1)/(4V_{dc})$ .

One approach to solve the set of nonlinear transcendental (4) is using an iterative method such as the Newton-Raphson

method. In contrast to iterative methods, the transcendental equations, characterizing the harmonic content, can be converted into polynomial equations and solved using resultant theory [7]. On the other hand, the solution using resultant theory produces all possible solutions, but it is complicated and time consuming. Therefore, it is worth to consider more techniques and simple techniques such as GA. The GA is simple, powerful, derivative free, stochastic global search algorithms inspired by the laws of natural selection and genetics. Furthermore, GA can solve complex objective functions and reduce computational burden and search time [9].

In this paper, the GA is used to perform the study of the SHE technique. Based on experience and trial and error, the GA operator probabilities and population size are selected. In the following simulation, the population size and the probability of the crossover are 400 and 0.8, respectively, with a Gaussian mutation function. Also, the population type is a double vector.

The solutions of switching angles for 9-level output voltage versus modulation index ( $m$ ) are shown in Fig. 14, where 5th, 7th and 11th harmonics are eliminated. It worth mentioning the triple harmonics can be eliminated in the three-phase application.

Fig. 15 displays the output voltage of the prototype multicell converter and the load current by using SHE technique for  $m = 3.14$ . The spectrum frequency of output voltage is shown in Fig. 16. As shown in this figure 5th, 7th, 11th harmonics are eliminated. In this condition, THD of the output voltage equals 10%. Also by eliminating triple harmonics, THD will equal 7%.

#### 4. Comparison of the SPWM and SHE

The THD and efficiency of SPWM and SHE techniques are compared in this section (at both method, series resonant network switching frequency is  $f_s = 55\text{kHz}$ ). According to Fig. 10, THD of the output voltage, controlled by SPWM technique ( $f_s = 1.9\text{kHz}$ ), is almost 13% while THD of the output voltage controlled by SHE technique is almost 10%. As shown in Fig. 17 the efficiency of the SHE technique is better than SPWM ( $f_s = 1.9\text{kHz}$ ) technique in the multicell multilevel inverter. In addition, number of switching in SPWM technique is higher than SHE technique. Thus, SPWM technique needs switches with ability of high switching frequency and low on-time and off-time, results in high cost converter.

#### 5. Conclusion

A multicell multilevel inverter which is controlled by SPWM technique and SHE technique has been presented. High

frequency isolation stage based on series resonant network is purposed to decrease the size and increase the efficiency of converter. The SPWM and SHE techniques are implemented to the DC/AC multicell converter. The simulation results point out that the SHE technique is so better than SPWM technique in point of view efficiency, cost and controlling circuit. Also, using GA in SHE technique offers some bold features, such as producing a continuous range of switching angles and all existence sets of solutions, as well as, canceling the complicated and time consuming computation of trigonometric equations.

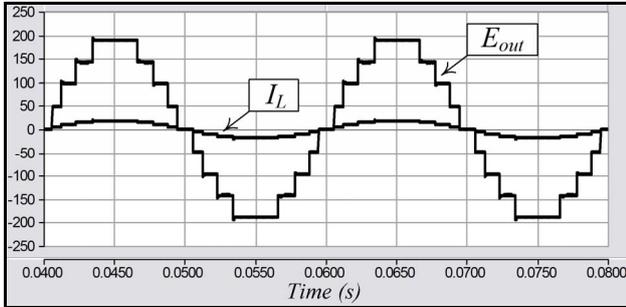


Fig. 15. SHE ac output voltage (Volt) and load current (Ampere).

### 6. References

[1] J. Rodriguez, J. Lai and FZ. Peng, “Multilevel converters: a survey of topologies, controls, and applications”, *IEEE Trans. Industrial Application*, vol. 49(4), pp. 724–738, Aug. 2002

[2] P. Lezana, J. Rodríguez and D. A. Oyarzún, “Cascaded multilevel inverter with regeneration capability and reduced number of switches”, *IEEE Trans. on Industrial Electronics*, vol. 55, no. 3, pp. 1059-1066, Mar. 2008.

[3] A. M. Lienhardt, G. Gateau and T. A. Meynard, “Zero-Steady-State-Error input-current controller for regenerative multilevel converters based on single-phase cells”, *IEEE Trans. on Industrial Electronics*, vol. 54, no. 2, pp. 733-740, Apr. 2007.

[4] S. H. Hosseini, A. Kh. Sadigh and A. Sharifi, “Estimation of flying capacitors voltages in multicell converters”, in *Proc. ECTI Conf.*, 2009, vol. 1, pp. 110–113.

[5] C. F. Nayar, S. M. Islam and H. Sharma, “Power electronics for renewable energy sources”, in *Power Electronics Handbook*, M. H. Rashid, Ed. New York: Academic, 2001, ch. 23.

[6] Patel HS and Hoft RG. “Generalized techniques of harmonic elimination and voltage control in thyristor inverters: part I – harmonic elimination”, *IEEE Trans Industrial Application*, vol. 3, pp. 310-317, 1973.

[7] Chiasson JN, Tolbert LM, McKenzie KJ and Du Z., “Control of a multilevel converter using resultant theory”, *IEEE Trans Control System Theory*, vol. 11(3), pp. 345-354, May. 2003.

[8] Kh. El-Naggar and T. H. Abdelhamid, “Selective harmonic elimination of new family of multilevel inverters using genetic algorithms”, *Elsevier Journal of Energy Conversion and Management*, vol. 49, issue 1, pp. 89-95, Jan. 2008.

[9] Ovaska SJ, Bose T and Vainio O., “Genetic algorithm-assisted design of adaptive predictive filters for 50/60 Hz power systems instrumentation”, *IEEE Trans. Instrument Measurement*, vol. 54(5), pp. 2041-2048, 2005.

[10] H. Ertl, J.W. Kolar and F. C. Zach, “Analysis of a multi-level multi-cell switch-mode power amplifier employing the flying-battery concept”, *IEEE Trans. Industrial Electronics*, vol. 49, pp. 816–823, Aug. 2002.

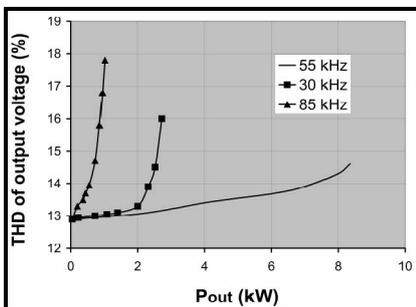


Fig. 11. THD of the output voltage versus the output power.

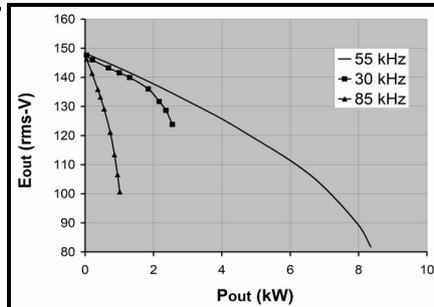


Fig. 12. Output voltage versus output power.

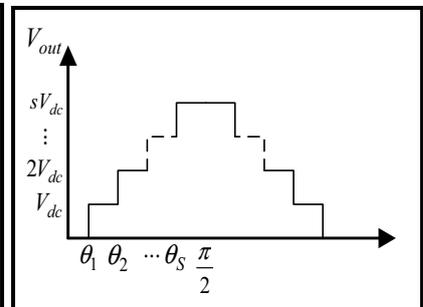


Fig. 13. Generalized stepped voltage of multilevel inverter.

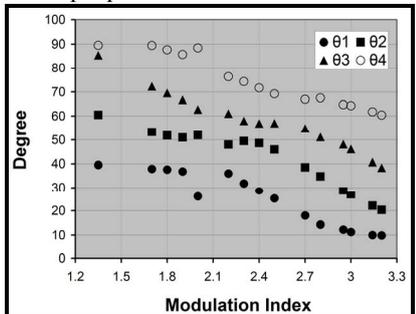


Fig. 14. Solutions of 4 angles versus  $m$  for 9-level inverter (5th, 7th and 11th harmonics eliminated).

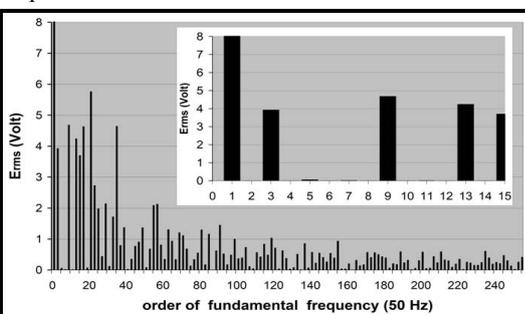


Fig. 16. Frequency spectrum of output voltage by using the SHE technique ( $E_1 = 141V - rms$ ).

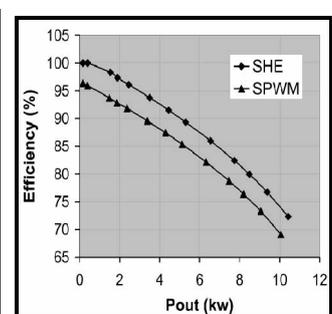


Fig. 17. Efficiency of the multicell inverter controlled by SPWM and SHE techniques.