Designing a New High Q Fully CMOS Tunable Floating Active Inductor Based on Modified Tunable Grounded Active Inductor

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Abstract

A new Tunable Floating Active Inductor (TFAI) based on modified Tunable Grounded Active Inductor (TGAI) is proposed. Multi regulated cascade stage is used in TGAI to boost gain of input impedance and inductor value thus the Q factor enhancement obtained. The arrangement of Multi-Regulated Cascade (MRC) stage is caused the input transistor which determines AI self-resonance frequency to be as small as possible and it is free of body effect which is crucial in sub-micron technology. Compared to traditional CMOS spiral inductors, the active inductor proposed in this paper can substantially improve its equivalent inductance and quality factor. This TFAI was designed using the AMS 0.18 um RF CMOS process, which demonstrates an adjustable quality factor of 10~567 with a 6~284 nH inductance. The Q factor and value of active inductor is adjusted with bias current and flexible capacitance (varactor), respectively. The self-resonance frequency for both grounded and floating AI is about 6.2 GHz. The proposed active inductor also shows wide dynamic range and higher quality factor compared to conventional floating active inductor circuits.

1. Introduction

A huge number of present day high-volume customer applications requires the accessibility of low-power, low-cost, remote Microsystems. According to these necessities, CMOS technology has turn into the best decision for wireless communication systems. However, the spiral inductor which is the major passive components in RF integrated circuits can't obtain high quality factor and occupies too large area.

Active inductor has pulled in much enthusiasm for as far back as couple of years [1-7]. Contrasted to typical on chip spiral inductor, the advantages of AI are large inductance value, high quality factor, small chip area, tunable inductance and quality factor and the likelihood of accomplishing higher inductance with high self-resonance frequency. Use of the AI incorporates Wilkinson power divider, phase shifter, active filter, oscillator, LNAs, current-mode stage bolted circle and matching network [2, 4].

The well-known CMOS active inductors, based on gyrator-C networks, have been designed for applications in high-speed analogue signal processing and data communication where chip area is critical and a large and tunable inductance is essential [1, 3]. Many TGAI and TFAI are designed and suggested for different applications [1-7]. However, a large portion of the already proposed AIs are initially grounded 1-port block. At the point when the 2-port floating characteristics are needed, the grounded node is typically floated just by extra current source and bypass capacitor. These FAIs don't have symmetric structure, they demonstrate to somewhat different characteristics from each port, which deviates from the behavior of an ideal inductor [4-7].

In this paper modified gyrator-C TGAI is designed then its symmetric floating counterpart is suggested. In section 2 system level description of AI is explained. Section 3 describes circuit level implementation of proposed design. Then simulation results is disused in section 4. The conclusion is given in section 5.

2. System level description

An ideal inductor can be presented in admittance form by Signal Flow Graph (SFG) with a weighted arrow (*1/sL*), as it is illustrated in Fig. 1, where *s* is the complex frequency and *L* is the inductance of the inductor.

Current flowing through the inductor is described by equation (1).

$$I_L = 1/(sL)V_L \tag{1}$$

The same transfer function can be obtained by constructing a graph with one capacitor and two Voltage Controlled Current Sources (VCCS) as shown in Fig. 2.

But in order to have high impedance in both input and output nodes SFG of GAI is modified as Fig. 3(a). Fig. 3(b) depicts floating counterpart of GAI.

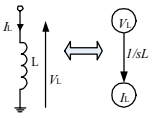

Fig. 1. An ideal inductor and SFG representation

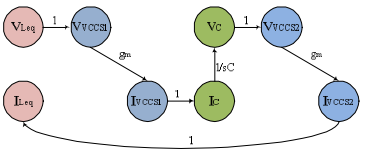

Fig. 2. General SFG for AI's circuit generation with VCCS

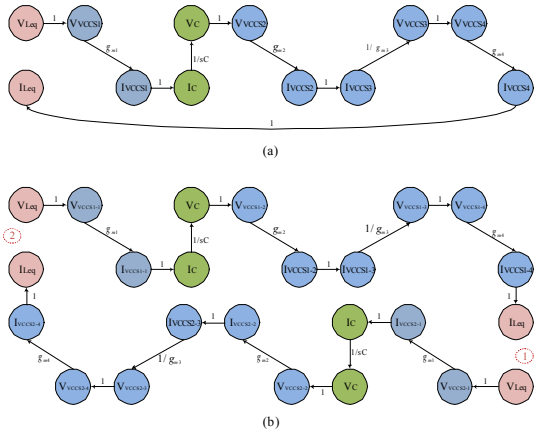

Fig. 3. (a) Modified SFG for Grounded AI. (b) SFG for Floating AI

Thus, the circuit is described by equation (2) for both grounded and floating AI:

$$I_{Leq} = (1/SL_{eq}) * V_{Leq} = g_{m1}g_{m2}g_{m4} / g_{m3}(sC)V_{Leq} \tag{2}$$

Where:

$$L_{Leq} = \frac{g_{m3}C}{g_{m1}g_{m2}g_{m4}} \tag{3}$$

Gyrator-C networks can therefore be used to synthesize inductors. These synthesized inductors are called gyrator-C active inductors. The inductance of gyrator-C active inductor is directly proportional to the load capacitance *C* and inversely proportional to the product of trans-conductors of the gyrator.

The graph presented in Fig.2 can be designed using two classical operational trans-conductance amplifiers (OTAs). Fig.4 (a, b) presents a lossy grounded and floating inductors, respectively.

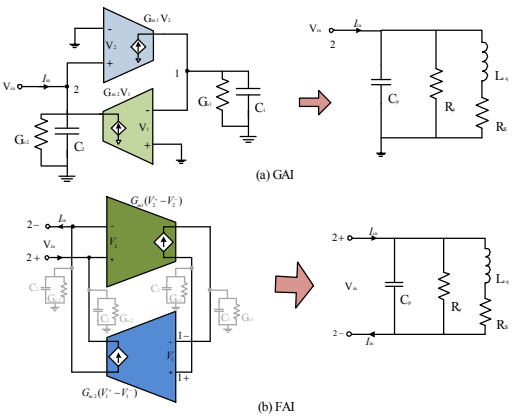

Fig. 4. Block diagram of AI realization by OTA and equilant passive model (a) Grounded (b) Floating

Full In Fig. 4. $C_{1,\ 2}$ and $G_{o\ (1,\ 2)}$ represent the total capacitances and conductances at nodes 1 and 2.

Floating gyrator-C active inductors offer the following attractive advantages over their single-ended counterparts:

1. The differential configuration of the transconductors effectively rejects the common-mode disturbances of the network, making them particularly attractive for applications where both analog and digital circuits are fabricated on the same substrate.
2. The level of the voltage swing of floating active inductors is twice that of the corresponding single-ended active inductors.

A lossy gyrator-C active inductor, however, only exhibits an inductive characteristic over a specific frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor.

$$Z = (\frac{R_s}{C_p L_{eq}}) \frac{s\frac{L_{eq}}{R_s} + 1}{s^2 + s(\frac{1}{R_p C_p} + \frac{R_s}{L_{eq}}) + \frac{R_p + R_s}{R_p C_p L_{eq}}} \tag{4}$$

When complex conjugate poles are encountered, the pole resonant frequency of Z is given by:

$$w_p = \sqrt{\frac{R_p + R_s}{R_p C_p L_{eq}}} \tag{5}$$

Because $R_p \gg R_s$, Eq. (5) is simplified to:

$$w_p \approx \sqrt{\frac{1}{C_p L_{eq}}} = w_0 \tag{6}$$

Where, w_0 is the self-resonant frequency of the active inductor. Also observe that Z has a zero at frequency

$$w_z = \frac{R_s}{L_{eq}} = \frac{G_{o1}}{C_1} \tag{7}$$

The Bode plots of Z are sketched in Fig.5. It is evident that the gyrator-C network is resistive, when $w \le w_z$, inductive when $w_z \le w \le w_0$, and capacitive when $w \ge w_0$. The frequency range in which the gyrator-C network is inductive is lower-bounded by w_z and upper-bounded by w_0. Also observed is that R_p has no effect on the frequency range of the active inductor. R_s, however, affects the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self-resonant frequency of the active inductor, which is set by the cut-off frequency of the trans-conductors constituting the active inductor. For a given inductance L_{eq}, to maximize the frequency range, both R_s and C_p should be minimized.

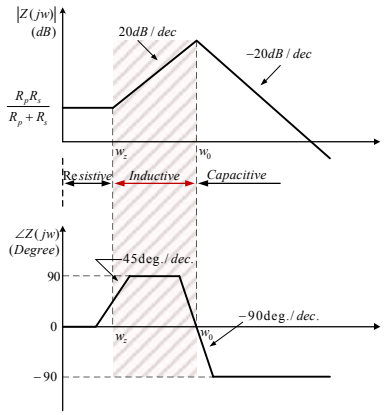

Fig. 5. Bode plots of the impedance of lossy Gyrator-C AI

3. Circuit level design

The basic schematic for a CMOS-based active inductor is shown in Fig. 2 in which there are two schematic of basic gyrator-C active inductors In Fig. 6(a), the trans-conductor with a positive trans-conductance is common gate configured while the trans-conductor with a negative trans-conductance is common-source configured. In Fig. 6(b), the trans-conductor with a positive trans-conductance is common-drain configured while the trans-conductor with a negative trans-conductance is common-source configured. All transistors are biased in the saturation region.

According SFG in Fig. 3(a), the circuit implementation of GAI can be modified as Fig. 7 [1].

The negative transconductance is realized by M_1 in common-source configuration, whereas $M_2 - M_4$ form the positive transconductance where the simple current mirror comprised of $M_3 - M_4$ is used to invert the negative transconductance of M_2, also configured in common-source connection. Since the sole contribution practically comes from a minimum number of MOS transistor drain terminal(s), this configuration allows low

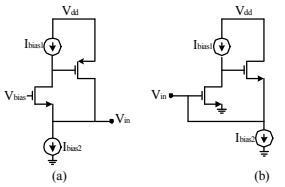

Fig. 6. simplified CMOS-based GAI

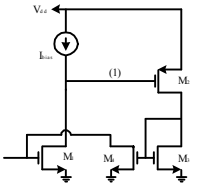

Fig. 7. Modified AI

equivalent conductances especially at node (1) which results in improved performance by decreasing series resistance of equivalent inductance.

The quality factor Q of an inductor quantifies the ratio of the energy stored in it to its ohmic loss in one oscillation cycle, then Q factor can be obtained:

$$Q = \frac{\mathrm{I}M[Z]}{RE[Z]} \tag{8}$$

The quality factor of a lossy gyrator-C active inductor can be derived directly from (4) and (8)

$$Q = \left(\frac{wL_{eq}}{R_s}\right)\frac{R_p}{R_p + R_s\left[1+\left(\frac{wL_{eq}}{R_s}\right)^2\right]}\left[1 - \frac{R_s^2 C_p}{L_{eq}} - w^2 L_{eq} C_p\right] \tag{9}$$

The sensitivity of the quality factor of the active inductor is merely depends on R_s in high frequencies. So to boost the quality factor of active inductors, R_s must be minimized. Reducing R_s is done by using advanced circuit techniques, such as Multi-Regulated Cascodes (MRC) stage. MRC stage is effective in lowering the output conductance and can be used here to reduce R_s, as shown in Fig. 8. In proposed circuit, M_n, M_{c-n} and M_{b-n} transistors are used for main elements of Gyrator-C, MRC stage and biasing, respectively.
MRC stage is made up of PMOS transistors in order to:

- The input transistor will be as small as possible in order to control second stage biasing
- Be free from body effect
- The number of transistors in main path of ac signal will be as minimum as possible

The tunability of AI is enhanced by variation of bias current and varactor value. By considering of SFG and block diagram of FAI in Fig. 3(b) and 4(b), the floating counterpart of proposed GAI is designed as Fig. 9.

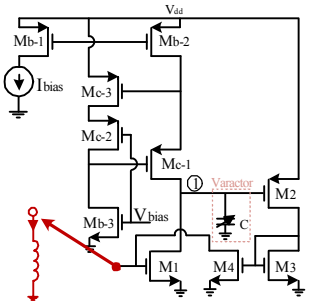

Fig. 8. Modified GAI

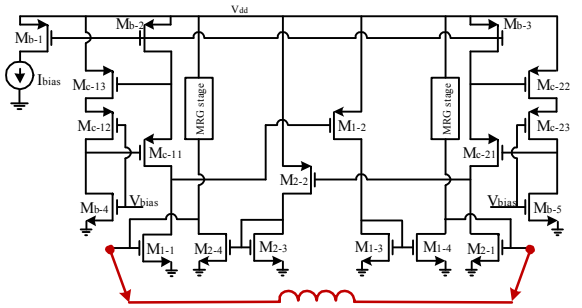

Fig. 9. Circuit implementation of proposed FAI

Standard circuit analysis techniques yield the important parameters of the grounded and floating AI as follows:

$$R_p = r_{04} \qquad R_s = \frac{r_{o1}}{g_{m1}\dfrac{g_{m2}g_{m4}}{g_{m3}}}$$

$$C_p = c_{gs1} \qquad L_{eq} = \frac{c_{gs2} + c_{\text{var}actor}}{g_{m1}\dfrac{g_{m2}g_{m4}}{g_{m3}}} \qquad (10)$$

4. Simulation results

The proposed GTAI and FTAI were designed and simulated using the AMS 0.18um CMOS process in cadence. All transistors have minimum channel length of 0.18 µm and work on saturation region. The width of the transistors, the values of I_{bias} and $C_{\text{var}actor}$ were chosen to optimize the quality factor and inductance value of the AI.

The simulated frequency response of the inductor is given in Fig. 10. The proposed circuit has a very wide operating bandwidth where the inductive characteristic extends from 100 MHz up to the self-resonance frequency at 6.2 GHz which make it suitable for RF applications. Fig. 11 compares GAI with and without MRC stage.

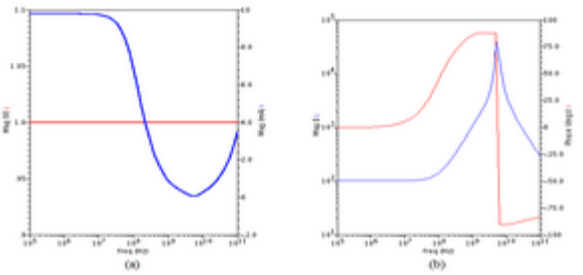

Fig. 10. Input impedance (IP) of AI (a) input voltage and current (b) magnitude and phase

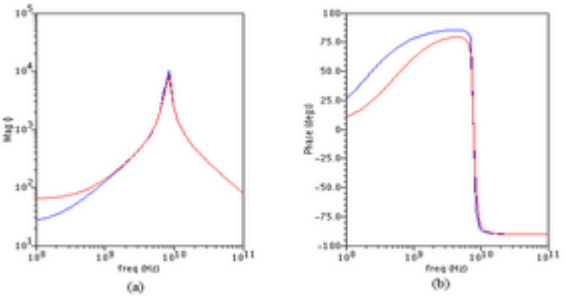

Fig. 11. Compression AI circuits with (blue) and without (red) MRC stage (a) magnitude (b) phase

For investigating the FAI performance, Fig. 12 configuration is used to simulation of ideal and CMOS FAI. The simulation result is shown in Fig. 13.

Quality factor is tuned through the controllable bias current source (I_{bias}) of Fig. 8 and 9. Fig. 14 shows the variation of Z_{input} for different values of controllable bias current source. When I_{bias} is varied, the Z_{input} brings corresponding changes in R_s and L_{eq}. Therefore, the quality factor can be tuned through the controllable bias current source. Table 1 compares the performance of proposed FAI with previous ones.

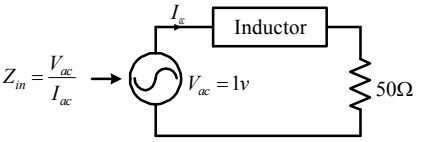

Fig. 12. circuit for FAI simulation

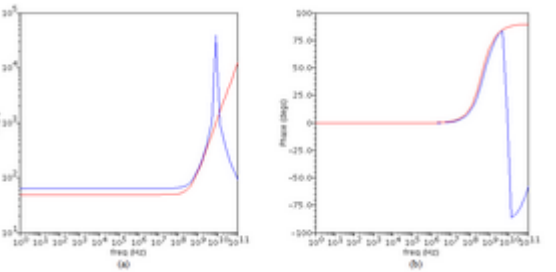

Fig. 13. Floating ideal (red) and active (blue) inductor simulation (a) magnitude (b) phase

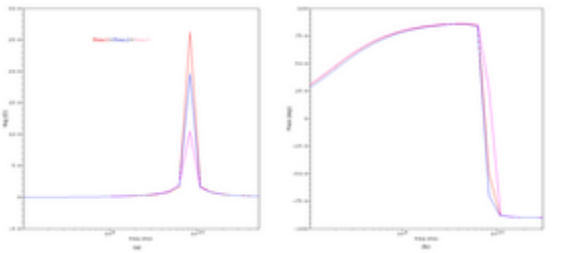

Fig. 14. Tunability of AI by changing bias current (a) magnitude (b) phase

Table 1. Comparison with Other FAI

Ref	CMOS process	V_{DD} (V)	L (nH)	Q	Inductive frequency range (GHz)	DC power (mW)
[3]	TSMC-0.18 um	1.8		40–200	0.375 – 2	3 mW
[7]	AMS-0.8um	3	294-394		1	8.6
[5]	TSMC-0.18 um	1.8	33	68		3.6
[4]	0.35 um	3.3	685uH-12.4mH		0.25-0.75	2
This work	AMS-0.18 um	1.8	6-284	10-567	0.1-6.2	2

6. Conclusion

A new high Q FTAI based on modified TGAI has been designed in this paper. The designed AI is designed on Gyrator-C topology and uses minimum number of transistors in main path of the signal. Therefore, it is suitable for RF applications. A CMOS varactor in the AI circuit is used to adjust the inductance value from few nH to 284 nH in the specific frequency range. Q factor can be tuned by changing bias current from 10 to 567. The dc power consumption of AI is 2 mW from 1.8 V dc power supply. Simulation results are provided for a 0.18 um CMOS-AMS process. Results show that the circuit can be used in many RF applications ranging in the 100 MHz~6.2 GHz frequency band.

7. References

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