WIDEBAND CURRENT CONVEYOR WITH RAIL TO RAIL INPUT STAGE

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ABSTRACT

In this paper an improved, wideband, second generation current conveyor (CCII) with rail to rail input stage is proposed. Wideband voltage and current transfers can be obtained with power consumption less than 1 mW. In addition, rail to rail input stage allows the dynamic range to be very close to supply voltages. A band-pass filter based on the proposed CMOS CCII with centre frequency of 30 MHz is given as an application example. Experimental results of the proposed circuit are included.

I. INTRODUCTION

There is a growing interest in high-frequency continuous time filters for numerous applications in audio-video, data storage and other telecommunication circuits. It is indeed well known that basic operations like, amplification, filtering and arithmetic operations such as addition, subtraction, or multiplication are easier to perform using currents instead of voltages; thus current-mode circuits are being widely used in high frequency circuit design applications [1]. The second generation current conveyor (CCII), introduced in 1970, is a versatile analogue component widely used as an elementary cell in applications of signal processing and as a basic building block in universal active elements. Recently, a great deal of study has been done in order to design high performance, wideband, low parasitic resistance CMOS and BiCMOS CCIIs.

To exploit wideband and wide dynamic range capabilities under low power operation of current-mode signal processing, a CCII based on the translinear loop has been proposed. These translinear CMOS circuits exhibit an excellent current following behaviour from port *X* to port *Z* over a wide bandwidth, but the voltage following property from port *Y* to port *X* is poor and the offset voltage is rather high. Additionally, the use of class AB configurations increases slew-rate. Open-loop structures are very sensitive to the body effect in single-well technologies and consequently high offset voltage and high gain error are exhibited [2-5].

In this paper, a wideband CMOS realization of the CCII based on the long tail differential pair with rail to rail input stage is proposed. The CMOS CCII circuit operates at supply voltages of ± 1.65V with biasing current of 25μA.

II. THE PROPOSED CMOS CCII

The CCII is a three terminal active block as shown in Fig. 1. It ensures two functionalities between its terminals:

- A current follower between terminals *X* and *Z*.
- A voltage follower between terminals *X* and *Y*.

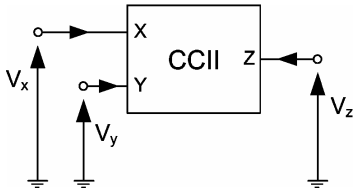

Figure 1. Second generation current conveyor

In mathematical terms, the input-output characteristics of CCII can be described by the following matrix equation:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \qquad (1.1)$$

where ideally $\alpha = 1$, $\beta = 1$, and $\gamma = 1$ and they represent the voltage and current transfer ratios of the current conveyor as described by the matrix equation. The sign of α, plus or minus, denotes positive or negative type current conveyor, respectively [6-9].

A high performance, translinear based CMOS CCII configuration is proposed in [3]. PSPICE simulations for AMS 0.35 μm CMOS technology show that the current and voltage bandwidths are respectively 2.6 GHz and 3.9 GHz and the parasitic input resistance is R_x=18Ω for a control current of 100 μA. This circuit has about 3 mW power consumption.

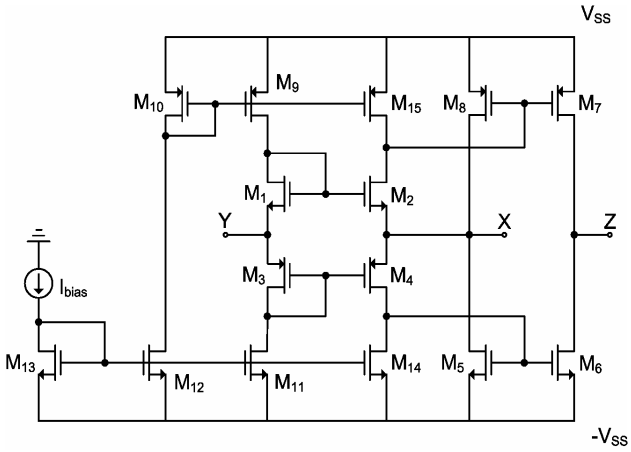

Figure 2. Translinear based CCII proposed in [3]

In this circuit wideband current and voltage transfer can be obtained but the dynamic range is not good enough. It deviates from linearity after ±0.8V (See Fig. 8).

It is known that the n-type based input stage operates in linear region for higher input voltages; while the p-type based input circuit operates in linear region for low input voltages. It is possible to manage input signals from positive supply voltage down to negative supply voltage, rail to rail operation, by using both the n-type and p-type differential pairs together [10]. Joining these two differential pairs in parallel allows implementing the "rail to rail input stage" CCII as shown in Fig. 3. P-type differential pair (M_8 and M_9) operates when the input voltage on port *Y* is low and n-type differential pair (M_7 and M_{10}) operates when the input voltage is high. In order to preserve low parasitic resistance on port *X*, two source followers M_{11} and M_{12} are used.

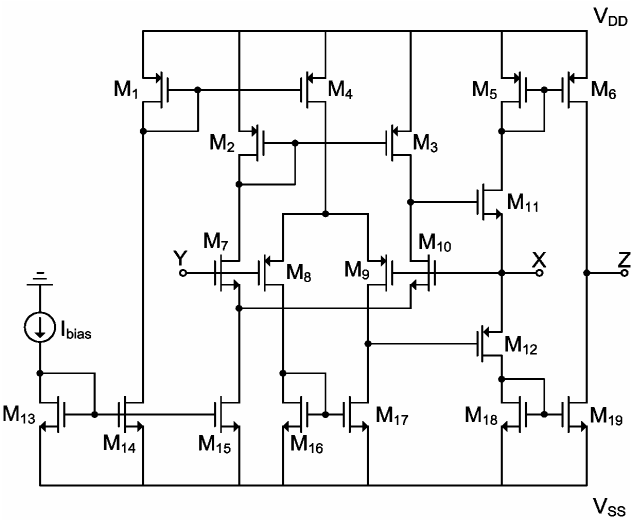

Figure 3. Circuit configuration of the proposed CCII

If we consider the differential pair having the same small signal parameters (equal r_o's), the parasitic resistance on port *X* can be evaluated as: [10]

$$R_x \cong \left(g_{m11}\left(1+\frac{r_o}{2}g_{m10}\right)\right)^{-1} // \left(g_{m12}\left(1+\frac{r_o}{2}g_{m9}\right)\right)^{-1} \quad (2.1)$$

The parasitic resistance on port *Z* can be evaluated as:

$$R_z \cong \frac{r_{o6}r_{o19}}{r_{o6}+r_{o19}} \quad (2.2)$$

III. SIMULATION RESULTS

The characteristics of the current conveyor shown in Fig. 3 have been determined from HSPICE simulations by using 0.35 µm AMS process parameters. If the supply voltage of ±2.5V, biasing current of 100µA and minimum channel length transistors (l=0.35µm) are used, the current and voltage transfer bandwidths are 3.20 GHz and 2.92 GHz, and the current and voltage gains are 1.069 and 0.953, respectively. In order to have low-power consumption, the supply voltages and the biasing current are decreased down to ±1.65V and 25µA, respectively. Moreover, in order to reduce the mismatches between transistors, channel lengths are selected as 0.7 µm. The simulation results in Fig. 4-5 are for the biasing conditions of ±2.5V supply voltage and 25µA biasing current, the simulation results in Fig. 6-7 are for the biasing conditions of ±1.65V supply voltage and 25µA biasing current. Transistors aspect ratios are reported in Table 1. The main performances are summarised in Table 2.

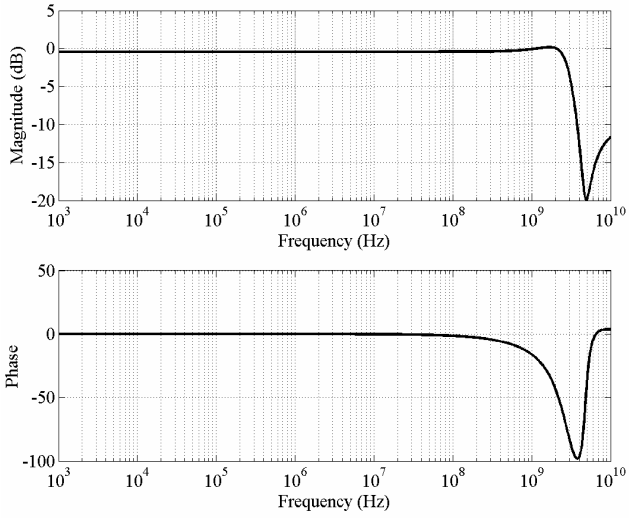

Figure 4. Voltage transfer gain and phase between ports *Y* and *X* (V_x / V_y) with ±2.5V supply voltage and 100µA biasing current.

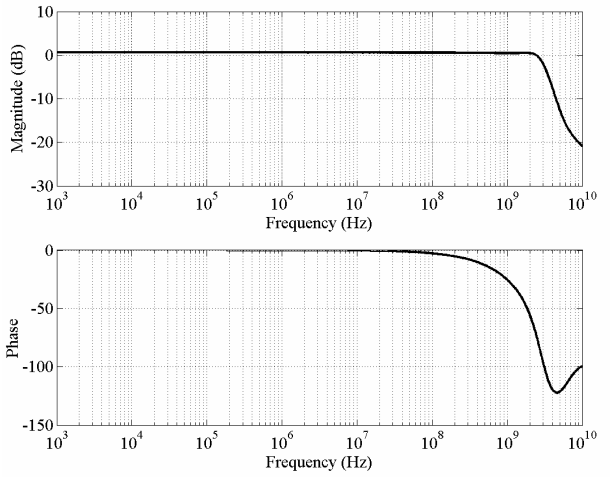

Figure 5. Current transfer gain and phase between ports X and Z (I_z / I_x) with ±2.5V supply voltage and 100µA biasing current

In [3], it is given that the voltage transfer bandwidth is 3.9 GHz, for the same biasing conditions it is 2.92 GHz in the proposed CMOS CCII. The current transfer bandwidth is 2.6 GHz in [3], for the same biasing conditions it is 3.2 GHz in our proposed CMOS CCII. Voltage transfers of the conveyor are determined with infinite load R_L connected at X with output Z grounded. Current transfers are determined with an input current applied on port X. The current I_z is then the current that flows through port Z to the ground; port Y being also grounded.

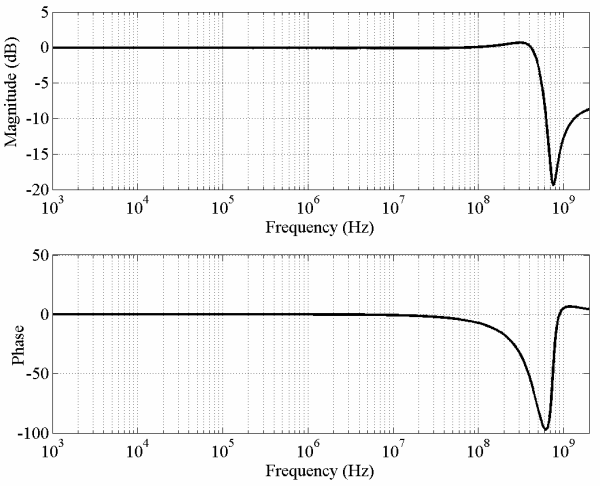

Figure 6. Voltage transfer gain and phase between ports Y and X (V_x / V_y) with ±1.65V supply voltage and 25µA biasing current

It can be seen that the voltage transfer bandwidth is decreased to 512 MHz but also the power consumption is decreased from 6 mW down to 815 µW.

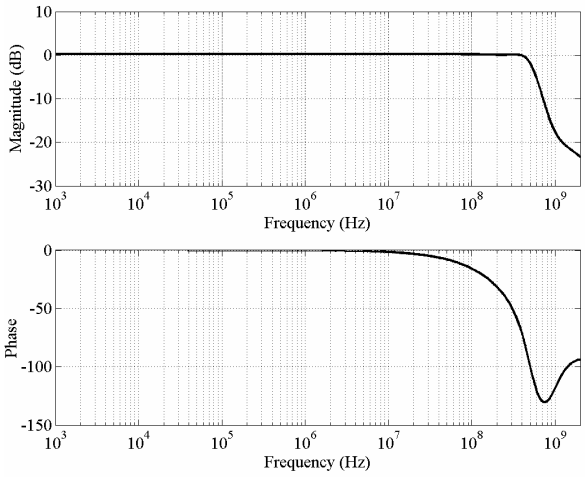

Figure 7. Current transfer gain and phase between ports X and Z (I_z / I_x) with ±1.65V supply voltage and 25µA biasing current

The current transfer bandwidth is decreased from 3.2 GHz to 572 MHz.

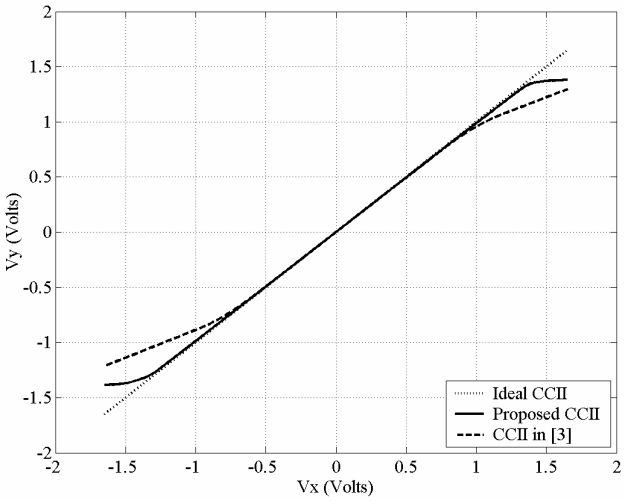

Figure 8. Voltage transfer characteristics from port Y to port X

The most important advantage of the proposed circuit is the improvement of the dynamic range. The figure above shows that by using n-type and p-type differential pairs in parallel, rail to rail input stage, it is possible to have better dynamic behaviour between ports X and Y. The proposed circuit operates linearly in the range of ±1.35V, while the circuits employing translinear-loop input stage, like the circuit in [3], deviate from linearity after ±0.8V. Moreover, it is mentioned in [3] that, when compared to the parasitic resistance on port X of the basic translinear based CCII configuration, a very good reduction is obtained and the value of R_x is 18Ω. In our proposed CCII configuration, this parasitic resistance has a lower value which is 12.6Ω.

Table 1. Aspect ratios of the transistors

Transistor	Aspect Ratio, W/L
M_1, M_2, M_3, M_5, M_6, M_{12}	30/0.7 (μm)
M_4, M_8, M_9	60/0.7 (μm)
M_7, M_{10}, M_{15}	20/0.7 (μm)
M_{11}, M_{13}, M_{14}, M_{16}, M_{17}, M_{18}, M_{19}	10/0.7 (μm)

Table 2. Performance characteristics of the CMOS CCII

Summary of CCII Performance	
Supply voltage (V_{dd}-V_{ss})	+3.3 V
Biasing current (I_{bias})	25 μA
Power dissipation	815 μW
Number of transistors	19
Voltage gain, V_x / V_y	0.9896
Voltage transfer BW	512 MHz
Current gain, I_z / I_x	1.0284
Current transfer BW	572 MHz
Offset voltage on X	16 μV
Offset current on Z	1.49 μA
Port X resistance	12.6 Ω
Port Y capacitance	96 fF
Port Z impedance	190 k Ω// 33.5 fF

IV. APPLICATION EXAMPLE

As an application example, a wideband, high output impedance, current mode band-pass filter circuit is designed and represented in this section. The topology of the filter is shown in Fig. 9.

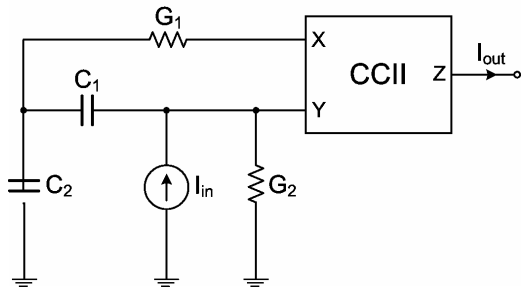

Figure 9. Band-pass filter circuit employing the proposed CMOS CCII

It is based on a single CCII block with minimum number of passive elements with the transfer function as:

$$\frac{i_{out}}{i_{in}} = \frac{C_2 G_1 s}{G_1 G_2 + (C_1 + C_2) G_2 s + C_1 C_2 s^2} \tag{4.1}$$

Band-pass filter condition for this transfer function is:

$$G_1 = \left(1 + \frac{C_1}{C_2}\right) G_2 \tag{4.2}$$

After applying the condition, band-pass filter transfer function can be obtained as:

$$\frac{i_{out}}{i_{in}} = \frac{(2G/C)s}{s^2 + (2G/C)s + (2G^2/C^2)} \tag{4.3}$$

The centre frequency and the quality factor for the band-pass filter can be obtained as:

$$w_0 = \frac{\sqrt{2}G}{C},\ Q = \frac{\sqrt{2}}{2} \tag{4.4}$$

The functionality of the filter circuit is illustrated with the element values of R_1=750Ω, R_2=1.5kΩ, C_1=5pF, C_2=5pF, which determine the centre frequency as f_o=30 MHz. Simulation results show that the response of the proposed circuit is very close to the ideal filter response.

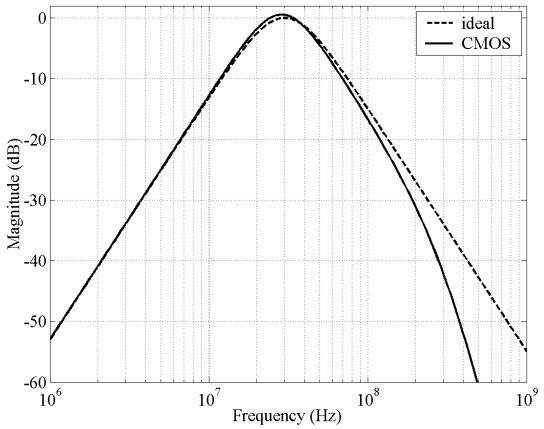

Figure 10. Simulation results of ideal and proposed current mode BP filter configuration

V. CONCLUSION

In this paper, wideband current conveyor with rail to rail input stage is proposed. By using 0.35 μm CMOS technology of AMS, high frequency performances were obtained. For the ±2.5V supply voltage and 100μA biasing current, the current and voltage bandwidths are 3.20 GHz and 2.92 GHz, respectively. In these biasing conditions, total power dissipation is about 6mW. In analogue IC design, minimum channel length transistors are not recommended in order to get rid of the mismatches. So, the new circuit is modified such that, both the supply voltage and biasing current is decreased down to ±1.65V and 25μA, respectively in order to decrease the power consumption and the channel lengths are selected as 0.7 μm for better matching. For the biasing conditions stated above, 572 MHz current transfer bandwidth and 512 MHz voltage transfer bandwidth are obtained. The parasitic resistance at port X has a value of 12.6Ω. The most important advantage of the proposed

CMOS CCII is the increase of the dynamic range. Our circuit operates linearly in the range of ±1.3V, while the circuits given in the literature [3] deviates from linearity after ±0.8V, as seen in Fig. 8. Additionally, the parasitic resistance on port *X* has a smaller value when compared to the CCII in [3]. A wideband, high output impedance band-pass filter based on the proposed CCII is given as an application example. The simulation results are in good agreement with the theoretical one.

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