A FREQUENCY SYNTHESIZER WITH COINCIDENCE MIXER

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ABSTRACT

The aim of frequency synthesis is to generate an arbitrary frequency from a given standard frequency. Today, the frequency synthesizers are also an essential part of any modern transceiver system. They generate clock and oscillator signals needed for up and down conversion. The fine frequency resolution, low spurious signals, accuracy and stability are most important for these devices. In this paper, the new frequency synthesizer architecture based on direct synthesis and coincidence mixer is presented. The simulation results are also shown.

I. INTRODUCTION

Several different frequency synthesis techniques have been presented in the literature over the years. They can be quite clearly divided into three separate categories, namely direct analog synthesis, direct digital synthesis, and indirect analog synthesis. In this context, "indirect" refers to a system based on some kind of a feedback action, whereas "direct" refers to a system having no feedback. One of the most frequently used indirect synthesizer types is the phase-locked loop (PLL). Phases of two signals, i.e. from an external reference and a feedback signal from an oscillator are compared in a phase and frequency detector. Any phase difference will be converted into a voltage by means of a charge pump. A succeeding loop filter extracts the DC component of this voltage, which is then used to control the output signal frequency of a voltage-controlled oscillator (VCO). A PLL provides high output frequency accuracy at reasonable short settling times [1], [2], [3].

In direct analog synthesizer the frequency resolution is achieved by mixing signals of certain frequencies, and then dividing the resulting frequency down. Theoretically, this process can be repeated arbitrarily many times to achieve a finer frequency resolution. Advantages of the direct analog synthesis are very fast switching times and, in theory, arbitrarily fine frequency resolution. However, this technique requires a very large amount of hardware. Also noise is a problem in direct analog synthesis [4]. An alternative architecture for frequency generation is the direct digital synthesis (DDS), e.g. [5], [6]. The output signal is generated in the digital domain with the help of accumulators and a ROM before it is converted to an analog output signal in a D/A converter. The advantages of direct digital synthesizers are good frequency resolution and very fast settling time while showing low spurious noise. As most of the DDS architecture is digital, a high degree of integration can be achieved. However, the accumulator clock must be faster (at least two times) than the generated output frequency which limits the use of DDS applications [7], [8].

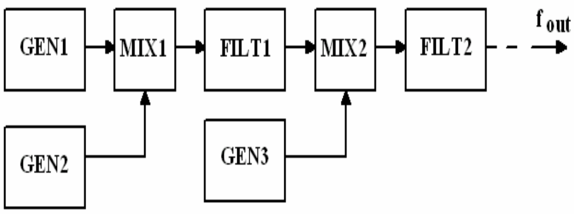

Fig. 1. The block diagram of a conventional direct analog frequency synthesizer. GEN - generator, MIX - mixer, FILT - bandpass filter.

II. DIRECT - FINE STEP SYNTHESIZER

The block diagram of a conventional direct analog frequency synthesizer is shown in Fig. 1. In this paper frequency synthesizer is based on programmable dividers, multipliers (based on PLL) and coincidence mixers, therefore no filters are need for this synthesizer. For this architecture, Cantor series approximations and Diophantine equations theory are used fine frequency step generation [9].

Let N_1 , N_2 , . . . N_k be relatively prime positive integers (GCD - Greatest common divisor of N_1 , N_2 , . . . N_k =1). Then for every integer u, there exist a k integers X_1, X_2 , . . . X_K, solving the linear Diophantine equation:

$$\frac{X_1}{N_1} + \frac{X_2}{N_2} + \ldots + \frac{X_k}{N_k} = \frac{u}{N_1 N_2 \ldots N_k} \qquad (1)$$

If N_1 , N_2 , . . . N_k are relatively prime positive integers, then for every integer u such that:

$$-N_1 N_2 \ldots N_k \leq u \leq N_1 N_2 \ldots N_k \qquad (2)$$

the equation (1) has a solution ($X_1, X_2, \ldots X_K$), where that $-N_i \leq X_i \leq N_i$ for all $i=1,2,\ldots k$. It is important to say, that equation (1) has a k solutions (for $-N_i \leq X_i \leq N_i$).

Example 1:

$N_1=7$, $N_2=9$, $N_3=11$ and $u=1$. The solutions of (1) are shown in Tab. 1.:

X_1	X_2	X_3	***Sum***
-6	2	7	89
1	-7	7	99
1	**2**	**-4**	**21**

Tab. 1. Example of solution (1) for $N_1=7, N_2=9, N_3=11$ and $u=1$. Solution [1, 2, -4] is optimal.

In Tab. 1., numbers in column "**Sum**" are computed according (3):

$$Sum = \sum_{i=1}^{k} X_i^2 \qquad (3)$$

and optimal value is minimal according eq. (3). Therefore, *Example 1* has 3 solutions:

$$(1/7)+(2/9)+(-4/11) = (-6/7)+(2/9)+(7/11) =$$
$$(1/7)-(7/9)+(7/11) = 1/(7*9*11) = 1.443.10^{-3}$$

Example 2:

$N_1=7$, $N_2=9$, $N_3=11$ and $u=10$. The optimal solution of (1) is: [-4, 2, 4] (also [3,-7, 4] and [3, 2,-7]). Optimal values of X_1 , X_2 , X_3 for values $N_1=7$, $N_2=9$, $N_3=11$ and $u/(N_1 N_2 N_3) =<0, 0.2>$ are shown in Fig. 2.

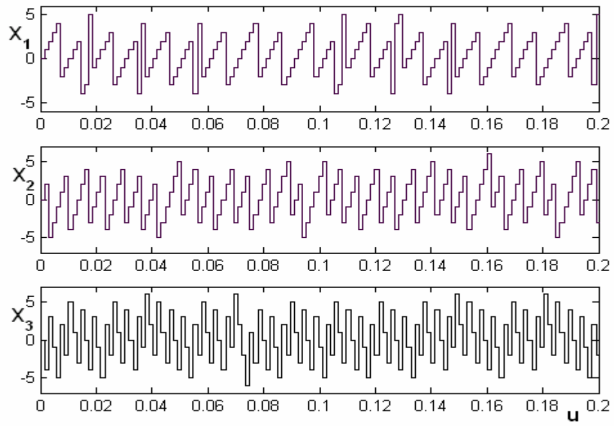

Fig. 2. Optimal values of X_1 , X_2 , X_3 for *Example 1* and $u/(N_1 N_2 N_3) =<0, 0.2>$.

For frequency synthesizer consist of k dividers and multipliers the minimal frequency and minimal frequency step is given by (4):

$$Frequency\_step = \frac{f_{REF}}{\prod_{i=1}^{k} N_i} \qquad (4)$$

For *Example 1*, *Frequency_step* $= 1.443.10^{-3} f_{REF}$, and the hardware implementation part of (X_i/N_i) is shown in Fig. 3. This can be simplified according Fig. 4.

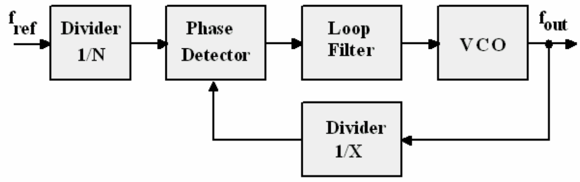

Fig. 3. Simplified hardware implementation of *(X/N)* part.

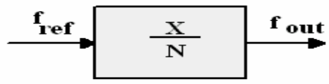

Fig. 4. The *(X/N)* part of Fig. 3 as a single block.

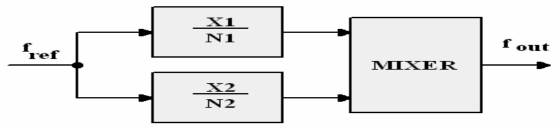

Fig. 5. Block diagram of synthesizer part (with mixer).

Output frequency *(X/N)* part (Fig. 3) is given by (5):

$$f_{OUT} = \frac{X_i}{N_i} f_{REF} \qquad (5)$$

Synthesizer part block diagram is shown in Fig. 5. Output frequency (Fig. 5) if given by (6):

$$f_{OUT} = \left(\frac{X_1}{N_1} + \frac{X_2}{N_2}\right) f_{REF} \qquad (6)$$

The block diagram of final version of frequency synthesizer with 3 *"(X/N)"* blocks is shown in Fig. 6. Output frequency of this synthesizer (for 3 blocks of *X/N*) is given by equation:

$$f_{OUT} = \left(\frac{X_1}{N_1} + \frac{X_2}{N_2} + \frac{X_3}{N_3}\right) M_4 M_5 f_{REF} \qquad (7)$$

Structure of synthesizer (Fig. 6) can be simply extended for more *"(X/Y)"* block. The N_1, N_2, N_3 are fixed dividers and X_1 , X_2 , X_3 are programmable dividers in PLL feedback. The M_4 and M_5 are frequency multipliers (also based on programmable dividers in feedback of PLL). These PLL are used for signal shape recover (from pulses to sine). Control block can be built with microcontroller or programmable array [10], [11].

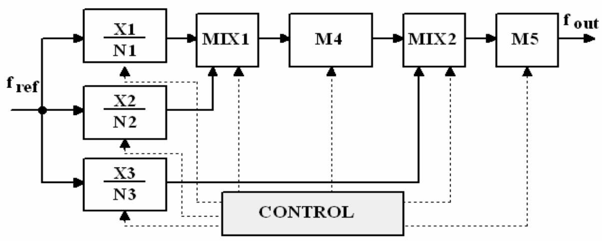

Fig. 6. Final version of frequency synthesizer with 3 blocks *(X/N)*. The blocks M4 and M5 are PLL which acts as frequency multipliers and signal shape recover.

III. COINCIDENCE MIXER

As a review, let's look at an conventional analog mixer, which performs the function of multiplication between two inputs. Analog mixing implements the following trigonometric identity:

$$C = AB = \cos(2\pi f_a t)\cos(2\pi f_b t) = \\ = \frac{1}{2}[\cos(2\pi(f_a + f_b)t) + \cos(2\pi(f_a - f_b)t)] \quad (8)$$

and bandpass filtered output D (depend on filter quality):

$$D \approx \frac{1}{2}[\cos(2\pi(f_a + f_b)t)] \quad (9)$$

There are some problems with filtering when frequencies $(f_a + f_b)$ and $(f_a - f_b)$ are close each other and tuning filter when frequency changing. Therefore new coincidence mixer was developed.

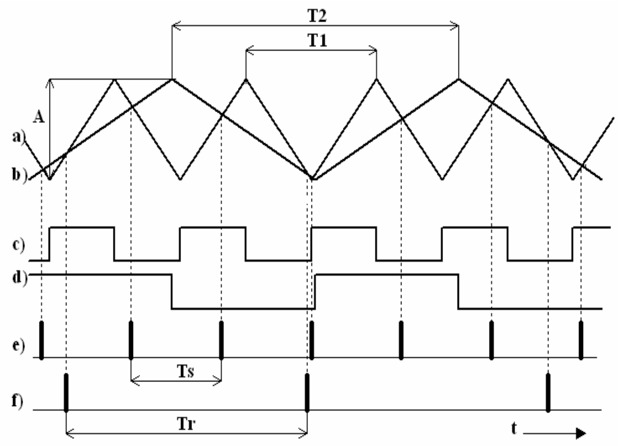

Fig. 7. Coincidence mixer time diagram. a) input signal with frequency f_1 (period T_1), b) input signal with frequency f_2 (period T_2), c) derivation of signal a), d) derivation of signal b), e) output pulses with frequency $f_S = f_1 + f_2$ (period T_S) f) output pulses with frequency $f_R = abs(f_1 - f_2)$ (period T_r).

The new coincidence mixer work with input signals, which must have the same amplitude values. The principle is shown in Fig. 7, with triangle wave. The time diagrams of signals with sine wave are shown in Fig. 8. and Fig. 9.

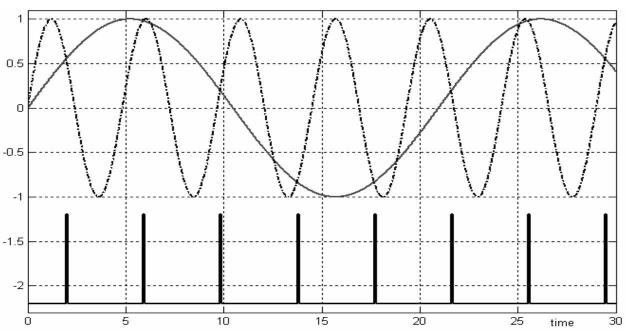

Fig. 8. Coincidence mixer - time diagram (Simulation result). Input signals (top) and output pulses (bottom). Frequency of output pulses is sum of input frequencies.

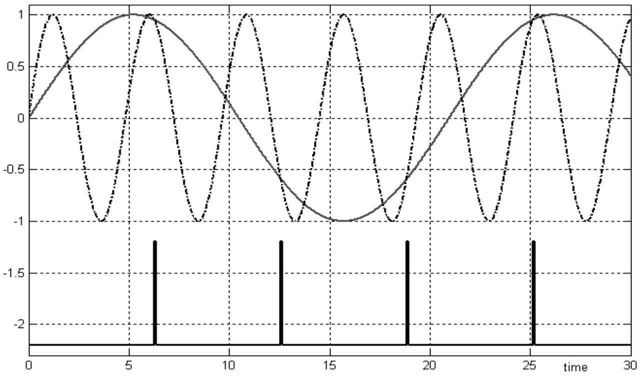

Fig. 9. Coincidence mixer - time diagram (Simulation result). Input signals (top) and output pulses (bottom). Frequency of output pulses is difference of input frequencies.

From Fig. 8 and 9 can be seen, that coincidence mixer can generate sum and difference of input frequencies on outputs, and outputs signals shapes are pulses. In Fig. 8 and 9, the frequency of input signals were 0.3 and 1.3 [rad/sec], therefore sum output is 0.3+1=1.6 and difference output is 1.3 - 0.3 =1 [rad/sec].The simplified block diagram of coincidence mixer is shown in Fig. 10.

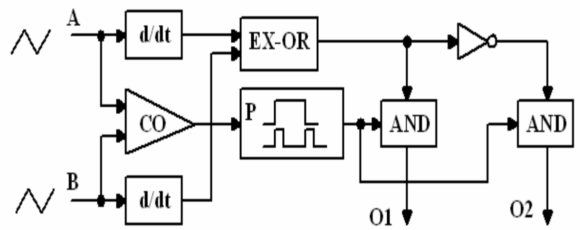

Fig. 10. Block diagram of coincidence mixer. A, B - input signals, d/dt - derivation block, CO - comparator, P - pulse block which generate pulse on rising and falling edge, EX-OR - exclusive-or gate, AND - logical and gate, O1 - output with sum of input frequencies, O2 - output with difference of input frequencies.

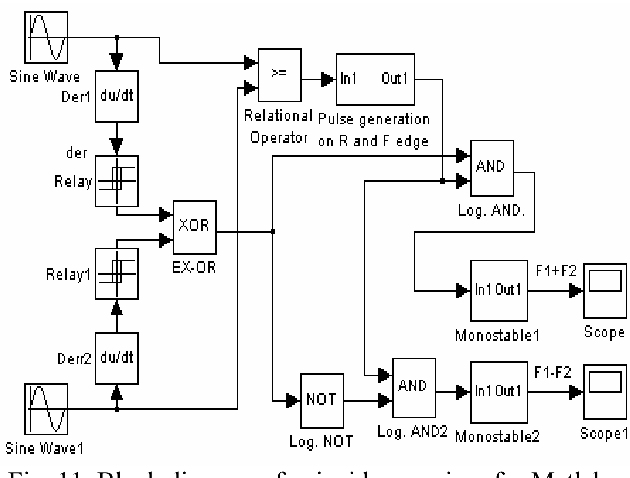

Fig. 11. Block diagram of coincidence mixer for Matlab-Simulink simulation. The mixer has 2 output F1+F2 and absolute value of F1 - F2. The Relay blocks are used as a converter to digital signal level.

IV. SIMULATION RESULTS AND DISCUSSION

From simulation results shown in Fig. 8 and Fig. 9 can be seen, that mixer output pulses are equally spaced and therefore good spectral purity for sum and difference frequencies. The main drawback of this synthesizer is pulsed output and therefore PLL on output is need for recovery triangle or sine output. The second disadvantage is: The same amplitude of input signals is need. The first main advantage of this mixer is that no output filter is need and therefore it has a wide frequency bandwidth without any tuning. The second advantage is almost pure digital architecture (only comparator and derivation function are not pure digital). The third, sum and difference of frequencies can be simply generated. Example of simulation results are shown in Fig. 12 (sine signal recovery) and Fig. 13 (frequency spectrum).

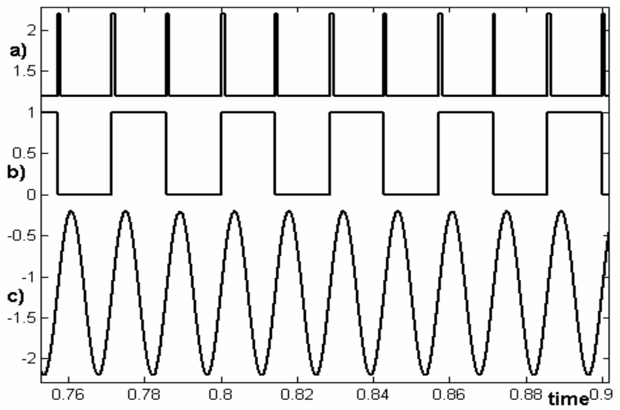

Fig. 12. The sine signal recovery. a) Mixer pulse output, b) Square wave pulses, c) Sine signal (PLL output).

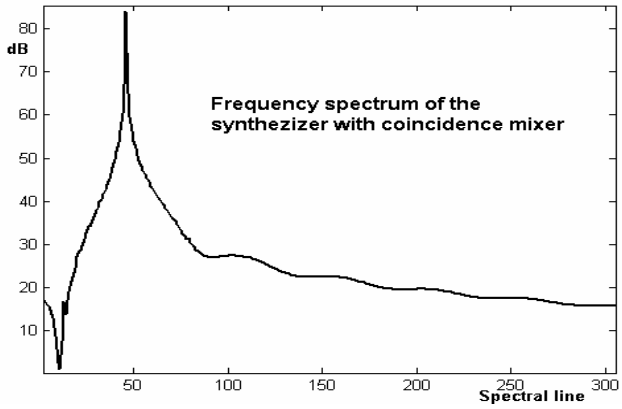

Fig. 13. Frequency spectrum of the frequency synthesizer.

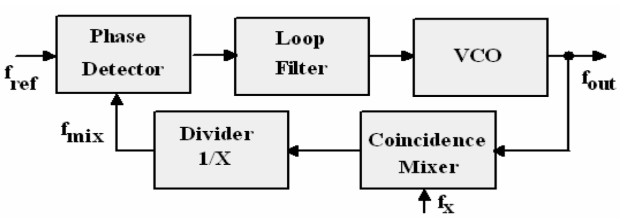

Fig. 14. The Phase-Locked-Loop with coincidence mixer and divider placed in feedback.

V. FRACTIONAL SYNTHESIZER WITH MIXER

The coincidence mixer can be also used directly in PLL feedback for some PLL construction. Block diagram of this system is shown in Fig. 14. For reference frequency f_{ref} and f_x frequency connected to mixer, the output frequency f_{out} is given by:

$$f_{out} = X(f_{ref} \pm f_x) \tag{10}$$

where X is divider number in feedback of and $\pm$ depend mixer output (difference or sum).

VI. EXPERIMENTAL RESULTS

The coincidence mixer was also constructed (according Fig. 10) and measured (Fig. 15). The two function generators GEN1 and GEN2 were used with triangle and sine signal outputs. The mixer has a 2 pulse outputs with sum of input frequencies f_{SUM} and difference of input frequencies f_{DIF}. The results are shown in Fig. 16 - 18. Only sum of frequencies output is shown.

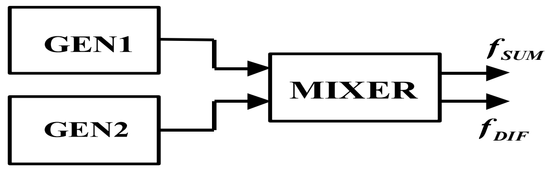

Fig. 15. The block diagram of mixer experimental measuring. GEN1 and GEN2 - functional generators, MIXER - coincidence mixer with f_{SUM} and f_{DIF} outputs.

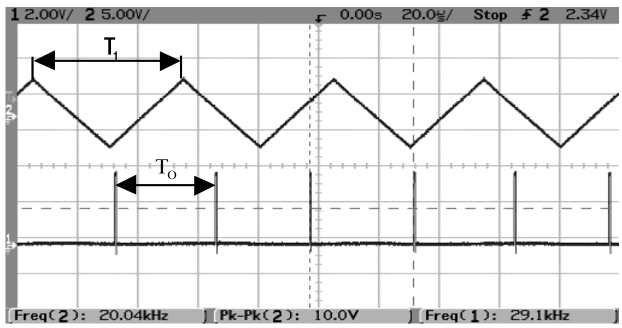

Fig. 16. The input signal with frequency 20.04 kHz (top) and output pulses with frequency 29.1 kHz (bottom). The frequency of second input signal was 9.06 kHz. T_1 - period of input signal, T_O - period of output.

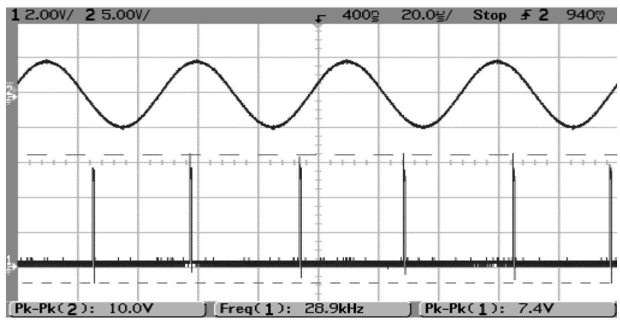

Fig. 17. The coincidence mixer with sine input signal (top) and output pulses (bottom).

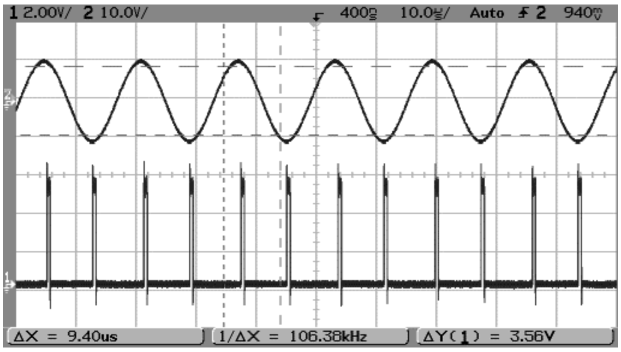

Fig. 18. The coincidence mixer used as frequency doubler. Input signal (top), output pulses (bottom).

VII. CONCLUSION

A detailed look at the concept of frequency synthesizer with new mixer, based on coincidence has been presented in this paper. Analysis, simulation and experimantal results of the synthesizer were also shown.

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