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MODELLING OF SUBMICRONIC MOSFET's AGEING EFFECTS USING SPICE

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Abstract

In this work we develop a submicronic transistor model (narrow and short channel) to study the MOSFET's ageing by the charge pumping technique. In this model, implemented in SPICE3F4, the majority of the physical effects have been incorporated for the different functioning regions. They concern the reduction mobility effect, the carriers velocity saturation, the channel length modulation, the short channel effect, the threshold voltage variation with the reverse bias voltage (V_{rev}), and the distribution of the interface states. The obtained results are compared to other theoretical and experimental results.

1. Introduction

The charge pumping technique [1] constitutes a powerful electrical analysis tool, allowing to follow the evolution of the interface traps parameters in the submicronic devices. This technique has been used to analyze the MOSFET's degradation [2,3], that generally leads to the creation of a fixed trapped charge in the oxid's layer and defects electrically active in the oxide-semi-conductor interface, after an ageing stress (ionizing radiation, hot carriers injection). This ageing is as pronounced as the dimensions are weak. It constitutes the principal challenge that the submicronic micro-electronic has to overcome.

In this work, we develop a submicronic physical model, allowing to study the charge effects and the interface states in the transistor gate. We have also taken into account the possible adaptation of the new techniques (three level charge pumping, spectroscopic charge pumping [4]...) to our model. In the same way, a transcient study was made, where we evaluate the variation of the pumped current when the gate of the MOSFET transistor is submitted to trapezoidal pulses. This analysis allowed us to characterize, with a hight precision, the MOSFET's interface Si-SiO₂, for very weak transistor dimensions (submicronic). The comparison of the simulations to measurements has allowed to validate the interesting results obtained with our Model.

2. Modelling

A model being only an approximation so as to get the best compromise between the calculations complexity and the model approximations, we have to know the physical phenomena which govern the device fonctioning and the limits of their validity.

Our developed model provides a simple tool, but useful for the investigation of the device miniaturisation limitations. First, we have developed the mathematical models corresponding to the regions 1 and 2 (Fig. 1), in which the expression of the pumped current for the region 3 is given by the equation (1). $I_{cp} = BLog \left(C.(\sigma_n.\sigma_p)^{1/2}.(V_{fb}-V_{fb})/\Delta V_{g}(T_r.T_f)^{1/2}\right)$ (1)

With B = 2. q. f. Dir. Act. K T and C = Vith. nj.

where q is the electron charge, f the frequency, D_{it} the interface state density, A_{eff} the effective area of the gate, K the boltzman constant, T the temperature, Vi_{thT} the termic velocity of the carriers and n_i the intrinsic concentration. σ_n and σ_p are the capture cross sections of the electrons and the holes, V_{fb} and V_{th} are the flat band and the thershold voltages, ΔV_g the gate voltage magnitude. T_r and T_f are the rise time and the fall time of the pulse. This proposed model, implemented in SPICE3F4; takes into account the three parameters : D_{it} , Q_{ox} (the oxyde charges) and θ (the degradation coefficient).



Even in the very recent works, the expressions of the current for the two regions 1 and 2 are not given. Taking as a basis the physical phenomena and some mathematical tools, we were able to determine the expressions that well approach our results to the measurements.

The region 1 is a region of accumulation, where the intensity of the pumped current, (the leak current of source/substrat and drain/substrat junctions) is given by [5] as follows:

$$I = q.A_{eff} \cdot (D_{n}/\tau_{n})^{1/2} \cdot n_{i}^{2} + q. A. n_{i} \cdot (w/\tau_{e})$$
(2)
(2)

$$n_i(1) = 3,9.10^{\circ}.1^{\circ}.e^{-g \pi i}$$
 (3)

where A is the jonction's area, D_n is electron diffusivity, τ_n and τ_p the electron and hole life time, W the depletion region depth and E_g the silicon band gap.

The first term of expression (2), proportional to n_{1}^{z} , represents a distribution term, whereas the second, proportional to n_{j} , is a generation-recombination term.

The region 2 is a linear region, corresponding to the transition from accumulation to inversion and vice versa. The expression of the developed mathematical model concerning the pumped current is given by:

$$I_{cp} = D_1 \cdot 1,587.(1 - \exp(w_3)) + I_{leak}$$
 (4)

With $w_3 = (\Delta V_g V_{fb}) / (V_{fb} - V_{tb})$, I_{leak} : The leak current, D_T : expression depending on the different parameters of I_{cpusax} , and the value (1.587) is a constant deduced from the product of the charge (q), the thermodynamic potential (kT/q) and some constant magnitudes.

3. Results and discussions

In the simulation result given in Fig.2, for a short channel and thin oxide transistor (L=0,8, W=4), the measured current in the substrate, called the pumped current, was too small (pA). This is in a good agreement with the measurements.

There is no a rising time, during the crossing from the accumulation to the linear region. This will allow us to have a good continuity, in the mathematical model, for the two regions of the accumulation and the transition.

But in the Fig.3, for a transistor of L=0,7 μ m, W=20 μ m, T_{ox} = 12 μ m, we observe a good variation of the pumped current, compared to measurements. Indeed, the magnitude of the simulated results is almost negligible when compared to the experimental pumped current's maximal value, it will be considered as a null magnitude by the simulator. In addition, a total shift of this curve is observed according to the magnitude and the type of the charges injected in the oxide. The magnitude's order well agree with the measurements. Notice that the expression of the leakage current is taken into account during the simulation. For the validation it is considered null.

The variation of the threshold voltage V_{tho} observed in the figures 2 and 3, is due to the variation of V_{rev} but there is a small shift (0,1 V) in comparison to the measurements. This is due to the different parameters, as the doping of the substrat and the Source-Drain junction depth, which are taken by default in the simulation.

Finally, we can notice that during the measurements, the sensitivity of the measuring apparatus and the stability of the pulse generator play an important role compared to the simulation.







Fig.3 Icp = $f(V_{GH})$ characteristic.

Nevertheless, we can claim that our results well agree with the measurements. In the same way, a study concerning a transistor with large and long channel ($L = 25\mu m$, $W = 25\mu m$, Tox = 12nm) (Fig.2), shows that the increase of the dimensions provokes an increase of the current (some nA). For several values of the voltage V_{rev} , there is no change in I_{cpumpo} but there is a light variation of the threshold's voltage. The figure 4, obtained for $V_{gh} = 2V$, and fixed during the simulation, shows that the variation of I_{cp} versus V_{gl} for ΔV_g fixed, is obtained with small variations at the transition. The maximal value of the simulated I_{cp} is in good concordance with the measurements.

The influence of the oxide charge and the interface states provokes a shift of the curve either to left or to right, according to the type of charge [6] as defined by Tpc in Spice.

In general, the results well agree with the measurements. However, during the crossing from the saturation to the accumulation, we can notice the absence of the null current region. This can be explained by the fact that the choosen values of electron and hole capture cross sections are different from the experimental values. The static study concerns the variation of the drain current Ids as a function of the bias voltage, as well as the transconductance, which must inform us about the MOSFET's degradation magnitude [7].

Therefor, the relationship betwen this static study and the charge pumping technique is given by the equation which links betwen the pumped current (Icp) and the drain current IDS, given by [8] :

 $I_{cp}/I_{DS} = 2 \cdot \exp(-1.7.10^6/E_m)$ (5)

Where E_m is the electrical field. $E_m = (V_D - V_{dsat}) / 0.2 \cdot T_{ox}^{-1/3} \cdot X_j^{-1/3}$, where X_j is the junction depth. For the validation of the CPM model, we have used the measurements carried out using the different models such in [9] (BSIM1, BSIM2, MOS6...). Then we compare the caracteristics $(I_{DS} = f(V_{DS}))$, with those simulated by our model. Generally, we follow the evolution of IDS, with the same parameters given for Icp.

The Curves of the figures 5 and 6, show the simulated voltage-current characteristics and the figure 7 shows the variation of the charge pumping current with the low gate pulse level. We obtain a good agreement with the measurements [2,3].



Fig.4 $I_{DS} = f (V_{DS})$ characteristic for : $V_{fb} = -1,008V$, $D_{it} = 1 \ 10^{10}$, $N_{ss} = 1,36 \ 10^{12}$ and $V_{rev} = 0.1V$.

4. Conclusion

The charge pumping technique allows to distinguish between the oxides charges and the interface states, and inform us about the damaged region of the channel [5] as shown in Fig.7, obtained by using the implemented model.



Fig.5 Icp = $f(V_{GH})$ characteristic for : f = 100khz, $V_{GL} = -2V, V_{rev} = 0.5V.$







1. Icp = $f(V_{GL})$ characteristic at $\Delta V_G = 5V$.

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5. References

[1] G. Groeseneken H.E. Maes, N. Beltran and R.F. Dekeersmaecker, "A reliable approch to charge pumping measurements in MOS transistors", IEEE trans-electron devices, 1984, Vol. N° 1, pp.42-53.

[2] F. Djahli " Mise au point d'un dispositif expérimental pour l'étude des structures MOS : application à l'étude du vieillissement des TMOS microniques par la technique de pompage de charge". Thèse Doct. : Institut National des Sciences Appliquées de Lyon, 1992, 141 p.

[3] F. Djahli and L. Kaabi "A macro model in SMART SPICE to study MOSFET degradations with the CP technique" Microelectronics Journal 29, 1998, pp. 805-811.
[4] J.L. Autran, F. Djahli, B. Balland, C. Plossu and L.M. Gaborieau, "Three-level charge pumping on submicronic MOS transistors", Solid State Commun, 1992. Vol. 84, N°6, pp 604-611.

[5] D. Vuillaume, "Nature et mécanismes de création des défauts induits à l'interface Si-SiO₂ par injections⁻

homogènes de porteurs à travers l'oxyde de grille", J.phys, 1992, Vol. N°6, pp.947-978.

[6] I.S. Brugler and P.G.S. Jespers, "Charge pumping in MOS devices", IEEE trans electron devices, 1969, Vol. 16, pp.297-302.

[7] F. Djahli, J.L Autran, C. Plossu and B. Balland. "Use of charge pumping technique to understand non uniform n channel MOSFET degradation", Mat.Sci.eng.B, 1994, Vol. 23, N°2, pp.120-122.

[8] H. Prédrag, "Charge pumping characteristics of virgin and stressed lightly doped drain MOSFET", solid state electronics, Vol. 38, N°4, 1995, pp.891-904.

[9] J.L Autran., F. Seigneur, J. Delmas, C. Plossu and B. Balland, "Caractérisation des états d'interface dans des transistors MOS submicroniques par différentes techniques de pompage de charge", J. phys, octobre 1993, pp. 1947.