High Performance 8-Bit Mux Based Multiplier Design Using Mos Current Mode Logic

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Abstract

This paper presents a high performance 8x8 bit mux-based multiplier using MOS Current Mode Logic (MCML). A small library of MCML logic gates consisting of NAND/AND, 2 to 1 MUX and full adder are designed and optimized for low power and high-speed operation. Also a 4:1 MUX is designed which is one of the most essential component of this multiplier. Using these gates, a mux-based 8 bit MCML multiplier is designed and tested for 2 different supply currents, in a UMC 0.18 µm CMOS technology and VDD of 1.8V. According to our simulations, the highest current circuit works at 1 GHz and consumes 16 mW, while the lowest power operates at 550 MHz and consumes 10 mW. The circuits are either consumes less power or operates up to a higher frequency compared to equivalent circuits in the literature. One of the most important advantages of this circuit is the absence of the power supply current spikes which makes the circuit very suitable for mixed mode designs.

1. Introduction

An analog friendly digital circuit style that seems to be promising in reducing both the power consumption and the delay is MOS Current Mode Logic (MCML). While bipolar CML, a derivative of emitter coupled logic (ECL), has been used for years in high performance applications, it has become less desirable over time due to its high static power consumption and reliance on bipolar processing [1]. MCML is preferred for mixed analogue-digital signal environments in order to reduce the digital inference between the analogue and digital blocks. MCML architectures provide higher immunity to supply noise due to their differential structure, lower cross talk due to the reduced output voltage swing and lower noise generated due to the constant current flowing through the supply rails. The constant current used in MCML is the reason for constant power consumption, which is independent of the frequency of operation or gate activity. The power consumption is independent from the frequency because the two branches are driven symmetrically and in opposition of phase [2].

In digital signal processor implementation like standard digital signal processors and ASIC digital signal processors, the multiplier is used as fundamental building block. The performance of different signal processing algorithms like frequency domain filtering (FIR and IIR), frequency-time transformations (FFT), correlation etc depend on performance of multiplier implementation. In most real-time DSP processing task, the multiplier block must operate at high speed, consuming less layout area and low power [3]. In the literature, there are some methods to get a high performance multiplier such as Booth encoding and Wallace tree [4]. But in this paper, we present a mux-based 8-bit multiplier circuit by using MCML, designed and simulated in a 0.18 µm CMOS process.

2. MCML Gate Library

Our library of MCML gates consists of NAND/AND, 2 to 1 MUX, full adder (Fig. 1 and Fig. 3) and 4 to 1 MUX (Fig. 4). We optimized our MCML gates for low power and high speed operation. The transistor sizes were chosen to give a maximum dc voltage gain of 2. Our design optimization results are given in Table 1.

Table 1. The Optimization Results of the Design Parameters

Parameter Name	*Value*
Supply voltage (V_{DD})	1.8V
Voltage Swing (ΔV)	400mV
Biasing Currents and Biasing voltages	30µA for V_{RFN}=0.7V and V_{RFP}=0.4V 20µA for V_{RFN}=0.65V and V_{RFP}=0.65V
PMOS Load Transistor Sizes	W=0.55µm L=0.24µm
NMOS Current Source Transistor Sizes	W=1.6µm L=0.5µm
Differential Pair Transistor Sizes	W=1.0µm L=0.18µm (2-input gates) W=1.2µm L=0.18µm (3-input gates)

The MCML full adder which is the most important component of this multiplier shown in Fig. 1 and Fig. 2 is based on the design proposed by Brauer and Leblebici [5]. In this circuit, the carry input of the sum circuit is connected to the lowest logic level to reduce the input load of the carry signal. This MCML full adder consists of 24 transistors. However a CMOS full adder consists of 28 transistors and 76 full adders are used in this 8 bit multiplier.

Also a 4:1 mux which is the other most essential component of this mux-based multiplier shown in Fig. 3 is designed by using MCML. This multiplexer consumes very low power at high frequencies since it only needs one power supply. Also this MCML 4:1 mux consists of 17 transistors. However a CMOS 4:1 mux consists of 42 transistors and twenty - eight 4:1 muxes are used in this 8 bit multiplier.

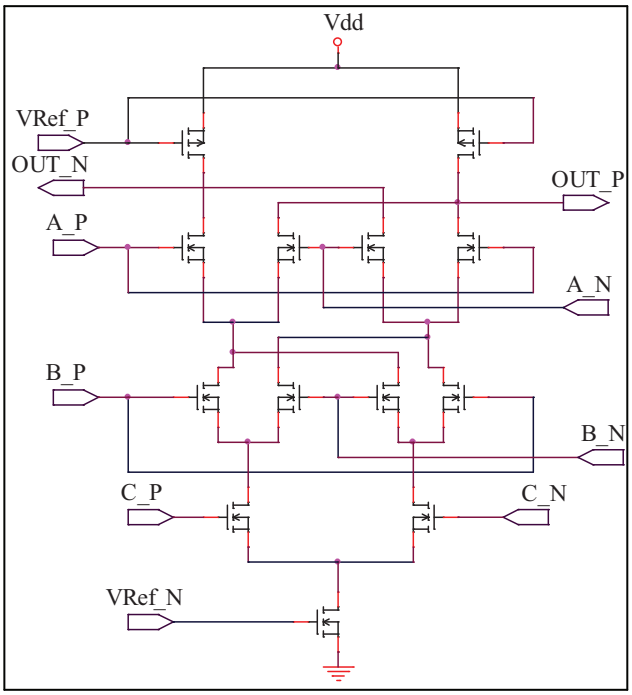

Fig. 1. The circuit diagram of 3 input XOR (SUM) gate

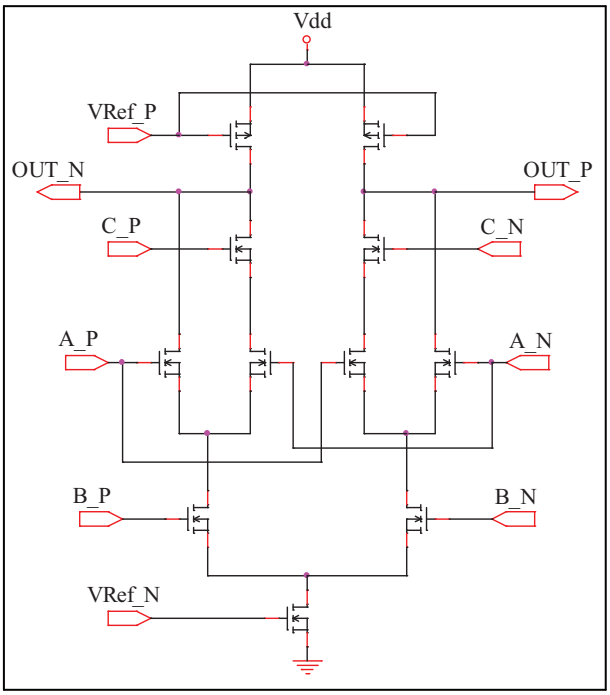

Fig. 2. The circuit diagram of majority function (CARRY) gate

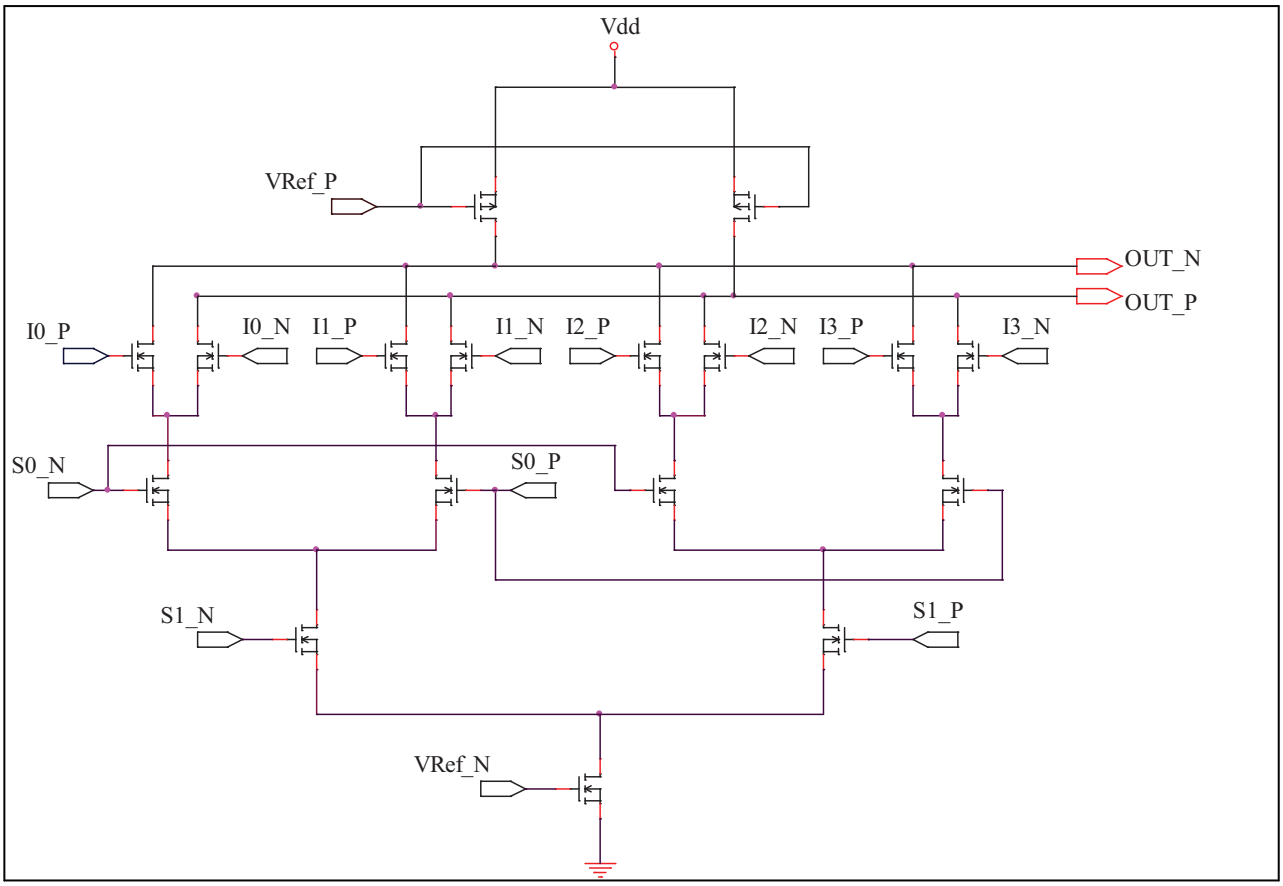

Fig. 3. The circuit diagram of 4 to 1 mux.

The gates are simulated for different power supply currents (different reference voltages) by HSpice to estimate the performance. The results are shown in Table 2.

Table 2. The Optimization Results of the Design Parameters

GATES	*Delays for different bias currents (ps)*	
	30 μA	*20 μA*
AND2	25	34
MUX2	35	50
XOR3 (Sum)	105	160
Majority (Carry)	120	185
MUX4	160	240

3. Proposed Multiplier Archiecture

In this paper, a new multiplication algorithm proposed by Pekmestzi [6] is used. In this algorithm at each step, one bit of the multiplier and one bit of the multiplicand are processed. So,the algorithm is symmetric; this means that multiplier and multiplicand can be interchanged. According to the proposed algorithm, the sum of the two operands, progressively computed, is a useful quantity that is used in the computation of certain partial products. This quantity is computed one bit at each step of the algorithm and is used in the next step, in case it is necessary. The paralel implementation of the proposed algorithm yields an iterative type array with almost equal number of cells as the five-counter multiplier. However, each cell of the proposed multiplier adds three bits instead of five bits of the five-counter multiplier. Consequently, a smaller circuit and faster addition of the partial products must be expected. Compared to the implementations based on the Modified Booth's algorithm, this require the same amount of circuitry but yields faster multiplication time.

The partial products that correspond to the right-boundary MUX are added in the first row of cells of Fig. 4. The partial products that are produced by the neighboring MUX are added in the second row of cells of the array of Fig. 4 and so on. Generally, the terms $Z_j$and 2^j and x_jy_j are added at the *j*th diagonal column cells of this array.

The array is composed of two types of cells. The first type of cells includes a 4 × 1 multiplexer and a Full-Adder and is shown in Fig. 5a. Input bits x_j and y_j are broadcast to $n - 1 - i$ cells of first type at the *i*th horizontal row of the array. The input bits x_j and y_j are broadcast to $j + 1$ diagonally placed cells of the array. The *j*th diagonal row of cells consists of *j* first type cells and one of second type cell. In total, $n(n-1)/2$ first type cells and *n* second type cells are required.

The second type cell, shown in Fig. 5b, includes two distinct circuits, each one of which performs a different job. The first circuit is a Full-Adder that produces at the new bits $s_j = s_i$ and $cj+1$. In all second type cells, indices *i* and *j* can be interchanged because they participate in horizontal and diagonal row of cells of the same order. Bits s_i along with x_j and y_j are broadcast to all first type cells of the *i*th row of the array. Bits c_j+1 are propagated to the next second type cells (for the progressive formation of the terms *Sj*).The second circuit of the second type cells completes the addition of the term *Zj* by summing the last bit of this term, equal to $x_j\, y_j\, c_j$, while at the same time it generates the term $x_j\, y_j$, which is required in the computation of the product. Finally, small complexity two-bit carry-select adders (CSLA) permit the addition of the outputs of the right boundary cells yielding high-speed operation. A CSLA performs two addition in paralel, one assuming a carry-in of zero, other a carry-in of one. A 2 bit CSLA consists of three 2 to 1 muxes and 4 full adders. As can be seen in Fig. 4, the total multiplier circuit consists of $\{\frac{n(n-1)}{2}+2n+1\}$ Full-Adders, $n(n\text{-}1)/2$ multiplexers, $2n$ AND gates and $(n-2)$ two-bit carry-select (CSLA) adders. For a 8 bit multiplier, *n* is equal eight.

Notice that the proposed multiplier scheme of Fig. 4 yields almost the same circuit complexity with the arrays based on the Modified Booth's algorithm, while it requires a considerably smaller number of gates or transistors compared to the other arrays. Seven connection input and output lines between cells are needed, compared to eight of the Modified Booth's algorithm, seven of a five-counter cell and four of an iterative multiplier array. Also by using MCML, it is possible to design very fast and low power ful adders and 4 to 1 muxes (Fig. 1,2 and 3). However, the interconnection lines do not consume more chip area, because they are realized using the metal interconnection layers of the VLSI technology. The multiplication time of the proposed scheme is equal to $T = (n+1)\,\tau\,(FA)$, where $\tau\,(FA)$ is the delay time of a Full-Adder [6].

4. The Simulation Results

The multiplier simulations are performed using HSpice. The circuit is tested for two different biasing currents. The results are shown in Table 3. The maximum operation frequency increases if a higher bias current is used in the expense of higher power consumption as expected.

Table 3 shows the worst case delay, maximum operating frequency and power consumption of our mux-based 8 bit MCML multiplier for different bias currents. The new multiplier is compared with the multipliers (same technology) in the literature in Table 4.

Table 3. The Performance of the Proposed 8-Bit Multiplier

V_{RFN} *[V]*	V_{RFP} *[V]*	I_{DD} *[mA]*	*Delay [ns]*	*Frequency [MHz]*	*Power [mW]*
0.7	0.4	8.88	0.95	1000	16
0.65	0.65	5.55	1.64	550	10

Table 4. The Comparison of the 8-Bit Multipliers

Ref.	*Technology*	*Delay [ns]*	*Maximum Frequency [MHz]*	*Power [mW]*
[7]	0.18μm MCML	3.8	4.76 (Pipelined)	260
[8]	0.18μm CMOS	0.793	1100	22.5
[9]	0.18μm CMOS	3.35		0.179 (@50 MHz)
Our design	**0.18μm MCML**	**0.95 1.64**	**1000 550**	**16 10**

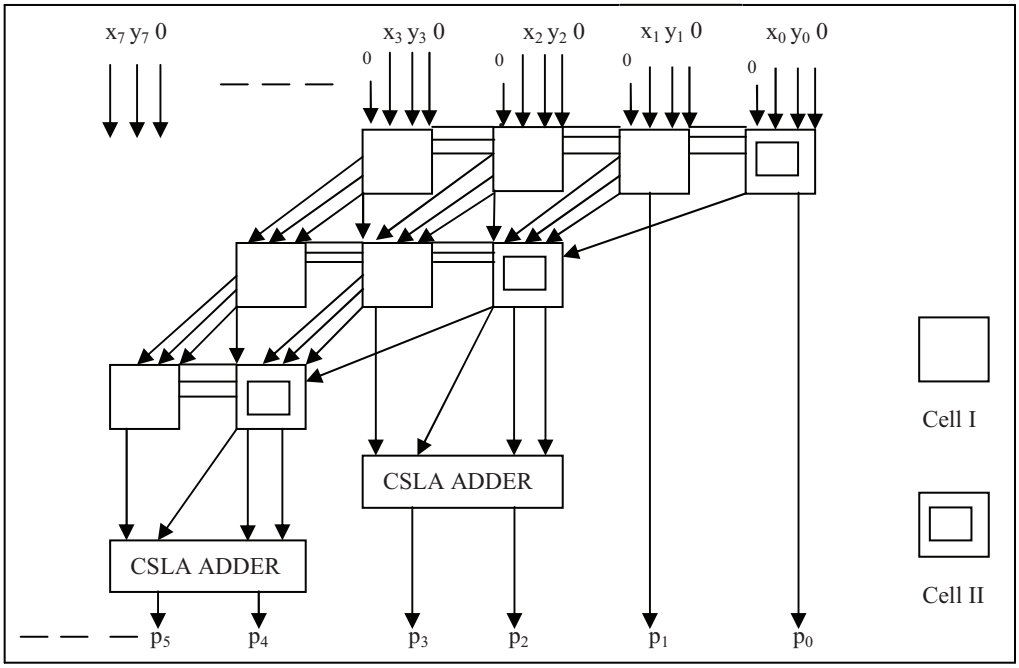

Fig. 4. The proposed 8 bit multiplexer based array multiplier [6]

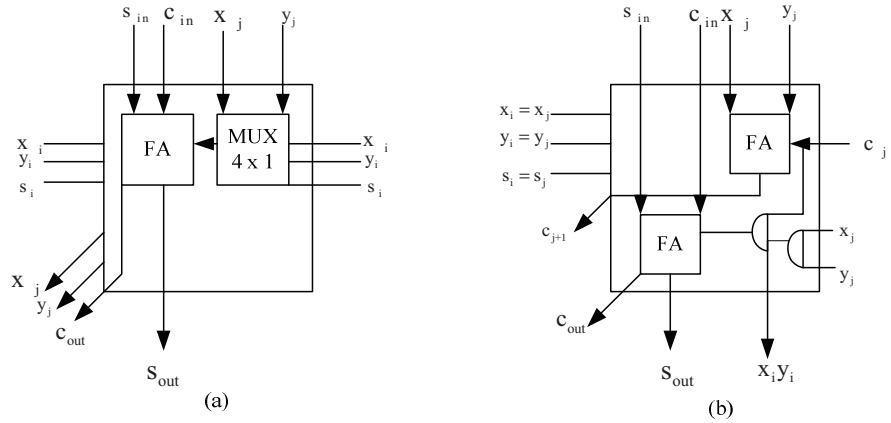

Fig. 5. (a) First type cell (CELL I) (b) Second type cell (CELL II) [6].

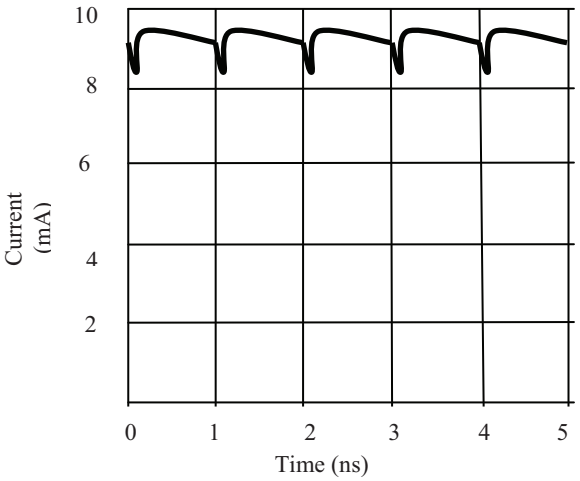

Fig. 6. Supply current waveform at maximum frequency

5. Conclusions

We designed an 8 bit high performance multiplier by using MCML. In this multiplier, multiplexer-based algorithm is used to get high performance. All of the circuits are designed using MCML gate structure. By using MCML, only 17 transistors are used in 4 to 1 mux compared to 42 transistors in equivalent CMOS circuit. We used multiplexer-based parallel multiplier structure proposed by Pekmestzi [6] for speed and power improvement. In this architecture, fewer gates are needed compared to Modified-Booth's algorithm. Pekmestzi used 2 bit Carry Look Ahead (CLA) adders for final addition. But by using MCML, implementation of 2 bit CSLA needs fewer transistors and consumes less power than 2 bit CLA. So we used 2 bit CSLAs for final addition.

According to our simulations, the multiplier may be operated either at maximum operation frequency of 1 GHz which consumes 16mW or at a lower speed of 550 MHz,

minimizing the power consumption down to 10 mW, by just reducing the bias current. The power supply current spikes (Fig. 6) are only 9 per cent of the nominal current and the multiplier consists of 2510 transistors. The Table 4. shows that our proposed mux-based 8 bit MCML multiplier is better than the other multipliers in the literature in 0.18µm technology, either in terms of maximum operation frequency or power consumption.

6. References

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