Interline Power Flow Controller Based on Multi Output Sparse Matrix Converter

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Abstract

A novel structure is proposed for Interline Power Flow Controller based on Multi Output Sparse Matrix Converter. The Multi Output Sparse Matrix Converter is first considered in this paper and has been used as IPFC instead of multiple inverters. The conventional IPFC contains a bulky capacitor in its structure that increases volume and cost of the system and since it has limited lifetime consequently it reduces reliability and life time of IPFC, but the new IPFC does not have those problems.

Necessary information needed to simulate Multi Output Sparse Matrix Converter is presented. The new IPFC system is modeled and sliding mode controller is used to control line current in order to control line power. Sliding mode control is selected because of its robustness and fast response time. Sliding mode control is implemented in an improved manner. Finally, proposed IPFC is simulated in PSCAD/EMTDC software and output waveforms are compared with reference values.

1. Introduction

In most of the AC systems the load sharing is governed by line impedances and most of the time it does not lead to full utilization of transmission line capacity, or it may result in over loads in some cases [1].

The FACTS is a power electronic based, real time computer controlled technology that provides the needed corrections of transmission functionality in order to efficiently utilize existing transmission systems and therefore, minimize the gap between the stability and the thermal level [2].

FACTS devices are an attractive alternative for increasing the transmission capability of existing transmission lines [3]. They can be used to control steady-state as well as dynamic/transient performance of the power system [4].

Interline Power Flow Controller (IPFC) is one of versatile FACTS devices. Conventionally, it consists of a set of converters that are connected in series with different transmission lines [5] , and sometimes one inverter is connected in shunt. DC links of all inverters are parallel. IPFC controls complex power of corresponding lines.

An IPFC can also be used to equalize active/reactive power between transmission lines, and transfer power from overloaded lines to under-loaded lines [4].

In conventional IPFCs there is a high capacity electrolytic capacitor in their DC link. This DC Link capacitor limits the life time of the converter thereby affecting its overall performance in addition to greatly increasing the weight, price and volume of the converter [6, 7, 8].

With the goal of higher power density and reliability, it is hence obvious to consider the Matrix Converter concepts that achieve three-phase AC/AC conversion without any intermediate energy storage element. [9].

Among many types of matrix converters, Sparse Matrix Converters have lower number of switches and can have more than one output, so they can be used as IPFC.

This construct, using Multi Output Sparse Matrix Converter as IPFC has not been reported any where so far.

In [10] and [8] conventional matrix converter is used as unified power flow controller (UPFC) and [7] proposed use of sparse matrix converter as UPFC, all of them used sliding mode control method to control transmission line power flow. They used sliding mode control both at input and output of matrix converters.

In this paper, sliding mode control is selected to control each transmission line power flow, because it is simple to implement, robust to parameter variation and has fast response time [10]. Sliding mode control guarantees the choice of the most appropriate control actions [11].

In contrast to [7] , [8] and [10], sliding mode control will not apply to input stage of Multi Output Sparse Matrix Converter and it will be controlled to provide fixed unity power at input of converter factor so that maximum output voltage will be provided for converter.

In the following sections of this paper, the new IPFC power circuit will be shown and explained, Multi Output Sparse Matrix Converter will be introduced and necessary information for its simulation will be given, the new IPFC system will be modeled and suitable controller will be introduced, and finally the simulation results of the new IPFC system in PSCAD/EMTDC [12] software will be presented.

2. New IPFC Power Circuit

Power circuit of the new IPFC is shown in Fig. 1. The IPFC system is implemented on two transmission lines of a bus, in order to control their power flow [13]. In this circuit, the conventional back to back VSCs have been replaced by Multi Output Sparse Matrix Converter (MOSMC). Low pass RLC filter at its input is dedicated to cancel input current high frequency harmonics.

The MOSMC controls the complex power of each transmission line by injection of a proper series voltage with that line. A step down transformer is dedicated to feed the MOSMC input and other transformers at each output to isolate the MOSMC and the transmission line.

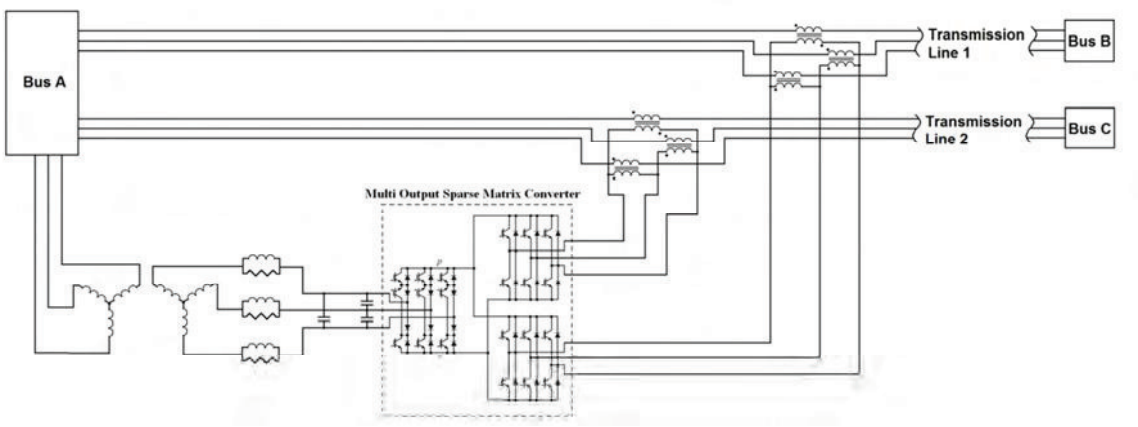

Fig. 1. New IPFC power circuit

3. Multi Output Sparse Matrix Converter

Sparse Matrix Converter (SMC) has a DC link in its structure which allows use of it as single-input-multi-output matrix converter. This is called Multi Output Sparse Matrix Converter (MOSMC). The input stage supports DC link voltage as well as providing desired phase displacement at its three phase side. Each of the output stages produces desired voltage space vector by means of DC link voltage.

Some essential information needed for simulation of MOSMC are presented. For more detail about SMC (and consequently about MOSMC) refer to [14].

A. Switching of input stage

The switching pattern of MOSMC is shown in Fig. 2. Switching period is T, each period is divided into two half periods that are mirrored of each other.

Rectifier	tr1			tr2			tr2			tr1		
Inverter 1	f1	f2	f3	f4	f5	f6	f6	f5	f4	f3	f2	f1
Inverter 2	h1	h2	h3	h4	h5	h6	h6	h5	h4	h3	h2	h1
	T/2						T/2					

Fig. 2. Switching pattern of MOSMC

There are two parts in each half period, named as tr1 and tr2. The input stage connects a pair of input phases to the DC link in tr1 interval and two other phases in tr2 interval, according to table 1.

Table 1. Switching order of MOSMC input stage

$\phi_1+\phi$	k_i	DC link			
		Positive		Negative	
		tr1	tr2	tr1	tr2
(0,30)	1	a	a	c	b
(30,90)	2	b	a	c	c
(90,150)	3	b	b	a	c
(150,210)	4	c	b	a	a
(210,270)	5	c	c	b	a
(270,330)	6	a	c	b	b
(330,360)	1	a	a	a	b

The letters a, b and c denote the input phases of the MOSMC. The measured voltage space vector of the input stage of the MOSMC is $u_1\angle\phi_1$ and desired phase displacement between input voltage and current is ϕ , and k_i is the sector number of input current. α is defined as:

$$\alpha = \phi_1 + \phi + 90 - 60k_i \quad (1)$$

So tr1 and tr2 can be calculated as:

$$tr1 = \frac{\sin(\alpha)}{\cos(\alpha-30)}, tr2 = 1 - tr1 \quad (2)$$

The average voltage of DC link in a period can be calculated as:

$$\bar{u}_{DC} = \frac{3}{2}u_1\frac{\cos(\phi)}{\cos(\alpha-30)} \quad (3)$$

This voltage is used at the output stage switching.

B. Switching of output stages

Switching methods of output stages are identical except that the voltages may be different, so inverter 1 is considered in the following. . There are six parts in each half period of switching, named as f1, f2, f3, f4, f5 and f6. Parts f3 and f4 are zero parts, that is, in those intervals all of output phases are connected to negative or positive bus of the DC link. Space vector of output voltage is assumed to be $u_o\angle\phi_o$. Switching order of output stages can be found in table 2.

Table 2. Switching order of MOSMC output stage

ϕ_o	k_o	A		B		C	
		f1,f6	f2,f5	f1,f6	f2,f5	f1,f6	f2,f5
(0,60)	1	p	p	n	p	n	n
(60,120)	2	p	n	p	p	n	n
(120,180)	3	n	n	p	p	n	p
(180,240)	4	n	n	p	n	p	p
(240,300)	5	n	p	n	n	p	p
(300,360)	6	p	p	n	n	p	n

The letters p and n denote positive and negative bus of MOSMC DC link, respectively and A , B and C denote the output phases of the MOSMC, k_o is the output voltage space vector, sector number and ϕ_o is phase angle of output voltage space vector. The angle β is defined as:

$$\beta = \phi_2 - 60k_o + 60 \quad (4)$$

Durations of output switching states are calculated as:

$$f1 = tr1\sqrt{3}\frac{u_o}{\bar{u}}\cos(\beta + 30) \quad (5)$$

$$f2 = tr1\sqrt{3}\frac{u_o}{\bar{u}}\sin(\beta) \quad (6)$$

$$f5 = tr2\sqrt{3}\frac{u_o}{\bar{u}}\cos(\beta + 30) \quad (7)$$

$$f6 = tr2\sqrt{3}\frac{u_o}{\bar{u}}\sin(\beta) \quad (8)$$

4. System Modeling and Controller Design

Considering any output of MOSMC which is series with a transmission line, its single phase equivalent circuit is shown in Fig. 3.

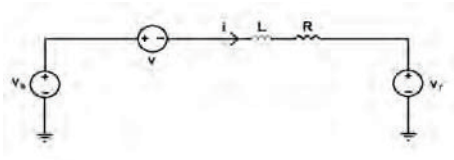

Fig. 3. Simplified single phase equivalent circuit of a series compensated line

In Fig. 3, v is the voltage produced by MOSMC, v_s is sending end voltage, v_r is receiving end voltage, R is the transmission line resistance and L is line inductance. All symbols represent the instantaneous values of quantities.

The main purpose of IPFC control is to force each line complex power track pre-determined values. For simplification of analysis and control, synchronous rotating reference frame and space vectors are used and quantities are represented by their d and q components. Reference values of line current components can be obtained by (9) and (10) [15]:

$$i_{dref} = \frac{2(P_{ref}v_{rd} + Q_{ref}v_{rq})}{3({v_{rd}}^2 + {v_{rq}}^2)} \quad (9)$$

$$i_{qref} = \frac{2(P_{ref}v_{rq} - Q_{ref}v_{rd})}{3({v_{rd}}^2 + {v_{rq}}^2)} \quad (10)$$

P_{ref} and Q_{ref} are reference values of each line receiving end active and reactive power respectively. So the problem is to control the line current.

The circuit equations of Fig. 3 with considering all phases, in d q coordinates are:

$$\frac{di_d}{dt} = \frac{1}{L}(v_{sd} - v_d - v_{rd} - Ri_d + Li_q\omega_0) \quad (11)$$

$$\frac{di_q}{dt} = \frac{1}{L}(v_{sq} - v_q - v_{rq} - Ri_q - Li_d\omega_0) \quad (12)$$

θ is Park transformation angle and ω_0 is the synchronous angular frequency of the network voltage and also time derivative of θ.

Sliding mode controllers are used to control each line current. Since the derivatives of transmission line currents are related to MOSMC output voltages and these voltages depend directly on the switches state, the two sliding surfaces (13) and (14) should depend directly on i_d and i_q current errors [7].

$$S_d = k_d(i_{dref} - i_d) \quad (13)$$

$$S_q = k_q(i_{qref} - i_q) \quad (14)$$

In sliding mode control, to guarantee system stability, at each time instant (15) and (16) should be satisfied [7, 8, 10, 11, 16].

$$S_d\dot{S}_d < 0 \quad (15)$$

$$S_q\dot{S}_q < 0 \quad (16)$$

At each time instant (or switching period), at any output of MOSMC, S_d and S_q are applied to two three level hysteresis comparators and their result will be C_d and C_q with values 1 , 0, 1. So, there are nine states (3×3) [7, 8, 10]. At each state, the most suitable voltage should be selected to satisfy stability conditions, (15) and (16). Table 3 shows suitable voltage selection based on sliding surfaces states.

Table 3. Suitable voltage selection based on sliding surfaces states

C_d	-1	-1	-1	0	0	0	1	1	1
C_q	-1	0	1	-1	0	1	-1	0	1
v_d	$\frac{u_M}{\sqrt{2}}$	u_M	$\frac{u_M}{\sqrt{2}}$	0	0	0	$-\frac{u_M}{\sqrt{2}}$	$-u_M$	$-\frac{u_M}{\sqrt{2}}$
v_q	$\frac{u_M}{\sqrt{2}}$	0	$-\frac{u_M}{\sqrt{2}}$	u_M	0	$-u_M$	$\frac{u_M}{\sqrt{2}}$	0	$-\frac{u_M}{\sqrt{2}}$

u_M is maximum amplitude of series voltage. The values of table 3 are selected based on following discussion.

From (11) and (13), (18) can be calculated.

$$\dot{S}_d = -k_d\left[\frac{1}{L}(v_{sd} - v_d - v_{rd} - Ri_d + Li_q\omega_0)\right] = A + \frac{k_d}{L}v_d \quad (18)$$

And from (12) and (14) , (19) can be calculated.

$$\dot{S}_q = -k_q\left[\frac{1}{L}(v_{sq} - v_q - v_{rq} - Ri_q - Li_d\omega_0)\right] = B + \frac{k_q}{L}v_q \quad (19)$$

From stability conditions (15) and (16), we can write:

a) If $S_d < 0$, there should be $\dot{S}_d > 0$, or from (18) there should be $v_d + \frac{L}{k_d}A > 0$

b) If $S_d > 0$, there should be $\dot{S}_d < 0$, or from (18) there should be $v_d + \frac{L}{k_d}A < 0$

c) If $S_d = 0$, then, v_d should be zero.

Similar sentences can be written about S_q. The values listed in table 3 have been selected to satisfy above conditions.

From these stories we can conclude that to guarantee stability, controller must be able to make $\dot{S}_d$ and $\dot{S}_q$ become positive or negative by means of v_d and v_q. At any switching period, a voltage is selected according to table 3 to determine sign of $\dot{S}_d$ and $\dot{S}_q$.

If P_{ref} and Q_{ref} satisfy (20) and (21), then, signs of $\dot{S}_d$ and $\dot{S}_q$ are controllable by v_d and v_q.

$$\left|v_{sd} - v_{rd} - R\frac{2(P_{ref}v_{rd} + Q_{ref}v_{rq})}{3({v_{rd}}^2 + {v_{rq}}^2)} + L\omega_0\frac{2(P_{ref}v_{rq} - Q_{ref}v_{rd})}{3({v_{rd}}^2 + {v_{rq}}^2)}\right| < \frac{u_M}{\sqrt{2}} \quad (20)$$

$$\left|v_{sq} - v_{rq} - R\frac{2(P_{ref}v_{rq} - Q_{ref}v_{rd})}{3({v_{rd}}^2 + {v_{rq}}^2)} + L\omega_0\frac{2(P_{ref}v_{rd} + Q_{ref}v_{rq})}{3({v_{rd}}^2 + {v_{rq}}^2)}\right| < \frac{u_M}{\sqrt{2}} \quad (21)$$

In fact (20) and (21) specify stable operation region of each line of the IPFC. For each MOSMC output, v_d and v_q are converted to space vectors of output voltages through (22), and are used to modulate output stages of MOSMC.

$$u_o \angle \phi_o = e^{j\theta}(v_d + jv_q) \quad (22)$$

5. Results

Based on parameters values listed in appendix, the stable operation region of the IPFC based on (20) & (21) is shown in Fig. 4.

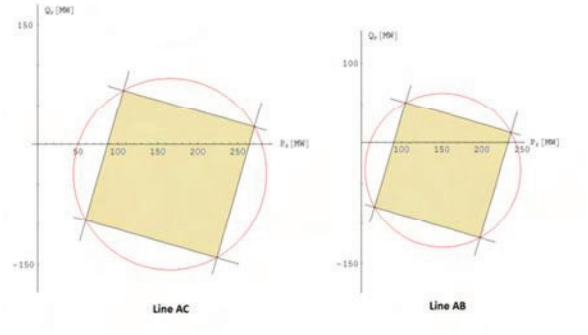

Fig. 4. Stable operation region of IPFC

The colored area is the stable operation region of IPFC. Inside of red circles are the absolute controllable regions offered by series voltages of each line. In this paper lowest controllable area reduction caused by sliding mode control is occurred compared to [7], [8] & [10]. This area reduction is due to nonparametric nature of sliding mode control method. The circuit shown in Fig. 1 is simulated in PSCAD\EMTDC software. The MOSMC switching frequency is 10 kHz, output coupling transformers are 30\20 kV, other parameter values are listed in appendix. Reference values for receiving end line powers are applied according to table 4.

Table 4. Reference values for receiving end line powers

Time (s)	Transmission line 1		Transmission line 2	
	P_{ref}	Q_{ref}	P_{ref}	Q_{ref}
(0,0.07)	90MW	0	90MW	0
(0.07,0.09)	230MW	0	90MW	0
(0.09,0.14)	230MW	0	260MW	0
(0.14,0.17)	230MW	0	220MW	0
(0.17,0.22)	190MW	0	220MW	0
(0.22,0.25)	190MW	-100MVAr	220MW	0
(0.25,0.3)	190MW	-100MVAr	220MW	-120MVAr

All reference values are passed through a $\frac{1}{1+sT_c}$ to avoid sudden variations. The response of simulated system to reference values of table 4 is shown in Fig. 4.

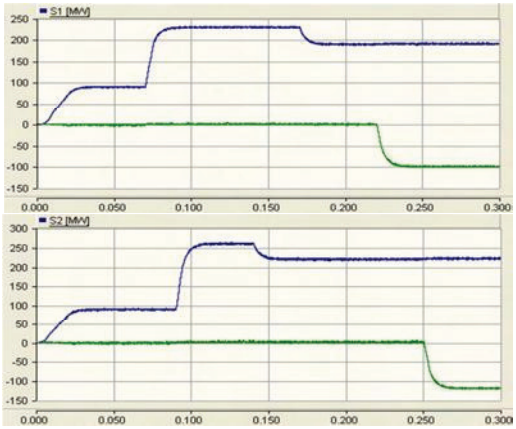

Fig. 4. Receiving end line 1 (S1) and line 2 (S2) power simulated curves, blue lines are active power and green lines are reactive power

It is seen that line powers have followed reference values with fast response and no interference between each line active and reactive powers and between different lines' powers.

Instantaneous power balance relation in MOSMC (with ideal switches) is:

$$P_{in} = P_{1o} + P_{2o} \quad (23)$$

In (23), P_{in} is power flowing into the input of MOSMC and, P_{1o} and P_{2o} are powers flowing out of outputs 1 and 2 of MOSMC.

Power rating of output parts 1 and 2 of MOSMC called P_{1omax} and P_{2omax} are determined according to which applications IPFC is used for, such as steady state power flow and voltage control, transient stability margin enhancement, oscillation damping, etc.

Power rating of input part of MOSMC, P_{inmax}, is $Max\{|P_{1o} + P_{2o}|\}$ which is determined according to power system topology and parameters value, and location of IPFC in power system and also application of IPFC in power system.

Here, power rating of MOSMC is evaluated in Fig. 1 based on parameters values listed in appendix while IPFC is used for steady state power flow control.

For each transmission line in Fig. 1, based on circuit analysis, there are ($P_o = P_{1o}, P_{2o}$):

$$P_O = \frac{3}{2(R^2 + L{\omega_0}^2)}(-Rv_d{}^2 + v_d\left(R(v_{sd} - v_{rd}) + L\omega_0(v_{sq} - v_{rq})\right) - Rv_q{}^2 + v_d\left(R(v_{sq} - v_{rq}) + L\omega_0(v_{sd} - v_{rd})\right)) \quad (24)$$

Maximum series voltage is v_m (${v_{rd}}^2 + {v_{rq}}^2 < v_m$), so, absolute maximum value of (24), or rating of each output terminal of MOSMC can be found as:

$P_{1omax} = Max\{|P_{1o}|\} = 14.7MW$, $P_{2omax} = Max\{|P_{2o}|\} = 16.4MW$ These are occurred by $v_d = -16281v$, $v_q = -1267v$ for line AB, and $v_d = -16254v$, $v_q = -1577v$ for line AC. Rating of input stage in this case is $P_{inmax} = Max\{|P_{1o} + P_{2o}|\} = 31.1MW$.

In the above case, the current drawn by MOSMC from bus A together with voltage of bus A is shown in Fig. 5.

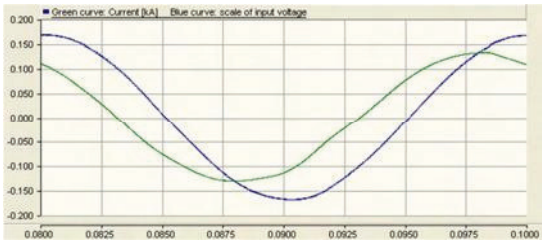

Fig. 5. Phase voltage of bus A (blue curve) and current drawn by MOSMC from bus A (green curve).

In Fig. 5 power factor is 0.83 leading at full loading of MOSMC.

6. Conclusion

A new IPFC system based on Multi Output Sparse Matrix Converter has been proposed. The system has been modeled and sliding mode controller has been used and the whole system has been simulated in PSCAD/EMTDC software. Sliding mode control was selected mainly to ensure system robustness to parameter variation, and no system parameters were used in controller design. As a consequence, MOSMC outputs produced zero or maximum voltage and no adjusted voltages were used. This is nature of sliding mode control. Linear decoupled controllers can be used to control this system and they will make MOSMC produce best voltage to minimize the line current ripple. But their proper performances are dependent on the knowledge of exact values of system parameters.

Input stage of Multi Output Sparse Matrix Converter was controlled with constant unity power factor to provide maximum DC link voltage. The sliding mode controllers responded fast to reference values changes, there was no interference between d and q components and between different line currents. Stable operating region of IPFC with sliding mode control was derived. This control method was implemented in a way that lower controllable area reduction was occurred compared to other papers.

7. Appendix

Buses A , B and C are assumed to be ideal three phase voltage sources with 230 kV rms L-L. Phase angle of bus A is 0 degree and phase angles of buses B and C decreases uniformly from 0 to -8 and -7 degrees, respectively.

Step down transformer is 230/20 kV rms L-L with negligible impedance.

The MOSMC input filter parameters are as follow: inductor is 2mh , resistor is 50 ohms and capacitors are 60uf.

Transmission line 1 equivalent inductance is 0.15H and line 2 is 0.12H and equivalent resistances are 7 and 6 ohms respectively.

8. References

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