LOW-POWER CMOS BULK-DRIVEN WEAK-INVERSION ACCURATE CURRENT-MODE MULTIPLIER/DIVIDER CIRCUITS

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ABSTRACT

Two current mode multiplier/divider circuits using bulk-driven MOS transistors will be presented. Because of the operation of MOS transistors in utilization of the bulk as the fourth active terminal reduces the circuit complexity and, in consequence, the silicon occupied area for the required function. The output currents of both versions of bulk-driven circuits are independent on the process parameters, so independent on temperature.

I. INTRODUCTION

Computational circuits and particularly multiplier/divider circuits are important building blocks for telecommunication applications, medical equipments, hearing devices and disk drives [1] - [5].

In the bipolar technology, the multiplication function could be easily obtained from the logarithmical characteristic [6] of the bipolar transistor. Important errors still remain because of the nonzero values of the base currents, especially for pnp transistors and of the temperature dependence of the bipolar transistor parameters (the thermal voltage is linear increasing with temperature and the saturation current has an exponential dependence on temperature).

Due to the rapid development of CMOS VLSI technology, many analog signal processing functions can be achieved by employing the square-law model of MOS transistors [7] – [15]. Analog circuits based on the square-algebraic identity can be easily realized from the well-known square-law model of the MOS transistors in the saturation region. Based on this principle, several basic building blocks, such as multipliers, active resistors and transconductors have been developed [7] – [15].

In order to respond to the low-power requirements of the newest CMOS designs, the subthreshold operation of the MOS transistor is an interesting choice. Based on the logarithmical law of a MOS transistor in weak inversion, the implementation of a CMOS current-mode multiplier/divider becomes very simple (even with respect to the bipolar version) and, in consequence, with the subthreshold region, these computational circuits allow obtaining a very small current consumption, responding to the low-power requirements of newer computational circuit designs. The result of a smaller silicon area consumption, making the circuit compatible with low-power VLSI designs.

II. THEORETICAL ANALYSIS

CURRENT MULTIPLIER/DIVIDER USING BULK-DRIVEN MOS TRANSISTORS

The double drive of the MOS transistor (on gate and on bulk) allows the reduction of the complexity for the circuits that realize mathematical functions. Unfortunately, the possibility of implementation in silicon is limited to CMOS technologies with independent wells.

The first proposed current multiplier/divider using bulk-driven MOS transistors is presented in Figure 1. Considering a weak inversion operation of all the transistors from Figure 1, the expressions of I_1 and I_2 currents will be:

$$I_{1,2} = I_{D0} \exp\left(\frac{V_{GS_{1,2}} + (n-1)V_{BS_{1,2}}}{nV_t}\right) \qquad (1)$$

where I_{D0} is a parameter with the following expression, resulted from the continuity between the strong inversion and weak inversion regions:

$$I_{D0} = \frac{2\mu_n C_{ox}(nV_t)^2}{e^2} \qquad (2)$$

$V_{GS_{1,2}}$ and $V_{BS_{1,2}}$ are, respectively, the gate-source and bulk-source voltages of the MOS transistor.

C_{ox} is the oxide specific capacitance and $V_t = KT/q$ is the thermal voltage. So:

$$\frac{I_1}{I_2}=\exp\left(\frac{V_{X_2}-V_{Y_2}}{nV_t}\right)\exp\left[\frac{n-1}{nV_t}\left(V_{X_1}-V_{Y_1}\right)\right] \quad (3)$$

$$\frac{I_{X_1}}{I_{Y_1}}=\exp\left[\frac{n-1}{nV_t}\left(V_{BS_3}-V_{BS_4}\right)\right] \quad (4)$$

Because $V_{GS_3}=V_{GS_4}$ it results:

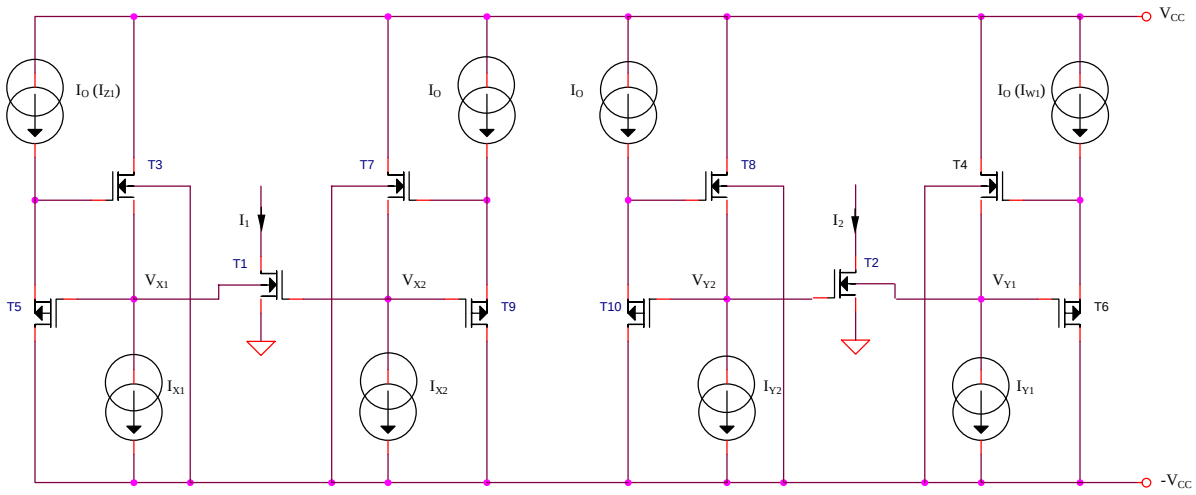

Figure 1: Current multiplier/divider using bulk-driven MOS transistors

Similarly, because $V_{GS_7}=V_{GS_8}$:

$$\frac{I_{X_2}}{I_{Y_2}}=\exp\left[\frac{n-1}{nV_t}\left(V_{BS_7}-V_{BS_8}\right)\right] \quad (5)$$

Knowing that:

$$V_{X_1}-V_{Y_1}=V_{BS_4}-V_{BS_3} \quad (6)$$

and:

$$V_{X_2}-V_{Y_2}=V_{BS_8}-V_{BS_7} \quad (7)$$

and using (2) and (3), the relations between the currents from Figure 1 could be written as:

$$\frac{I_1}{I_2}=\frac{I_{Y_1}}{I_{X_1}}\left(\frac{I_{Y_2}}{I_{X_2}}\right)^{\frac{1}{n-1}} \quad (8)$$

A generalization of relation (8) for different values of current sources I_0 (I_{Z_1}, I_{W_1} and I_{Z_2}, I_{W_2}, respectively) allow obtaining a more complex relation with currents as variables:

$$\frac{I_1}{I_2}=\frac{I_{Y_1}}{I_{X_1}}\frac{I_{Z_1}}{I_{W_1}}\left(\frac{I_{Y_2}}{I_{X_2}}\frac{I_{Z_2}}{I_{W_2}}\right)^{\frac{1}{n-1}} \quad (9)$$

CURRENT-MODE MULTIPLIER/DIVIDER CIRCUIT USING A BULK-DRIVEN ACTIVE-LOAD DIFFERENTIAL AMPLIFIER

Another possible implementation of a current-mode multiplier/divider is referred to a bulk-driven active- load differential amplifier from Figure 2.

Considering a weak inversion operation of all the transistors from Figure 2, the ratio of I_1 and I_2 currents will be:

$$\frac{I_1}{I_2}=\exp\left(\frac{V_{GS_1}-V_{GS_2}}{nV_t}\right) \quad (10)$$

For the active-load differential amplifier it is possible to write:

$$1=\exp\left(\frac{V_{GS_1}-V_{GS_2}}{nV_t}\right)\times$$

$$\times \exp\left[\frac{n-1}{nV_t}\left(V_{BS_1}-V_{BS_2}\right)\right] \quad (11)$$

From the two previous relations it results:

$$\frac{I_1}{I_2}=\exp\left[\frac{1-n}{nV_t}\left(V_{X_1}-V_{X_2}\right)\right] \quad (12)$$

Similarly, the ratios of I_{X_1}, I_{X_2} and I_{Y_1}, I_{Y_2} are, respectively:

$$\frac{I_{X_1}}{I_{X_2}}=\exp\left(\frac{V_{GS_3}-V_{GS_4}}{nV_t}\right) \quad (13)$$

and:

$$\frac{I_{Y_1}}{I_{Y_2}}=\exp\left(\frac{V_{GS_3}-V_{GS_4}}{nV_t}\right)\times \times\exp\left[\frac{n-1}{nV_t}\left(V_{BS_3}-V_{BS_4}\right)\right] \quad (14)$$

So, it results:

$$V_{BS_3}-V_{BS_4}=\frac{nV_t}{n-1}\ln\left(\frac{I_{Y_1}}{I_{Y_2}}\frac{I_{X_2}}{I_{X_1}}\right) \quad (15)$$

From (12) and (15), using that $V_{X_1}-V_{X_2}=V_{BS_4}-V_{BS_3}$, the relation between the currents from Figure 2 will be:

$$\frac{I_1}{I_2}=\frac{I_{Y_1}}{I_{Y_2}}\frac{I_{X_2}}{I_{X_1}} \quad (16)$$

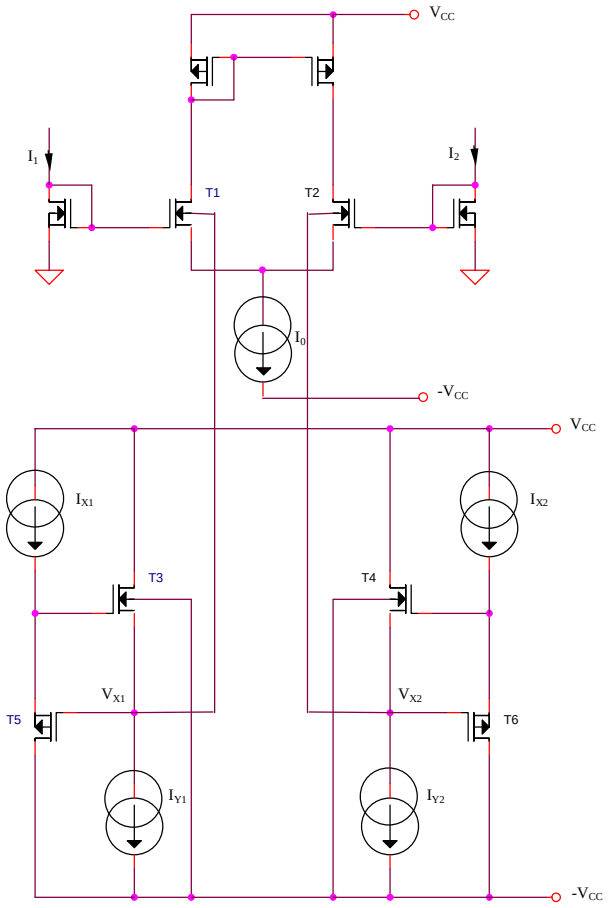

Figure 2: Current-mode multiplier/divider using bulk-driven active-load differential amplifier

III. CONCLUSIONS

Two CMOS multiplier/divider circuits were presented. The reducing of the circuit complexities and, in consequence, of the silicon occupied areas is achieved by using the bulk as the fourth active terminal of the MOS transistors, making these computational circuits compatible with the latest VLSI designs. The proposed multiplier/divider circuits respond, also, to the low-power requirements due to the subthreshold operation of MOS transistors. The circuits' output currents are independent on the process parameters, so independent on temperature variations.

REFERENCES

1. R. Harjani, A Low-Power CMOS VGA for 50 Mb/s Disk Drive Read Channels, IEEE Transactions on Circuits and Systems II, Analog Digital Signal Processing, pp. 370-376, 1995.
2. A. Motamed, C. Hwang, M. Ismail, A Low-Voltage Low-Power Wide-Range CMOS Variable Gain Amplifier, IEEE Transactions on Circuits and Systems II, Analog Digital Signal Processing, pp. 800-811, 1998.
3. P.C. Huang, L.Y. Chiou, C.K. Wang, A 3.3V CMOS Wideband Exponential Control Variable gain Amplifier, Proceedings 1998 of IEEE International Symposium on Circuits and Systems, Volume I, pp. 285-288, 1998.
4. C.H. Lin, T.C. Pimenta, M. Ismail, A Low Voltage CMOS Exponential Function Circuit for AGP Applications, Proceedings of 11th Brazilian Symposium on Integrated Circuit Design, pp. 195-198, 1998.
5. W.A. Serdijn, A.C. Van der Woerd, J. Davidse, A.H.M. Van Roermund, Low-Voltage Low-Power Fullw-Integratable Automatic Gain Controls for Hearing Instruments, IEEE Journal of Solid State Circuits, pp. 943-946, 1994.
6. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.
7. K. Bult, H. Wallinga, A CMOS Four-Quadrant Analog Multiplier IEEE Journal of Solid-State Circuits, vol. SC-21, pp. 430-435, 1986.
8. K. Bult, H. Wallinga, A Class of Analog CMOS Circuits Based on the Square-Law Characteristics of an MOS Transistor in Saturation, IEEE Journal of Solid-State Circuits, vol. SC-22, pp. 357-364, 1987.
9. E. Seevinck, R.F. Wassenaar, A Versatile CMOS Linear Transconductor/Square-Law Function Circuit, IEEE Journal of Solid-State Circuits, vol. SC-22, pp. 366-377, 1987.
10. F. Pena-Finol, A. Connely, A MOS Four-Quadrant Analog Multiplier Using the Quarter-Square Technique, IEEE Journal of Solid-State Circuits, pp. 1064-1073, vol. SC-22, 1987.
11. H.J. Song, C.K. Kim, A MOS Four-Quadrant Multiplier Using Two Input Squaring Circuits with Source Followers, IEEE Journal of Solid-State Circuits, pp. 841-847, vol. 25, 1990.
12. S. Sakurai, M. Ismail, A CMOS Square-Law Programmable Floating Resistor Independent on the Threshold Voltage, IEEE Transactions on Circuits and Systems II, vol. 39, pp. 565-574, 1992.
13. O. Landolt, E. Vittoz, P. Heim, CMOS Selfbiased Euclidean Distance Computing Circuit with High Dynamic Range, Electronic Letters, vol. 28, pp. 352-354, 1993.
14. S. Churcher, A.F. Murray, H.M. Reekie, Programmable Analogue VLSI for Radial Basis Function Networks, Electronic Letters, vol. 29, pp. 1603-1605, 1993.
15. S.I. Liu, Y.S. Hwang, CMOS Four-Quadranr Multiplier using Bias-Offset Crosscoupled Pairs, Electronic Letters, vol. 20, pp. 1737-1738, 1993.