# MOS Class E Power Amplifier Optimization for Wireless Applications

of Subharmonically Drain Pumpedof{private }
Katibe Ilhan
*e-mail:Katibe.Ilhan@enk.ericsson.se*
*Ericsson Telecommunication A.S. Istanbul, Turkey,*

Osman Palamutçuoğulları
*e-mail: opal@ehb.itu.edu.tr*
*Istanbul Technical University, Electrical & Electronics Faculty, 34469, Maslak, Istanbul, Turkey*

Key words:Class-E Amplifier, Non-linear capacitance, Efficiency

## ABSTRACT

**An alternative optimization and the design technique which would lead to better understanding of the trade offs in Class E performance is introduced. The limitations of the classical Class E theory for the high frequency design is considered and it has been found that the main limitation arises from the fact that the parasitic drain-source capacitance is essentially non-linear. A novel Class-E theory was proposed for to calculate the optimum component values with non-linear shunt capacitance. The proposed theory is based on the physical proporties of this capacitor and thus not restricted to any particular capacitance model. This approach has proved to be efficent as a good first-cut Class –E design. It has finally shown that the load matching at the fundamental frequency and the suppression of the second harmonic is sufficent for a Class-E design.**

## I. INTRODUCTION

Therotically, Class-E amplifiers with almost 100% efficiency can be achieved if optimal conditions are met[1], [2]. For a given supply voltage, output power and duty-cycle, the required shunt capacitance which is connected across the output of the switching transistor is inversely proportional to the operating frequency. When this frequency is in the range of 1GHz or higher, the required shunt capacitance becomes comparable to or even smaller than the output parasitic capacitance of the transistor. Therefore, the non-linear effect of this capacitance becomes a key factor for the design of Class-E amplifiers for applications.

The first attempt to use the non-linear output capacitance as a substitude to the linear shunt capacitance was made by Chudobiak [3]. In his paper, an analytic theory with a parasitic non-linear capacitance with abrupt junction capacitance was presented. A different approach which is based on numerical methods with hyper-abrupt junction capacitance model with the grading coefficent MJ=0.5, 0.67 and 0.75 was presented by Alinikula[4]. But, his theory which is based on a simple hyper-abrubt junction capacitor is not sufficent for practical applications. Additionally, the inductance value of DC-feed inductor (RF choke) is assumed to be infinitely large in both theories by Chudobiak and Alinikula. Practically, this inductance cannot be very large due to the undesireable effects of the series resistance and self-resonance. In certain applications, such as for envelope elimination and restoration system, it is desirable to use a small DC-feed inductor to allow modulation on the output voltage by the supply. But, a small DC-feed inductor can not provide an open circuit for the fundamental and its harmonics. Therefore, the effect of the harmonics should be included into the analysis. For linear passive components the circuit can be analyzed with standart techniques for ordiary differential equation problems [5]. To account for both non-linear shunt capacitance and finite DC-feed inductor value Genetic Algorithm and Ronger-Kutta Method was proposed for the computation of the optimum component values for the Class-E power amplifier[6]. In this work a new analyzis approach the optimal component values for Class-E power amplifiers with non-linear shunt capacitance are obtained numerically. Since this approach is based on the physical proporties of the capacitors, the computation is not restricted with any capacitance model. A simple output load network design with frequency matching at the fundamental and the second harmonic is suggested to accompany the numerical procedures as the second design stage of Class-E power amplifiers with both non-linear shunt capacitance and finite DC-feed inductor[7]. The non-linear shunt capacitance is asumed to be consisted with the gate-drain , drain-buttom junction and drain-sidewall capacitances.

## II. THEORETICAL ANALYSIS

The schematic representation of an ideal Class-E power amplifier is shown in Fig.-1.If an analytic expression for the non-linear capacitance is given the analysis of the circuit can be done under the following assumptions;

**The transistor acts as an ideal switch
**The inductance of the RF choke $L_1$ is infinite,
**The quality factor $Q_L$ of the resonant tank formed by $C_O$ and $L_O$ is infinite,
**All the passive components except $C_1$ are linear.
**The shunt capacitor $C_1$ is a reverse-biased hyper-abrupt juncion capacitor,
**The switching duty-cycle is 50%.

The analysis of the circuit was presented by several researchers [3],[4]. Since, exact behaviour of the shunt capacitances can not solely be represented by single capacitance model the better solutions can be reached if the physical proporties of the capacitors are considered.

The following assumptions were considered in the proposed analysis;

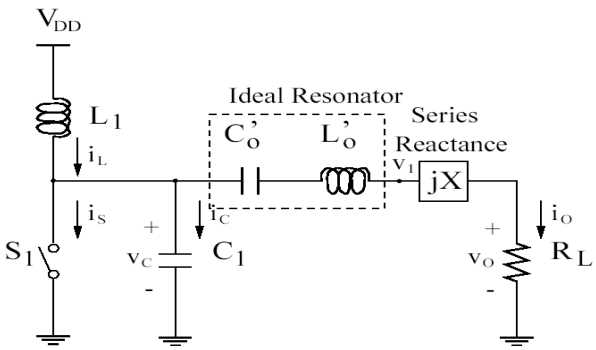


Fig.-1. The ideal model of Class-E power amplifier.

**The amount of stored charge is zero if only if the voltage across the capacitor is zero.
**The rate of change of the voltage across acapacitor is zero if only if the charging current is zero.
**The amount of stored charge increases monotonically with the voltage across the capacitor.
**For the same amount of stored charge, higher the than lower the voltage across the capacitance.

Since the currents and voltages vary periodically in the circuit, the charge in the capacitor can be written as;

$$Q_i(\theta) = \frac{I\theta + \frac{V_O}{R_L}\left[\cos(\theta+\varphi) - \cos\varphi\right]}{\omega} = \tag{1}$$

$$Q_v(v_c) = V_{bi}C_{jo}(n+1)\left[\left(1+\frac{v_c}{V_{bi}}\right)^{\frac{1}{1+n}} - 1\right]$$

where, I is the DC current, $V_O$ is the output voltage amplitude, $Q_v(v_c)$ and $Q_i(\theta)$ are the charges in the capacitor in terms of angular time $\theta$ and the capacitor voltage $v_c$, respectively. So, the optimal condition , $v_c = 0$ at $\theta = \pi$ can be written as;

$$Q_i(\pi) = Q_v(0) = 0 \tag{2}$$

$$I\pi - \frac{2V_O}{R_L}\cos(\varphi) = 0 \tag{3}$$

According to the capacitor characteristics, the rate of change of the voltage across the capacitance is zero if and only if the charging current is zero. Hence, the optimal condition $dv_c / d\omega = 0$ at $\theta = \pi$ leads to;

$$i_C(\pi) = 0, \qquad I - \frac{V_O}{R_L}\sin(\varphi) = 0 \tag{4}$$

Equations (2), (3) and (4) gives the following results;

$$\varphi = \tan^{-1}(-\frac{2}{\pi}), \qquad I = \frac{P_O}{V_{DD}}$$

$$R_L = \frac{2V_{DD}^2}{\left[1+\frac{\pi^2}{4}\right]P_O}, \quad V_O = IR_L\sqrt{1+\frac{\pi^2}{4}} \tag{5}$$

It is interesting to see from these results that the Class-E conditions are uneffected by the non-linearity of the shunt capacitor. The phase shift $\varphi$ and DC current is unchanged,
the required load $R_L$ and the output voltage amplitude $V_O$ are uneffected by the non-linearity of the capacitor.

The numerical method can be generalized for any non-linear shunt capacitor. In this case the second equation in (1) will be considered as;

$$Q_v(v_c) = \int_0^{v_C} C_1(v)dv \tag{6}$$

For a given expression of $C_1(v)$, the charge $Q_v(v_{c)}$ can
be obtained from (6). Given any $C_1(v)$, the drain voltage $v_C(\theta)$ can be obtained by solving the root of the following equation with the bisection method for each value of angular phase $\theta$ ;

$$G(v_c) = Q_v(v_c) - Q_i(\theta) \tag{7}$$

Considering the non-linear capacitance $C_1(v,\alpha)$ with parameter $\alpha$ such that;

$$C_1(v,\alpha_1) < C_1(v,\alpha_2) \text{ if } \alpha_1 < \alpha \ , \ \forall v \tag{8}$$

$$\int_0^{v_C} C_1(v,\alpha_1)dv \ < \ \int_0^{v_C} C_1(v,\alpha_2)dv \tag{9}$$

which is equivalent to;

$$Q_v(v_c,\alpha_1) < Q_v(v_c,\alpha_2) \tag{10}$$

Since $Q_v(v_c,\alpha_1)$ is a monotonically increasing function of voltage across $C_1(v,\alpha_1)$ must be higher than across $C_1(v,\alpha_2)$ for the same amount of stored charge $Q_i(\theta)$,

$$v_c(\theta,\alpha_1) > v_c(\theta,\alpha_2) \quad \text{if} \quad \alpha_1 < \alpha_2 \tag{11}$$

Therefore, the average drain voltage $\bar{v}_c(\alpha)$ is a monotonically decreasing function of $\alpha$ and its value can
be found by calculating the root of the following function by the bisection method.

$$F(\alpha) = \bar{v}_c(\alpha) - V_{DD} \tag{12}$$

As it is shown above generalized method requires two bisectional procedure loops. The outher loop is used to find of $F(\alpha)$ in Eq.(12) and the inner loop is used to find the root of $G(v_c)$ in Eq.(7) for the each value of $\theta$. After finding the optimized value of $v_c(\theta)$ the series reactance $jX$ and the normalized power capability can be calculated .

In a traditional Class-E load network the DC feed inductor $L_1$ is a RF choke. But, since it is difficult to provide RFCs in the IC realizations particularly, for RF applications realizations using a finite inductance is preferable [8]. If the finite inductance is used than, we have one more degree of freedom- the value of DC-feed inductance- in choosing the element values for a given output power than with an RFC. The load resistance $R_L$ is now not only the function of the output power and supply voltage but also the value of DC-feed inductance. Since the finite DC-feed inductor can be regarded as a part of the output load network, the design of the Class-E power amplifier can be divided into two stages; Firstly, the required non-linear shunt capacitance $C_1$ and the excess reactance $jX$ can be obtained in time-domain with the numerical method described above. Then the output network with finite DC-feed inductor is designed in the frequency domain to provide an appropriate load for the switch with the shunt capacitor.

It has been observed that an appropriate load at the fundamental frequency and an open circuit at the second harmonic are sufficent for the Class-E operation. This requirement can be met in practice in some extend by designing the network to provide the required load at the fundamental frequency and a large reactive load at the second harmonic and capacitive load at the third and higher harmonics.

The proposed circuit for a Class-E power amplifier with a finite DC-small inductor as shown in Fig.-2. A linear capacitor $C_2$ is added in parallel with the required shunt capacitor $C_1$.

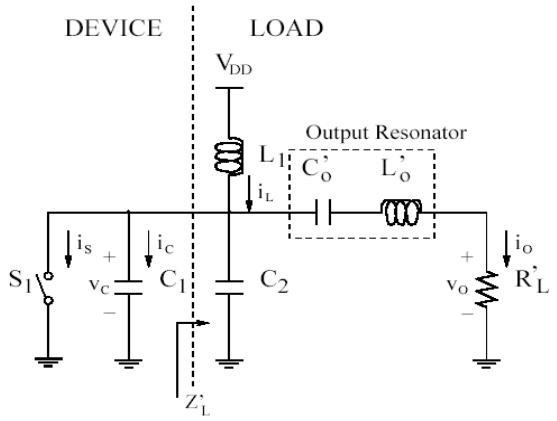


Fig.-2. Class-E power amplifier with finite DC-feed inductor.

The component values of the output load network are given by:

$$R_L^{'} = \left(1 + \tan^2(\psi)\right)R_L \tag{13}$$

$$L_1 = \frac{3}{4}\left(\tan(\psi) + \frac{1}{\tan(\psi)}\right)\frac{R_L}{\omega_0} \tag{14}$$

$$C_2 = \frac{1}{4L_1\omega_0^2} \tag{15}$$

## III. DESIGN EXAMPLE

An amplifier giving 1 W output power with 3,3 V supply voltage is designed by using the method described above. The AMS- $0{,}35\mu m$ CMOS process BSIM3v3 model is used in the simulation. The drain parasitic capacitance for this particular technology is modeled as;

$$C_1(v_c) = w\left[cgd0 + ld + cj\left(1 + \frac{v_c}{pb}\right)^{-mj} + cjsw\left(1 + \frac{v_c}{pbsw}\right)^{-mjsw}\right] + 2ld.cjsw\left(1 + \frac{v_c}{pbsw}\right)^{-mjsw} - 2dwc.cgd\,0 \tag{16}$$

where, cgd0, cj, pb, mj, cjsw and dwc are dependent parameters, w is the channel width and ld=1,1 $\mu m$ is the length of the drain. The load resistance $R_L$, the

capacitance $C'_O$ and the inductance $L'_O$ of the series resonator are independent of the non-linearity of the shunt capacitance. They were calculated by using the numerical method as described above which resulted as;

$R_L = 6{,}28\ \ \Omega, C'_O = 2{,}534\ \ pF, L'_O = 10\ \ nH$.

Minimum channel length of $0{,}6\ \mu m$ is used to maximize the drain current driving capability of the transistor. The design stages can be outlined as follows;

*Stage-1:* The optimum width of the NMOS transistor and the excess reactance were calculated by using the numerical method as described above which resulted as;

$w = 4631{,}5\ \ \mu m$, $X = 7{,}465\ \ \Omega$ which corresponds to the inductance of $1{,}19\ \ nH$ and $\tan(\varphi) = 1{,}18$ identical to $\varphi \cong 50^0$. A large DC-feed inductor $L_1 = 1\mu H$ was required to satisfy the assumtion of the infinite DC-feed inductance.

*Stage-2:* The component values for the load network with small DC-feed inductance were also calculated by using the numerical method as described above which yielded;

$R'_L = 15\ \ \Omega$, $C_2 = 4{,}2\ \ pF$ and $L_1 = 1{,}50\ \ nH$.

The transient analysis were performed by the Cadence spectres simulator. The simulation time was set to be long enough for the circuit to reach the steady-state. A 1 GHz square-wave input was used to drive the switching transistor. The equivalent circuits which are found from the simulations are shown in Fig.-3 and Fig.-4.

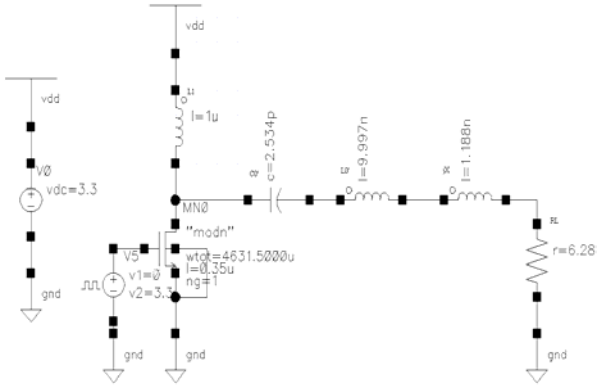


Fig.-3: Simulated equivalent circuits of the amplifier with large feed inductance.

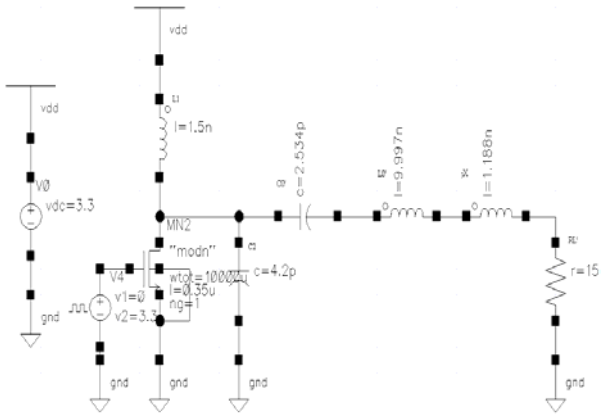


Fig.-4: Simulated equivalent circuits of the amplifier with small feed inductances.

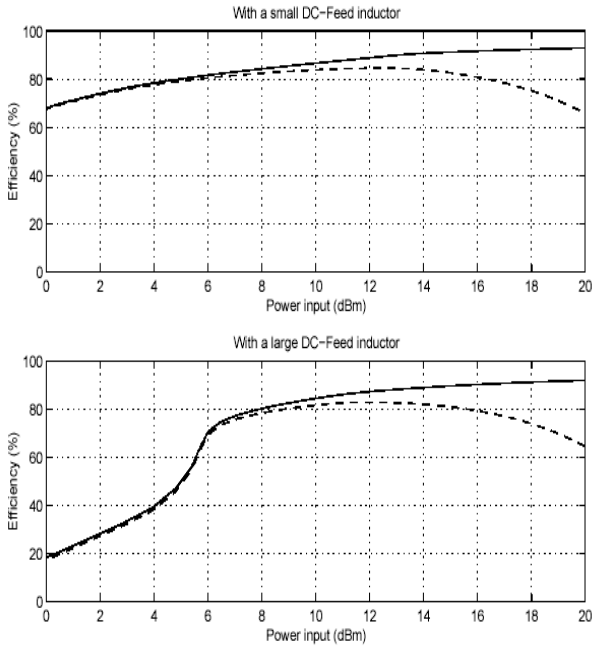


Fig.-5: Drain efficiency(continuous line) and PAE(dashed line) variations with input power.

The drain and the power added efficiency variations of the both circuit are plotted in Fig.-5. As it is seen from the figures PAE over 80% is obtainable with the input power of around 8 dBm (6,3 mW).

The waveforms for drain voltage , drain-to-source current and the output currents which are found from the simulated circuits are plotted in Fig.6 and Fig.7 for the both cases. It is clearly seen from those figures that the drain voltage and its slope aproach zero before the switch turned on in both cases. Therefore, the presented method proves that the similar waveforms and efficiencies are also obtainable by using a small DC-feed inductance which

eases the requirements for the realization of this inductance inside an IC.

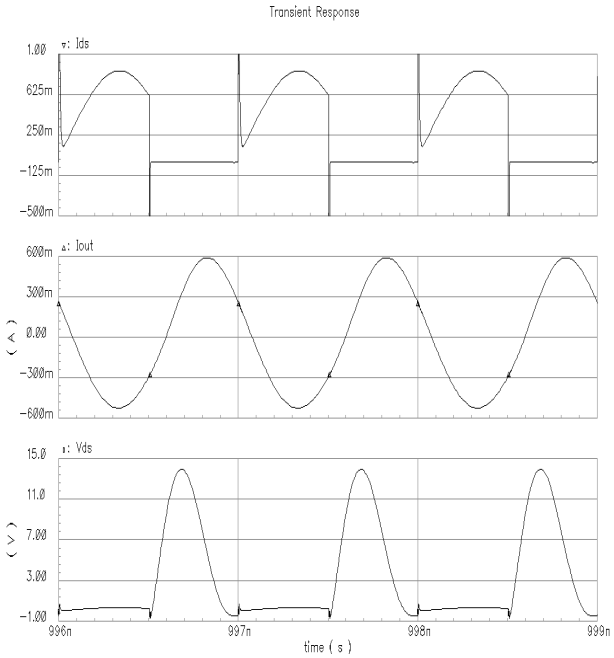


Fig.-6:Waveforms of the simulated amplifier with large DC-feed inductance

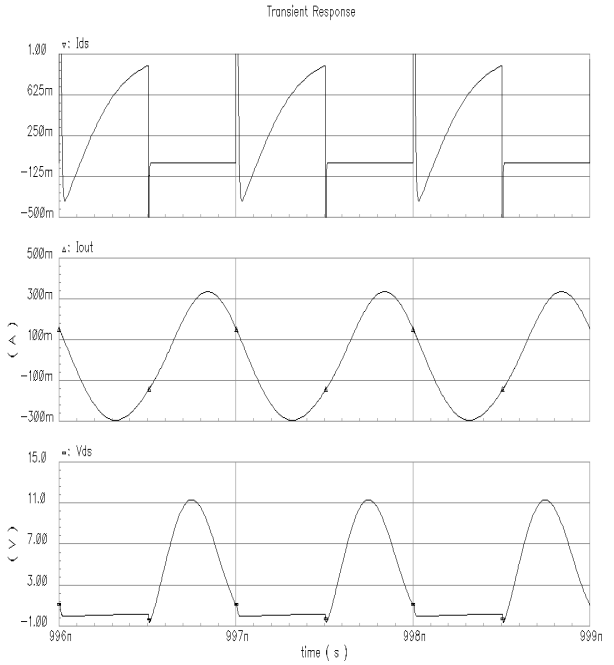


Fig.-7:Waveforms of the simulated amplifier with a small DC-feed inductance

## IV. CONCLUSION

A physically based numerical method to find optimum component values for Class E power amplifiers with non-linear transistor output capacitance is presented. Component values for Class E power amplifiers with hyper-abrupt junctions is investigated. It has been shown that the method can also be applied to a realistic drain capacitance model which consists of gate-to-drain capacitance, drain bottom junction capacitance and drain sidewall junction capacitance. A simple and effective method is presented to find the component values for Class E power amplifiers with non-linear transistor output capacitance and finite DC-feed inductance. It has been shown that the results are almost identical with those obtained with the infinite DC-feed inductance under the condition that the matching of the output load at the fundamental frequency and the second harmonic. The simulation results of a 1*GHz* Class E CMOS power amplifier showed that 80% PAE is obtainable under the optimized conditions which demonstrate the validity of the method.

## V. REFERENCES


1. N. O. Sokal and A. D. Sokal,"Class E-a new class of high efficiency tuned single-endedswitching power amplifiers", *IEEE Journel of Solid-State Circuits*, vol. 10, pp.168-176, 1975.
2. F. H. Raab, "Idealized operation of the Class E tuned power amplifier," *IEEE Transactions on Circuits and Systems*, vol. 24, pp. 725-735, 1977.
3. M. J. Chudobiak,"The use of parasitic nonlinear Capacitors in Class E amplifiers*" IEEE Transactions on Circuit and Systems-I: Fundamental Theories and Applications"*, vol. 41, pp. 941-944, 1994.
4. P. Alinikula, K. Choi and S. I. Long, "Design of Class E power amplifier with nonlinear parasitic output capacitance," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 46, pp. 114-119, 1999.
5. R. E. Zulinski and J. W. Steadman, "Class E power amplifier and frequency multipliers with finite DC-inductance", *IEEE Transactions on Circuits and Systems*, vol. 34, pp. 1074-1078, 1987.
6. Y. Wang, and B. X. Gao, "Analysis of a Class E power amplifier with nonlinear parasitic capacitance, using genetic algorithm," *IEEE Transactions on Circuits and Systems*, vol. 46, pp. 829-832, 1999.
7. C. K. T. Chan and C. Toumazou, "Design of a Class E power with nonlinear transistor output capacitance and finite DC-feed inducance ", *Proceedings of the IEEE International Symposium on Circuit and Systems*, vol. 1, pp. 129-132, 2001.
8. C. P. Avratoglou and N. C. Voulgaris,. "A Class E tuned amplifier configuration with finite DC-Feed inductance and no capacitance in parallel with switch", *IEEE Transactions on Circuits and Systems*, vol. 35, pp.416-422, 1988