SUPERIOR-ORDER CURVATURE-CORRECTED PROGRAMMABLE VOLTAGE REFERENCES

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ABSTRACT

Two new voltage references will be presented, having the goals of low-power low-voltage operation and of an extreme temperature coefficient, respectively. The first circuit was based on the compensation of the nonlinear temperature dependence of the gate-source voltage for a subthreshold operated MOS transistor by a correction current obtained by taking the difference between two gate-source voltages. The reducing of *TCR* for the second circuit is achieved by the cumulative effect of two methods: autoprogrammable temperature stabilization of the chip and superior-order curvature-correction technique. A digital programmable loop is designed to select the optimal stabilization temperature and the optimal type of the curvature-correction. SPICE simulations confirm the theoretical estimations, *TCR* s of *5.51 ppm / K* and *0.0004 ppm / K* , respectively.

I. INTRODUCTION

The voltage references find applications in a large area of applications, including A/D and D/A converters, memories, data acquisition systems or smart sensors.

Two important goals in developing this class of circuits could be differentiated: one focusing on low-power low-voltage operation, the circuit being designed for portable equipments or medical devices and other referring to an extreme temperature behavior, dedicated to professional systems. In order to obtain a low-power operation, the supply voltage is typically much lower than the nominal supply voltage for the process and the minimum voltage of a battery often dictates it. For the high-performance voltage references, the system must operate on the nominal supply voltage, because all the circuits have to reach high performance. As a result of the superior performance of bipolar references with respect to the circuits using MOS transistors, the first approaches of high-performance voltage reference were implemented in bipolar technology. However, due to the nonlinear temperature dependence of the base-emitter voltage [1], it exists a theoretical limit for improving the temperature stability of a simple BGR. In order to reduce the temperature dependence of the bandgap reference, a lot of curvature-correction techniques [2]-[4] have been developed. For CMOS bandgap references, the required bipolar devices are realized as parasitic vertical or lateral transistors, available in CMOS technology. The result will be a small degradation of the circuit temperature behavior because of the poorer match of MOS devices' parameters with respect to those of bipolar transistors.

II. THEORETICAL ANALYSIS

There will be proposed two voltage references based on the same principle, but focusing on low-power low-voltage operation and on extreme temperature performance, respectively.

THE LOW-POWER LOW-VOLTAGE VOLTAGE REFERENCE

The first voltage reference represents an improvement of the circuit presented in [5], being designed for implementing in CMOS technology. The original idea is that each single bipolar transistor to be replaced by three MOS transistors working in weak inversion (Figure 1).

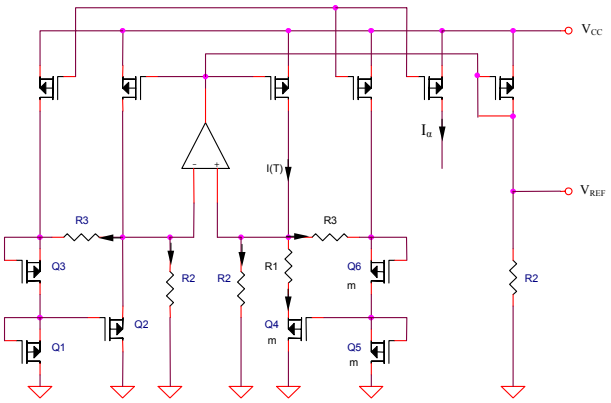

Figure 1: The low-power low-voltage voltage reference

The main advantages of these replacements are:

- The full compatibility with CMOS technology;
- The reducing of the mismatch errors;
- The canceling of the errors caused by the nonzero values of the base currents and by theirs temperature dependencies;
- The possibility of obtaining a very good controllability of the temperature behavior of the curvature-corrected voltage reference by choosing a proper temperature dependence of a polarization current, $I_\alpha = CT^\alpha$. The exact value of parameter α will be further determined in concordance with the current technology.

Considering a subthreshold operation of MOS transistors from Figure 1, the temperature dependence of gate-source voltage could be expressed as:

$$V_{GS}(T) = V_{FB} + E_G + \frac{V_{GS}(T_0) - V_{FB} - E_G}{T_0} T + \\ + \frac{nKT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_0} \qquad (1)$$

where T_0 is the reference temperature, E_G is the silicon bandgap energy, n and V_{FB} are constant parameters and γ models the temperature dependence of the carriers' mobility. The first term is a constant term, the second one is a linear term, which will be compensated by a complementary linear dependent on temperature current, I_{R_1} and the last term models the nonlinearity of the gate-source voltage temperature dependence. This term will be compensated by a suitable logarithmic dependent on temperature current, I_{R_3}, also added with $V_{GS}(T)/R_2$.

Imposing the design condition that both the linear and the logarithmic curvature-correction to be fulfilled and using the usual values $\gamma = 2$ and $R_2 / R_3 = 3$, it result $\alpha = 2$, equivalent with the necessity of polarizing Q_1, Q_3, Q_5 and Q_6 transistors at $PTAT^2$ currents. The reference voltage will be approximately independent on temperature, $V_{REF} = 2(V_{FB} + E_G)$.

THE EXTREME PERFORMANCE AUTOPROGRAMMABLE THERMAL SYSTEM

In order to obtain an extremely small temperature coefficient, an autoprogrammable thermal system will be presented [6].

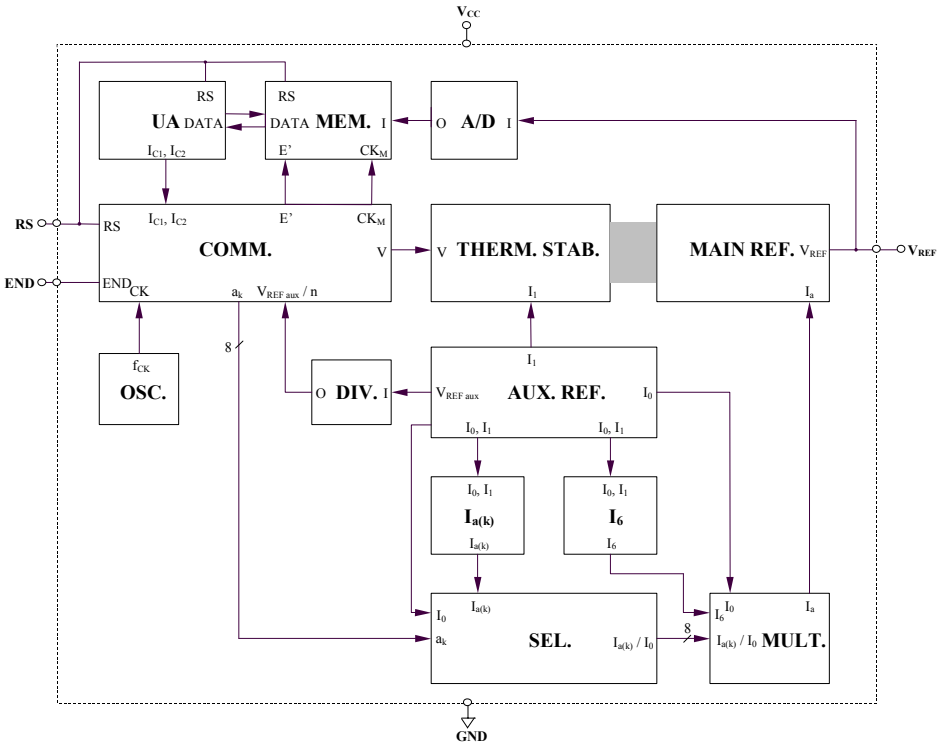

Figure 2: The block diagram of the thermal system

Considering that the main voltage reference from Figure 2 is implemented using the bipolar version of the circuit from Figure 1, the reference voltage will have the following expression:

$$V_{REF}(T) = 2E_G + (2\eta - \alpha - 1)\frac{KT}{q}\left(1 + \ln\frac{T_0}{T}\right) \quad (2)$$

In order to cancel the temperature dependence of V_{REF}, it is necessary that $\alpha = 2\eta - 1$, where η is a technology dependent parameter, with an usual value of $3{,}6 \div 3{,}7$. Because η has an empirical value, an accurate value of α is difficult to achieve. The new proposed idea is to implement an automate loop, which digitally select the optimal value of α from a large list of values, between 6 and 7. The concrete implementation of this technique is based on a constant factor, $PTAT^6$ and a variable factor, $PTAT^{0\div1}$. The selection of the optimal value for the α parameter is digitally made, with a 8 bit resolution.

$I_{a(k)}$ circuits implement $PTAT^{1/2^k}$ currents for realize a $PTAT^{\alpha}$ temperature dependence. In order to obtain $\alpha = 6 + \sum_{k=1}^{8} a_k / 2^k$ expression, 8 identical current multipliers were used (a_k are binary coefficients). The selection of the currents active in the computation of the α exponent (equivalent with the selection of the current curvature-correction technique) will be made using 8 selection circuits. I_0 and I_1 are approximately independent on temperature and $PTAT$, respectively.

The thermal stabilization circuit will fixed the main reference temperature at an optimal value T_0. A variation range of the stabilization temperature between $(T_0)_0 = 365K$ and $(T_0)_{15} = 380K$ will be imposed in order to minimize the difference between T_0 and the central point of the circuit temperature characteristic.

Together with the arithmetical unit, the command circuit will start and supervise the study of the voltage reference thermal characteristic and the selection of optimal stabilization temperature and of optimal correction type. The stabilization circuit drive is achieved by a digital changing of potential V in $365mV \div 380mV$ range, with a $1mV$ step.

The measurement cycle

This cycle will assure the data basis for evaluate the thermal behavior of the entire system, resulting 256×16 values of the reference voltage, corresponding to 256 distinct curvature-corrections and to 16 values of stabilization temperature. Based on this information, an arithmetical unit UA will determine the optimal correction and the optimal reference temperature.

Resetting the system

An output RS signal, applied to $C1$ and $C2$ counters and to B bistabil at t_0 moment will start the system with the first correction ($\alpha = 6$) and with the first temperature $(T_0)_0 = 365K$.

Measurements for $(T_0)_0 = 365K$

Applying f_{CK} on the clock input of $C1$ will increment it, passing through all the 256 types of correction. $C2$ will remain in the "0" state (equivalent with $(T_0)_0$ temperature) and $CK_M = f_{CK}$ (the memory is active and store the 256 distinct values of V_{REF}).

Heating of the system from $(T_0)_0$ to $(T_0)_1$

After $256T_{CK}$ (t_1 moment), $O_9O_{10} = 10$, so $CK_2 = 1$ and $C2$ will pass in "1" state, equivalent with $(T_0)_1 = 366K$. Because of the thermal inertia of the system, the $t_1 - t_2$ interval (whose length depends on the chip thermal resistance) is introduces to allow the system to stabilize at $(T_0)_1$. For this reason, f_{CK} is disconnected from the memory for $3\times256T_{CK}$; CK_2 will fall when O_9O_{10} becomes 01.

Measurements for $(T_0)_1 = 366K$

At t_2 moment, the temperature is stabilized al $(T_0)_1$, so the measurements are valid. $CK_M = f_{CK}$, equivalent with an active memory.

The cycle is repeated for all the 16 values of the temperature, resulting 256×16 values for V_{REF} stored in the memory. An A/D converter resolution of 32 bits is enough large in order not to introduce supplementary errors.

The optimization cycle

The measurement cycle ends at t_4 moment. After Δt_1 (which allows the arithmetical unit to compute the optimal values of the type correction and of the reference temperature), the PE inputs of the counters will be activated. After Δt_2 (necessary for the chip to stabilize at the optimal temperature), the END signal will be activated, pointing out the end of the optimization cycle and the validity of the reference voltage with autoprogramable superior-order curvature-correction.

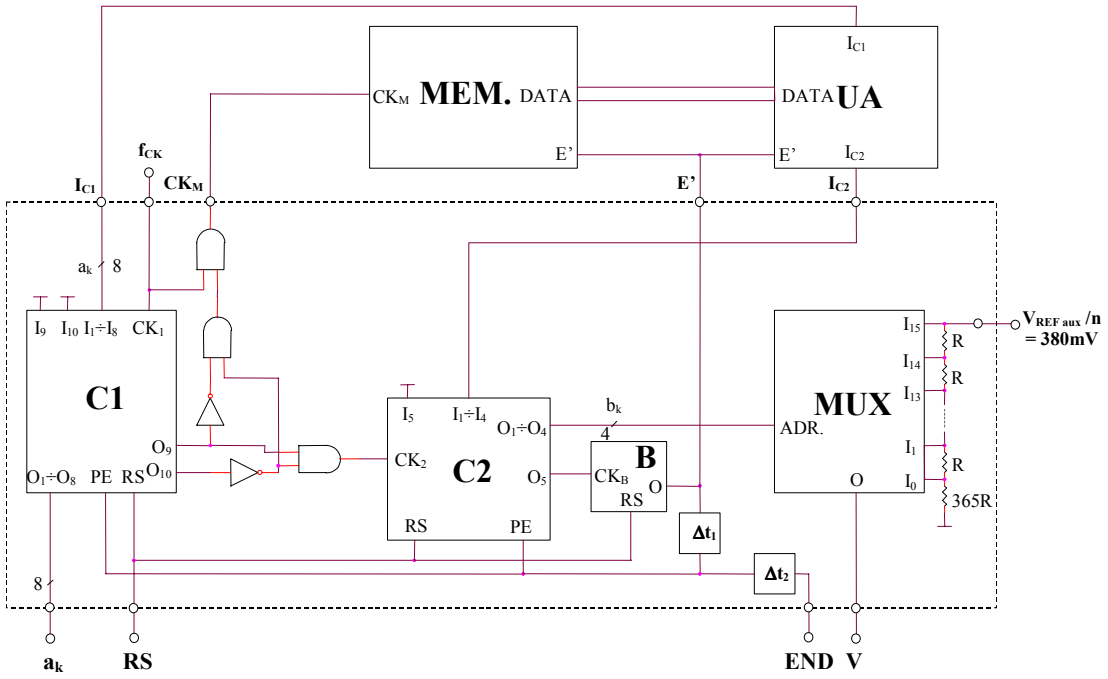

Figure 3: The command circuit

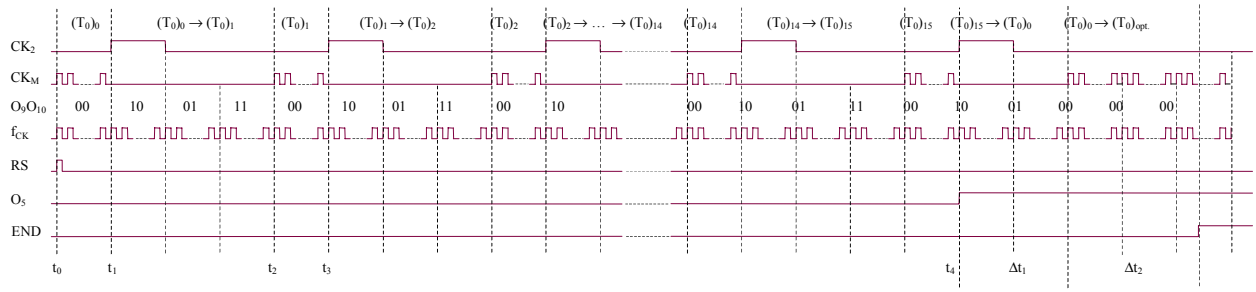

Figure 4: The graphical diagrams for measurement and optimization cycles

III. EXPERIMENTAL RESULTS

The SPICE simulation $V_{REF}(t)$ for the low-power low-voltage curvature-corrected voltage reference from Figure 1 ($0.35\mu m$ CMOS technology) is presented in Figure 5.

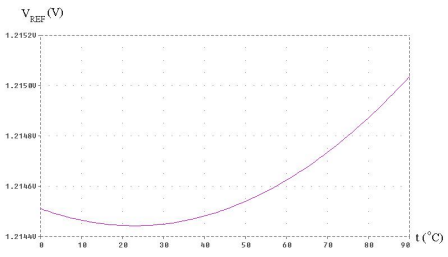

Figure 5: SPICE simulation $V_{REF}(t)$ for the low-power low-voltage circuit

The simulated temperature coefficient is $TCR = 5.51 ppm/K$ for $0 < t < 90^{o}C$ and $V_{CC} = 2.5V$. The simulated results $V_{REF}(t)$ for the autoprogrammable thermal system, using 5 values of α parameter $(0,1,2,6,7)$, are presented in Figure 6, showing a decreasing of the temperature coefficient when α matches better the theoretical estimated values (Table 1)

Table 1

α	0	1	2	6	7
$TCR(ppm/K)$	3.4	1.3	0.013	0.002	-0.0004

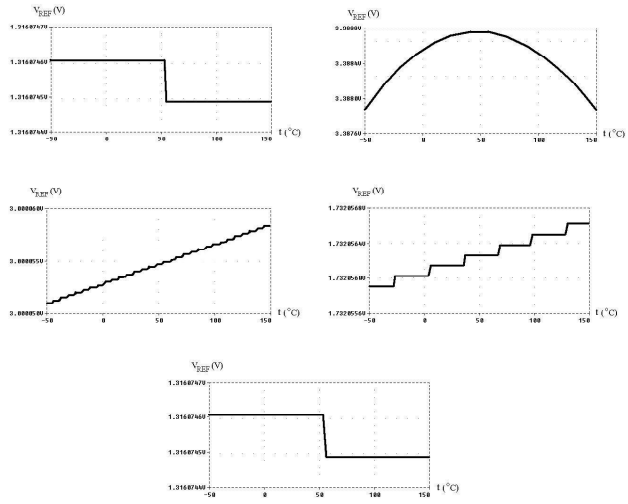

Figure 6: Simulation results for $V_{REF}(t)$

CONCLUSIONS

Two superior-order curvature-corrected voltage references have been presented, focusing on low-power low-voltage operation and on high performance.

The new proposed low-power low-voltage circuit was based on the compensation of the nonlinear temperature dependence of the gate-source voltage for a subthreshold operated MOS transistor by a correction current obtained by taking the difference between two gate-source voltages for MOS transistors polarized at drain currents with different temperature dependencies. The low-power operation was achieved by polarizing MOS transistors in weak inversion. The circuit was implemented in $0.35\mu m$ CMOS technology. The SPICE simulation based on the previous mentioned technology confirms the theoretical estimated results, reporting a temperature coefficient of $5.51ppm/K$ for an extended temperature range, $0 < t < 90^{o}C$ and a small supply voltage, $V_{CC} = 2.5V$.

The thermal system with multiple superior-order curvature-correction from the second part includes an autoprogrammable digital loop, which selects the optimal values of the curvature-correction type and of the stabilization temperature. The minimal value of the simulated temperature coefficient was about $0.0004ppm/K$ (an idealized value because no mismatches' errors have been considerred), the circuit requiring a technology with small parameters' spread.

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