Flying Adder Principle Frequency Synthesizer

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Abstract

The frequency synthesis is one of the most important and most actively researched subjects in the field of VLSI mixed-signal circuit design. Among the existing techniques in this area, phase locked loop fractional architecture is a widely used one for generating frequencies which are not integer multiple of the input reference frequency. Flying-Adder architecture is an emerging technique which is based on a new concept time-average-frequency, to generate frequencies. This paper presents simple fractional frequency synthesizer architecture based on concept flying-adder and phase locked loop principle. The simulation results concerning this approach are presented.

1. Introduction

In the history of frequency synthesis development, Phase-Locked Loop (PLL) based synthesis method is the mostly used approach. Within this approach, there are several milestone techniques: Integer-N architecture, Fractional-N architecture and Sigma-Delta Fractional-N architecture. Integer-N PLL is commonly used in the cases where frequency requirement is straightforward. Fractional-N PLL is a technique which can generate output frequencies that are fractional multiples of the input reference frequency. This is important step forward from the Integer-N PLL. However, this advancement is accompanied with a serious drawback. It degrades the spectrum purity of the output frequency. To overcome this problem, Sigma-Delta Fractional PLL was developed [1-5].

The Flying-Adder architecture is an emerging technique in the field of frequency synthesis. The proof of concept was constituted in 2000 [6]. It was built on the foundation of a new concept: Time-Average-Frequency. The theoretical foundation was established in 2008 [7, 8]. The more in-depth study is delivered in [9, 10]. The most distinguished features of this technique are its instantaneous response speed and the capability of generating arbitrary frequency [6].

In this paper, the architecture of fractional flying adder (FFA) is used with conjunction of PLL. Compared to the pure structure FFA frequency synthesizer, the proposed approach can achieve the same frequency resolution with reduced fractional spurs.

2. The Synthesizer principle

The FFA [6, 7], which is also referred to as direct digital period synthesizer or digital-to-frequency converter (DFC), is an independent frequency synthesis. The FFA shares some functionality with circuits that involve phase-switching prescalers and digital phase accumulators [9, 10].

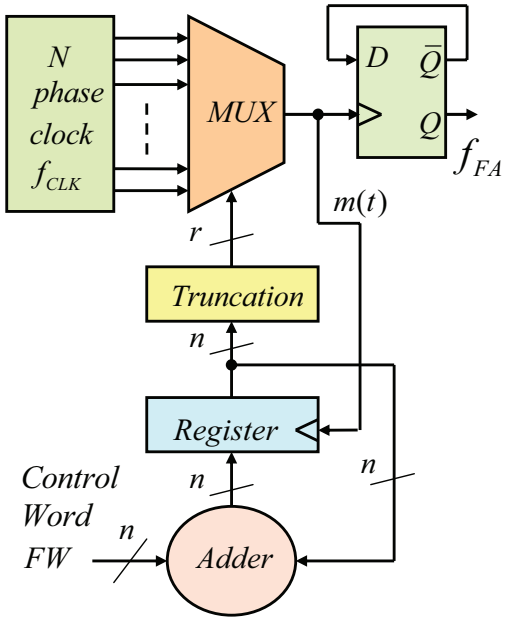

Fig. 1.The block diagram of basic fractional flying adder (FFA) frequency synthesizer consist of: *N*-phase clock generator (frequency f_{CLK}), multiplexer MUX, D-flip-flop, digital adder with control frequency word FW, register and truncation which convert *n*-bit word to *r*-bit word.
The output frequency of FFA is f_{FA}.

The block diagram of basic FFA is shown in Fig. 1. All parts of this system is digital. The system is driven by the $N = 2^m$ clock phases with frequency f_{CLK}), one of which is selected by the *N*-to-1 multiplexer (*MUX*). The rising edges of *MUX*'s output (signal *m(t)*) is a trigger for the *n*-bit register changing its value from

$$x_{k+1} = (x_k + FW) mod 2^n \tag{1}$$

where *FW* is the *n*-bit long frequency control word and *k* is integer variable which presents counts of the rising edges of signal *m(t)*. The register value x_k, is then truncated by taking the first *r*, most significant bits to y_k according (2).

$$y_k = fix\left(\frac{x_k}{2^{n-m}}\right) \tag{2}$$

The y_k controls the *MUX* and therefore chooses the input phase that passes through the *MUX*. The signals *m(t)* which is a sequence of pulses, or spikes is fed to the D-Flip-Flop which

acts as a frequency divider by-2 providing the output signal f_{FA}. FFA employs a multiphase generator to generate multiple clock signals evenly distributed in a full clock cycle. These same-frequency-but-different-phases clock signals are used to synthesize desired frequency. The synthesized signal is directly related to the phase difference $\Delta=\pi/4$ (for $N=8$) among the multiple outputs from the generator, see Fig. 2. The frequency control word FW sets the number of Δ before the synthesized clock toggles. The frequency f_{FA} of the clock output So is given by the following expression [11]:

$$f_{FA} = \frac{1}{FW \cdot \Delta} = \frac{1}{FW \dfrac{1}{f_{CLK} \cdot N}} = f_{CLK} \frac{N}{FW} \qquad (3)$$

where N is the number of VCO stages. It is important to note that value x_k, eq. (1) in *Register* is limited to 2^n-1 (function $mod2^n$) and therefore y_k, eq. (2) is also limited. Unlike the conventional PLL, the FFA consists of digital circuitry such as multiplexers, adders, and flip-flops, thereby resulting in fast switching time and wide tuning range. Specifically, an FFA architecture with an N-stage VCO has a frequency range of $0.5 \cdot f_{CLK}$ to $0.5 \cdot N \cdot f_{CLK}$ [5].

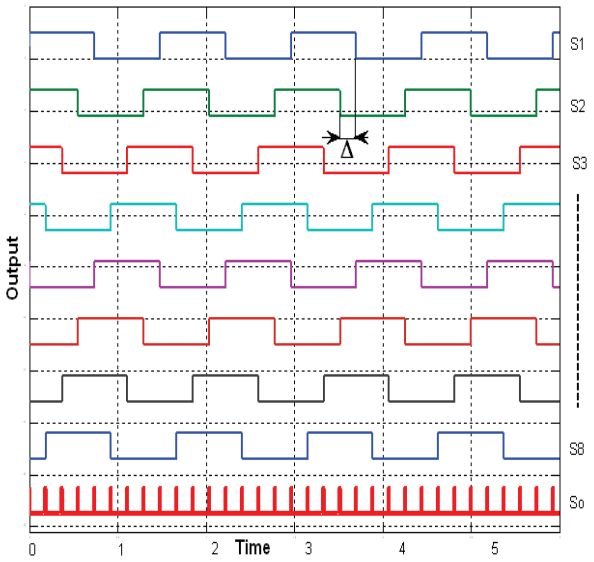

Fig. 2. Example of multiphase generator (8 phase generator, $N=8$, *S1, S2, S3 ... S8* with phase difference Δ among the multiple outputs and output pulses *So*. The output pulses are generated by digital edge combiner circuit.

Due to its wide tuning range and instant response time, the FFA frequency synthesizer is highly suitable for many System-on-Chip applications. The frequency control word could be an integer or a fractional number when high frequency resolution is desired. When FW is an integer, the FFA synthesizer can be viewed as a phase divider which can achieve finer resolution than frequency divider does. When FW is a fractional word, the FFA modulates the output frequency to achieve higher resolution. The frequency modulation results in spurious spikes in the frequency spectrum. Although dithering methods can be used to eliminate or effectively reduce the spurs, this approach comes at the cost of increased overall noise.

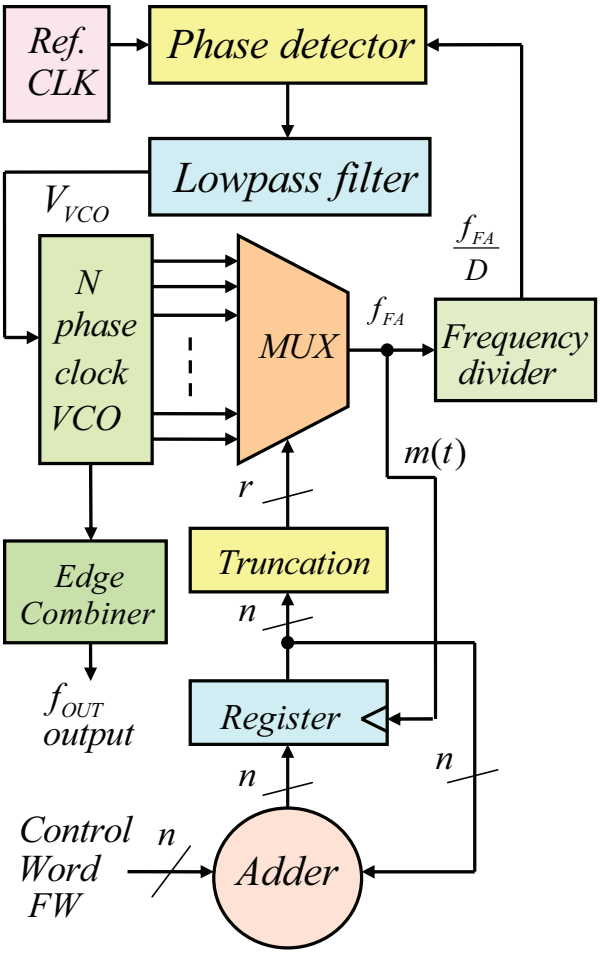

Fig. 3. The block diagram of second type fractional frequency synthesizer based on PLL and FFA principles. The synthesizer consists of: Reference clock, N-phase voltage controlled oscillator (controlled by V_{VCO}), multiplexer MUX, frequency divider (divide by number D), digital adder with control frequency word FW, register and truncation which convert n-bit word to r-bit word. Output frequency of FFA is f_{FA}. The synthesizer output frequency is f_{OUT}.

3. The second type synthesizer

The block diagram of the proposed fractional frequency synthesizer based on flying adder principle and PLL is shown in Fig. 3. The synthesizer consists of: Reference clock, charge-pump phase detector, N-phase voltage controlled oscillator (controlled by voltage V_{VCO}), multiplexer MUX, frequency divider (divide by number D), digital adder with control frequency word FW, register and truncation which convert n-bit word to r-bit word. Output frequency of FFA is f_{FA}. The synthesizer output frequency (generated by edge combiner) is f_{OUT}. The output frequency of this synthesizer is given by (4) and (5). For $(FW) mod2^n \in <0, 2^n\text{-}N>$

$$f_{OUT} = f_R N D \left(1 - \frac{FW}{2^n}\right) \qquad (4)$$

and for $(FW) mod2^n \in <2^n\text{-}N, 2^n>$

$$f_{OUT} = f_R ND\left[(N-1)\frac{FW}{2^n} - (N-2)\right] \quad (5)$$

where f_R is frequency of reference oscillator, D is divider number, N-number of phases of voltage controlled oscillator, n is number of register bits and FW is control word..

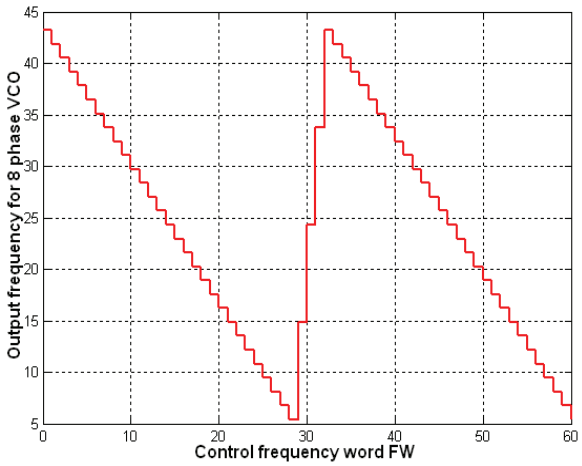

Fig. 4. The output frequency as function of FW for f_R=1.35, D=4, N=8 and n=5.

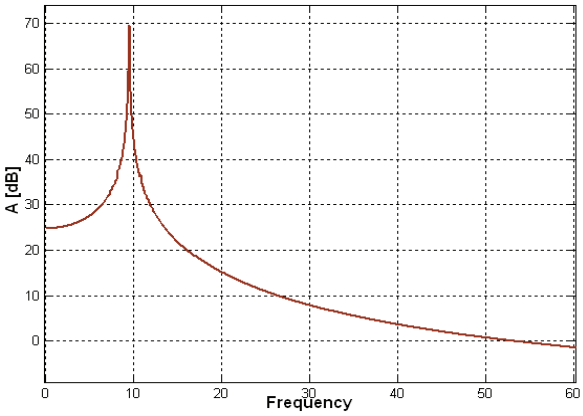

Fig. 5. The frequency spectrum (sinus output) for FW=25 and f_R=1.35, D=4, N=8 and n=5.

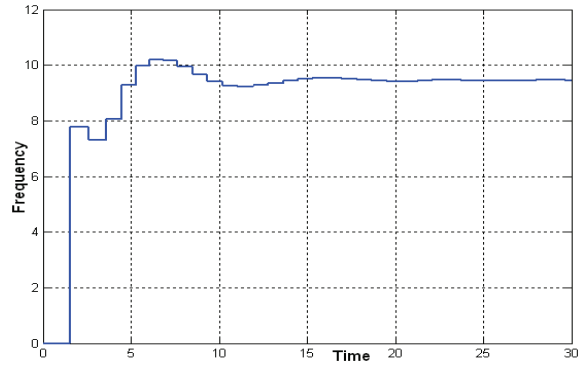

Fig. 6. The time response (step response) of the frequency synthesizer (from zero to 9.45) for FW=25 and f_R=1.35, D=4, N=8, n=5 and 4-th order low-pass filter.

The output frequency as function of FW for f_R=1.35, D=4, N=8 and n=5 is shown in Fig. 4. The maximal output frequency is 43.2. It is important to note that function shown in Fig. 4 is periodic, e.g. for n=5 and FW=32, FW=(32)mod32=0, therefore f_{OUT} is given by (4).

The example of frequency spectrum (sinus output) for FW=25 and f_R=1.35, D=4, N=8 and n=5 is shown in Fig. 5. The time response (step response) of the frequency synthesizer (from zero to 9.45) for FW=25 and f_R=1.35, D=4, N=8, n=5 and 4-th order low-pass filter with cut-of frequency is 0.5 is shown in Fig. 6.

The similar step response of PLL containing the 4-th order low-pass filter with the same parameters, are displayed in Fig. 7.

For fine tuning of output frequency the switching between $FW1$ and $FW2$ can be used. The block diagram of such synthesizer is shown in Fig. 8.

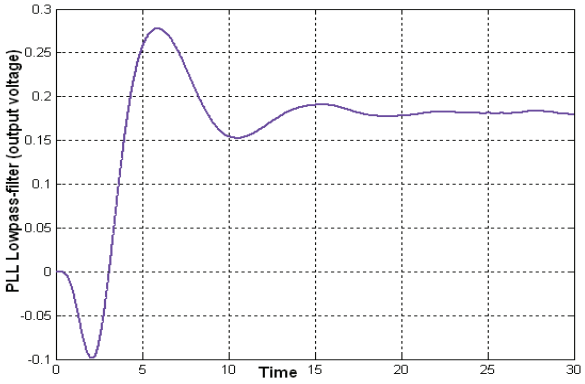

Fig. 7. The time response of PLL low-pass filter.

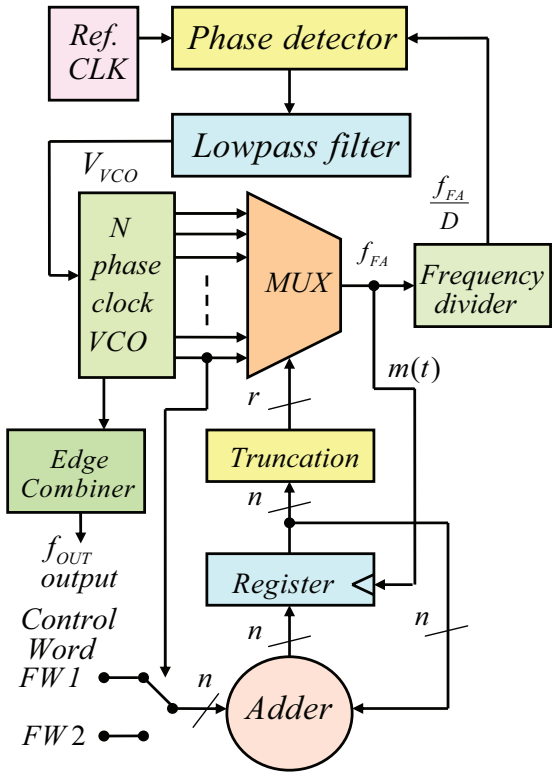

Fig. 8. The frequency synthesizer with switching FW.

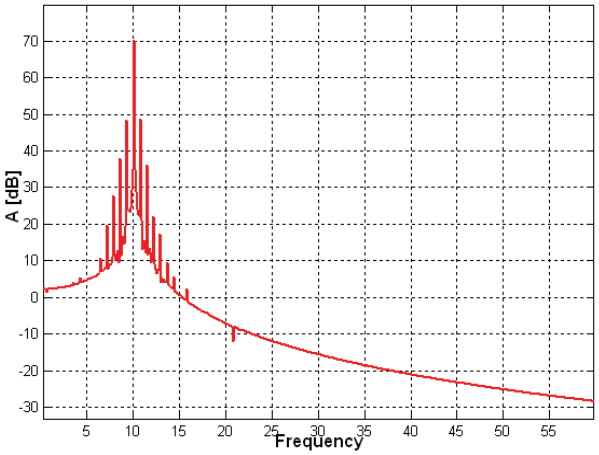

Fig. 9. The frequency spectrum of frequency synthesizer (Fig. 8) with switching *FW* between 24 and 25.

In Fig. 9. the frequency spectrum of synthesizer according Fig. 8. with switching *FW* (*FW1* and *FW2*) is shown. The block diagram concerning frequency synthesizer simulation is shown in Fig. 10. - on the last page. In this Fig., also the measuring blocks, scopes and blocks "To workspace" are added. The control frequency word is 28.

4. Discussion

The simulation results of fractional frequency synthesizer based on flying adder used in feedback and phase locked loop shown good spectral properties and time responses. In comparison with others types of fractional synthesizers, presented principle is much simpler. The maximal and minimal frequency ratio is given by (5).

$$\frac{f_{OUT\_MAX}}{f_{OUT\_MIN}} = N \tag{5}$$

and minimal frequency step Δf (without *FW* switching) is

$$\Delta f = f_R ND \frac{1}{2^n} \tag{6}$$

When the *FW* switching is used the minimal frequency step is $\Delta f/2$, but frequency spectrum contain more spurious lines.

6. Conclusions

Flying-Adder architecture is an innovative method for frequency synthesis. The effeteness of this technique has been proven by many commercial products in the past few years. The great advantage is that Flying-Adder architecture consists of pure digital circuitry such as multiplexers, adders, and flip-flops, thereby resulting in fast switching time, wide tuning range and therefore enables simple programmable logic construction. In this paper, a simple frequency synthesizer has been presented and simulated. The proposed approach uses Flying-Adder technique in cooperation with Phase Locked Loop. The trade-off of this approach is that Flying-Adder loses its "instant response" advantage, because in a Phase Locked Loop low-pass filter is included. Consequently, the response time will depend on the low-pass filter used in the Phase Locked Loop.

The main properties of synthesizer was described and simulated in this paper.

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7. References

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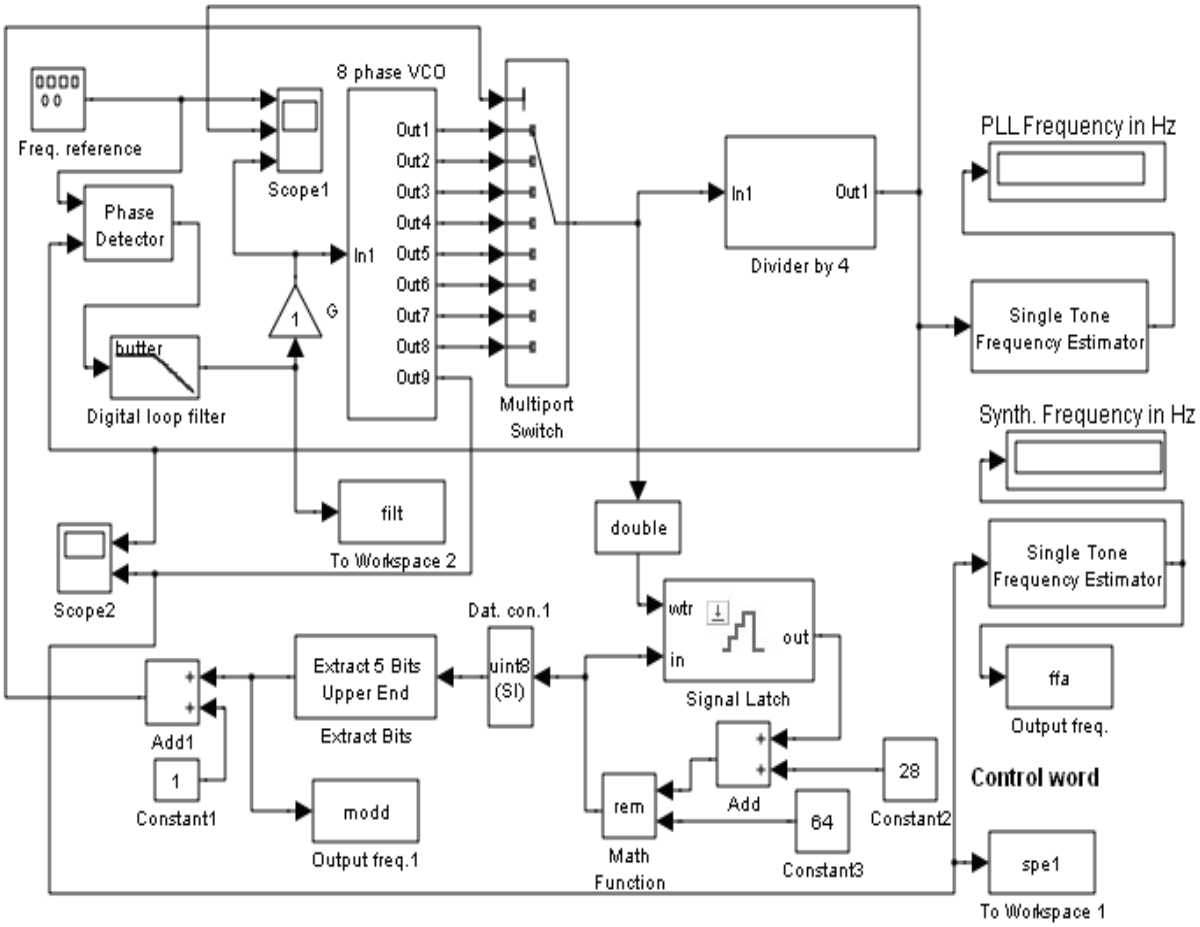

Fig. 10. The functional block diagram for simulation flying adder frequency synthesizer with measuring accessories (blocks) added. The control frequency word is 28.