A 0.13μm CMOS 5-MHz BW 47-dB SNDR All-Digital Time-Mode First-Order $\Delta\Sigma$ ADC with 3-bit Gated VCO Quantizer

G. Zhu, F. Yuan and G. Khan

***Abstract*— This paper presents an all-digital time-mode first-order $\Delta\Sigma$ ADC with 3-bit gated VCO quantizer. The $\Delta\Sigma$ ADC consists of a voltage-to-time integrator that performs both voltage-to-time conversion and feedback subtraction, a 7-stage gated current-starved ring oscillator as a 3-bit quantizer, and a digital differentiator that provides both first-order noise-shaping and frequency feedback. Implemented in IBM 0.13 μm 1.2V CMOS technology, the ADC provides SNDR of 47.4 dB and SFDR of 34.1 dB over 4 MHz bandwidth. The power consumption of the ADC is 1.1mW. The silicon consumption excluding bonding pads of the ADC is 470 X 470 μm^2.**

***Index Terms*— Time-mode signal processing, gated-ring oscillators (GRO), time-mode $\Delta\Sigma$ modulators.**

I. INTRODUCTION

Conventional voltage-mode approaches to implement analog-to-digital converters (ADCs) becomes increasingly difficult due to deteriorating voltage accuracy caused by device scaling. Technology scaling, on the other hand, has sharply improved the time accuracy of digital circuits. As a result, time-mode approaches where analog variables are represented by the timing information of digital signals rather than the nodal voltages or branch currents of electric networks reap the benefits of scaling and offer a viable and technology-friendly alternative for mixed-mode signal processing [1], [2]. Itawa *et al.* demonstrated that an input voltage can be quantized using a multi-stage voltage-controlled ring oscillator and a counter (VCO phase quantizers) [3]. VCO phase quantizers possess an inherent first-order noise-shaping characteristic. In addition, since the frequency of ring oscillators scales well with technology, a large oversampling ratio (OSR) subsequently a better signal-to-noise ratio (SNR) can be obtained. The low power consumption of ring oscillators also makes them attractive for low-power applications. The long latency of the counter of these quantizers, however, limits OSR. Hovin *et al.* showed that first-order noise-shaping can be obtained by employing phase differentiators without using counters [4], [5]. We term these quantizers VCO frequency quantizers. As compared with VCO phase quantizers, VCO frequency quantizers offer the key advantage of speed, enabling a large OSR. Straayer *et al.* showed that gated ring oscillators also possess the desired first-order noise-shaping characteristics [6]. The performance of VCO quantizers, however, is greatly affected by the nonlinear voltage-to-phase characteristics of VCOs [7]. The absence of a mechanism to suppress the effect of the nonlinear characteristics of the VCO results in large harmonic tones at the output of the ADC, deteriorating signal-to-noise-plus-distortion ratio (SNDR). It is well understood that $\Delta\Sigma$ configuration is effective in reducing the effect of nonlinear elements. In addition, quantization noise is both noise-shaped by the loop characteristics and suppressed by the loop gain. The reduced swing of the control voltage of the VCO due to negative feedback also results in the reduced nonlinear characteristics of VCO quantizers. Since sampling takes place in the loop, the need for an anti-aliasing filter is also removed. To increase the order of time-mode $\Delta\Sigma$ ADCs so as to achieve a better SNDR, voltage-mode active loop filters have been widely used [8], [9]. Active loop filters, however, are non-digital and their performance scales poorly with technology.

In this paper, we propose an all-digital time-mode $\Delta\Sigma$ ADC with multi-bit VCO quantizer. The proposed $\Delta\Sigma$ ADC consists of a voltage-to-time converting integrator that performs both voltage-to-time conversion and feedback subtraction, a 7-stage gated current-starved ring oscillator as a 3-bit quantizer, and a digital differentiator that provides both first-order noise-shaping and frequency feedback. As our goal of this study is to explore possible architectures of all-digital time-mode $\Delta\Sigma$ ADCs, no active loop filter is employed. As a result, the order of the ADC is only one. Higher order $\Delta\Sigma$ modulators can be readily implemented using digital integrators such as those in [10].

II. ALL DIGITAL TIME-MODE $\Delta\Sigma$ MODULATOR

The block diagram of the proposed all-digital first-order $\Delta\Sigma$ ADC is shown in Fig.1. The ADC comprises of a voltage-to-time converting integrator, a DFF-based phase-frequency detector (PFD), a 3-bit GRO quantizer, and a first-order phase differentiator providing both first-order noise-shaping and frequency feedback. DFFs are implemented using true-single-phase-clock (TSPC) logic to take advantage of their high speed and low power consumption. The PFD detects the difference between the phase/frequency of the VTC integrator and those of the reference clock. The output of the PFD is a pulse whose width is proportional to the difference. It is digitized by the GRO. The first-order digital differentiator detects the threshold-crossing of the output voltage of each delay stage of the oscillator so as to yield the frequency of the GRO. In addition, it performs first-order noise-shaping on quantization noise.

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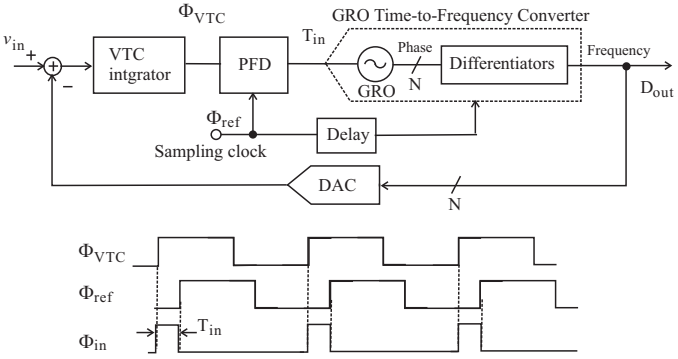


Fig. 1. Architecture of proposed all digital time-mode $\Delta\Sigma$ ADC.

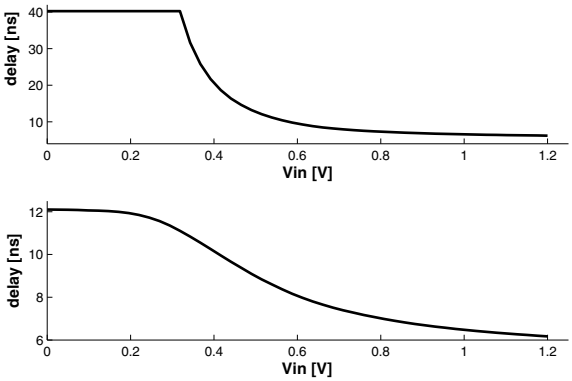
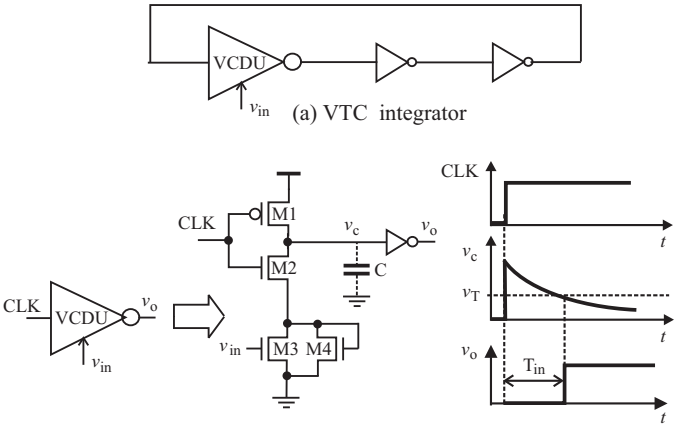


Fig. 3. Simulated dependence of the time delay of voltage-controlled delay unit on input voltage. Top : Without M4. Bottom : With M4.

A. VTC Integrator

The VTC integrator shown in Fig.2 is a voltage-control oscillator consisting of two voltage-control delay units (VCDU), one by the input voltage while the other by the feedback voltage. The VCDUs are implemented using a current-starved inverter in concatenation with a static inverter. Fig.3 plots the dependence of the delay of the VCDU on the input voltage. It should be noted that M3 should be in saturation to ensure a good transconductance. The use of M4 in parallel with M3 improves the linearity.

A DFF based phase/frequency detector (PFD) is deployed to capture the time difference between the rising edge of the output of the integrator and that of the reference clock. VTC integrator frequency should be set to a value that is slightly higher than that of the reference clock to prevent the accumulated phase of the VTC integrator from exceeding one sampling period (phase wrapping). The negative feedback stabilizing the frequency of the VTC integrator ensures that phase wrapping will not occur [11].



(b) Voltage-controlled delay unit (VCDU)

Fig. 2. (a) VTC integrator that comprises of two voltage-controlled delay units. (b) Schematic of voltage-controlled delay unit consisting of a current-starved inverter and a static inverter.

B. GRO-Based TDC

In this work, we use a 7-stage GRO followed by a first-order digital differentiator to map the time variable from the PFD to a 7-bit digital code (frequency). Fig.4 depicts the implementation of the GRO delay stage and that of the phase differentiator. It should be pointed out that even though the GRO quantizer offers first-order noise-shaping on the quantization noise, phase noise and other noise sources within the GRO, noises generated by other components will not be first-order shaped. Also any nonlinearity caused by the negative feedback path, which merges with the VTC integrator to perform a subtraction act, cannot be suppressed by the closed loop.

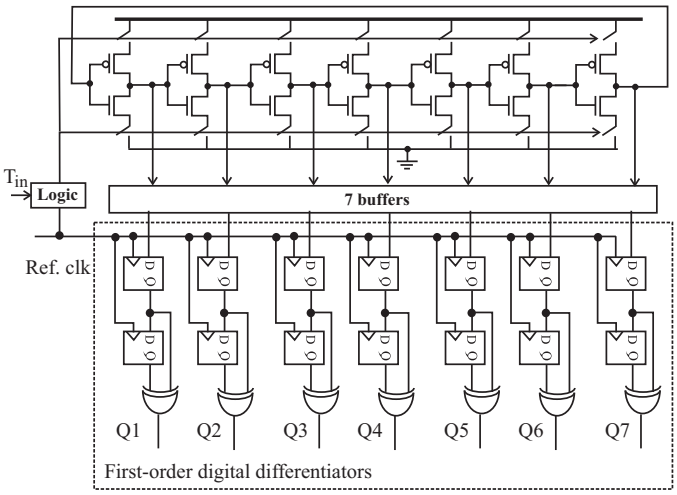


Fig. 4. Top : Gated ring oscillator. Bottom : First-order digital phase differentiators.

If the width of the gating pulse of the GRO is too small, the gated transistors will not be turned on fully and the GRO will seize its operation. Fig.5 plots the dependence of the pulse width of the input voltage to the sum of the output voltage of the seven first-order differentiators. It is seen that the GRO exhibits good linearity when the input pulse width is above 0.5 ns. Below 0.5 ns, the GRO seizes operation.

C. Frequency Feedback

A negative feedback is formed by feeding the digital output signal from the seven first-order digital differentiators to the

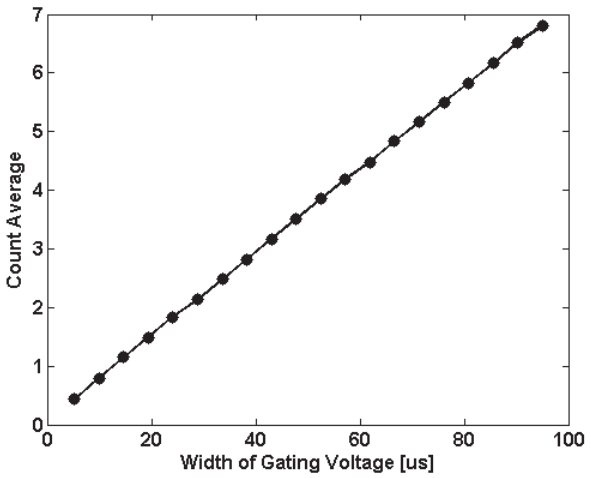


Fig. 5. Simulated transfer characteristic of GRO quantizer. The vertical axis is the sum of the voltage of seven phase differentiators.

capacitor node of the VCDU, as shown in Fig.6. Since the input voltage controls the discharging of this node, the feedback counteracts this by injecting a current from the top. If the input voltage increases, the discharging process will speed up, in other words, the rising edge after the regular inverter tends to advance, the negative feedback will try to delay the rising edge by subtracting a current directly proportional to the feedback from the discharging current.

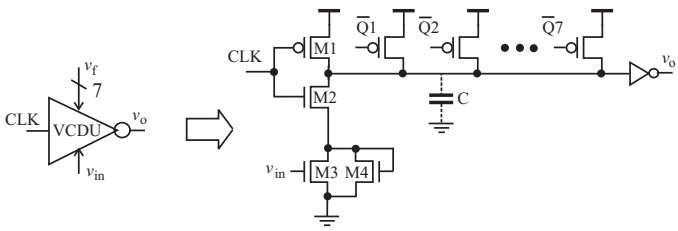


Fig. 6. Negative feedback using current injection. The feedback current injecting PMOS transistors are equally sized.

III. Simulation Results

The proposed time-mode delta sigma ADC has been designed in an IBM 130 nm 1.2V CMOS technology with its layout shown in Fig.7. The pads are laid out as per the probes available to us. Two sets of 3 pads for two RF GSG differential probes (G: ground, S: signal) are placed on the left and right of the chip. One for probing the output of the differentiator and the other for probing the output of the VTC integrator. Static inverter-based voltage buffers are employed for both outputs so as to drive test equipment. The 5 pads at the top of the chip are for VDD and ground, and an external clock of 10 MHz is provided by the bottom pads. The modulator is analyzed using Spectre from Cadence Design Systems with BSIM4 device models. The input of the modulator is a 100 mV 100 kHz sinusoid.

A 8192-point FFT is performed on the output bit stream of the first-order differentiator to obtain the spectrum of

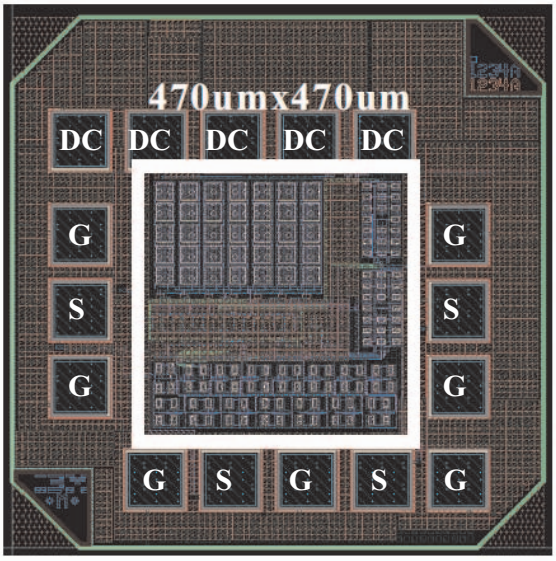


Fig. 7. Layout of proposed all-digital time-mode first-order $\Delta\Sigma$ modulator. GRO has 7 stages. Each stage has a $10pF$ capacitor in order to have 4.4 MHz oscillation frequency. Total silicon area including bonding pads: $1mm$ X $1mm$. The core circuit occupies an area of 470 μm X 470 μm.

the output of the modulator. Fig.8 shows the spectrum of the modulator. Evaluated over 4 MHz bandwidth, the $\Delta\Sigma$ ADC has an SNDR of 47.4 dB and an SFDR of 34.1 dB. Fig. 10 exhibits the dynamic range of the ADC and Fig. compares the FFT plots for different input levels. In Table I, the performances of some recent key time-mode $\Delta\Sigma$ ADCs are compared.

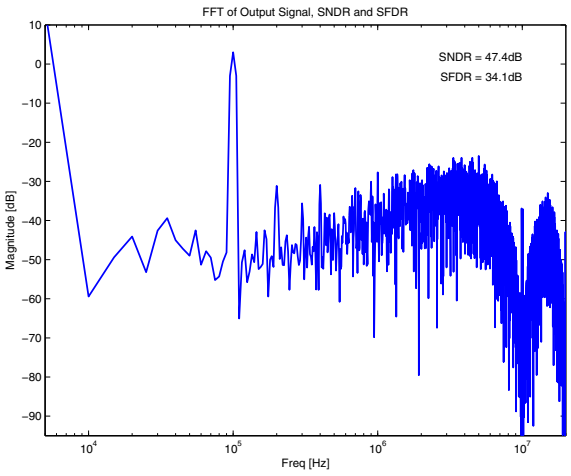


Fig. 8. Simulated spectrum of the one output bit stream (the output of one phase differentiator) of proposed all-digital time-mode first-order $\Delta\Sigma$ ADC.

IV. Conclusions

An all-digital time-mode first-order $\Delta\Sigma$ ADC with 3-bit gated VCO quantizer has been proposed. The $\Delta\Sigma$ ADC consists of a voltage-to-time integrator performing voltage-to-time conversion and feedback subtraction, a 7-stage gated current-starved ring oscillator functioning as a 3-bit quantizer, and a

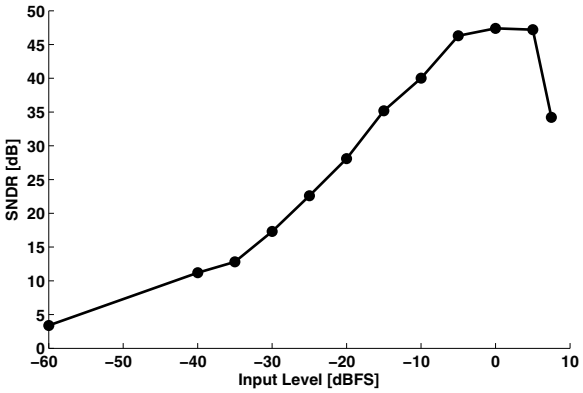


Fig. 9. Simulated dynamic range of proposed all-digital time-mode first-order $\Delta\Sigma$ ADC.

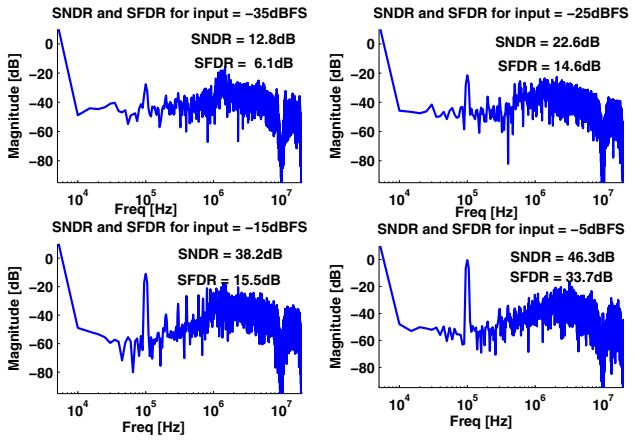


Fig. 10. Simulated spectrum of proposed all-digital time-mode first-order $\Delta\Sigma$ ADC at various input levels.

digital differentiator performing both first-order noise-shaping and frequency feedback. The all-digital implementation of the proposed ADC allows it to scale well with technology so as to benefit from scaling. Implemented in an IBM 0.13 μm 1.2V CMOS technology, the ADC provides 47.4 dB SNDR and 34.1 dB SFDR over 4 MHz bandwidth. The low SNDR of the proposed ADC is due to the absence of a loop filter that can effectively suppress in-band harmonics. Higher order $\Delta\Sigma$ modulators can be readily implemented using digital integrators such as those in [10]. The high noise floor is due to the large quantization noise due to the use of 3-bit quantizer. Quantization noise can be greatly reduced should the GRO contains more stages, for example 31 stages or 5-bit quantizer in [6].

TABLE I

PERFORMANCE COMPARISON OF CLOSED-LOOP TIME-MODE $\Delta\Sigma$ MODULATORS.

Ref.	Tech.	f_s (MHz)	BW (MHz)	SNDR (dB)	Power (mW)
[5]	90 nm	3.4	0.02	44.2	0.44
[6]	0.13μm	950	20	55	38.4
[11]	0.18μm	140	0.4	42.2	0.8
[12]	65 nm	950	20	60	4.5
[14]	0.18μm	128	2	83.9	—
[15]	65 nm	250	20	60	5.66
[16]	90 nm	600	10	78.3	16
This work	130nm	10	4	47.4	1.1

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