NOVEL HIGH-PRECISION CURRENT-MODE MULTIPLIER/DIVIDER

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Key words: reducing MOSFET's second order effects, square-root circuit, squarer/divider circuit, multiplier circuit

ABSTRACT

In this paper, a method to reduce the second order effects on the circuit performances caused by the small sized MOS transistors is proposed and a multiplier/divider circuit is designed using this method. The main advantages of the proposed circuit are reduced errors of the output current function, a smaller area on the chip, possibility of controlling the output current with the control voltage, operation at higher frequencies and more efficient power consumption.

I. INTRODUCTION

It is well known that the decrease in dimensions of MOS transistor in IC fabrication technology affects MOS transistor performance and the MOS transistor voltage-current relationship changes from square-law to linear. Therefore errors may occur in the output current function of the current-mode circuits employing small sized MOS transistors.

In this paper, a method is proposed to reduce the errors generated by the second order effects in the current-mode circuits employing MOS translinear loop, furthermore high-precision multiplier/divider circuit is designed and presented using this method. Analog building blocks such as analog modulator, frequency doubler and etc. can be easily obtained using the proposed multiplier/divider circuit. The output current function of the proposed circuit can be controlled by a control voltage. The proposed method enables the use of much smaller transistors and the circuits to be designed are smaller than their counterparts. Thus they may be operated at much higher frequencies.

The proposed circuit is appropriate to be used for filtering in square-root domain, fuzzy logic controllers, artificial neural networks, modulators, phase discriminators, adaptive filters, RMS-DC converters, sine/cosine synthesizers, cryptography systems etc.

II. CURRENT-MODE MULTIPLIER/DIVIDER CIRCUIT

The multiplication of two signals is one of the most important operations in analog signal processing. Recently several CMOS multipliers have been reported [1-6] and some of them are based on MOS translinear principle.

Translinear circuit principle which was originally formulated for loops of bipolar transistors is generalized and the MOS translinear (MTL) principle is derived by Seevinck [7]. MTL circuits are designed by applying MTL principle and used in synthesizing many nonlinear signal processing functions [8-10]. Square-root circuit and squarer/ divider circuit are two important structures of the MTL circuits. A multiplier/divider circuit can be obtained by using both square-root and squarer/divider circuit as in Figure 1 [11-12].

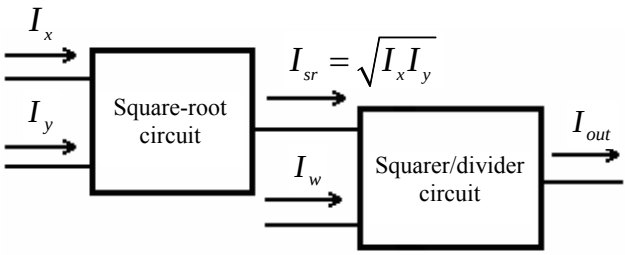


Figure 1. Simplified diagram of the multiplier/divider circuit.

Since I_x and I_y are the input currents of the square-root circuit, the output function of the first circuit can be written as in (1),

$$I_{sr} = \sqrt{I_x I_y} \tag{1}$$

Assuming that this current is the one of the input currents and applying a second I_w to the input, the output current of the whole circuit can be expressed as in (2),

$$I_{out} = \frac{I_{in}^{\,2}}{I_w} = \frac{\left(\sqrt{I_x I_y}\right)^2}{I_w} = \frac{I_x I_y}{I_w} \tag{2}$$

In order to implement a multiplier/divider circuit, square-root and squarer/divider circuits must be designed. Both

square-root circuit and squarer/divider circuit can be obtained by using either the up-down or stacked voltage-translinear (VTL) loops shown in Figures 1a and 1b, respectively.

Figures 2a and 2b show a possible way of designing the square-root and squarer/divider circuit, using stacked VTL loops [13].

Assume that the aspect ratios of the transistors satisfy the $\beta_1=\beta_2=\beta$ and $\beta_3=\beta_4=2\beta$ where β is the transconductance parameter of the MOS transistor, (3) is obtained using the VTL law.

$$V_{GS1}+V_{GS2}=V_{GS3}+V_{GS4} \tag{3}$$

Assuming that the second order effects are negligable, the drain current of a MOS transistor operated in saturation can be expressed:

$$I_D=\frac{1}{2}\mu_o C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2=\frac{\beta}{2}\left(V_{GS}-V_{TH}\right)^2 \tag{4}$$

V_{GS} voltage can be obtained from (4) and substituting this term into (3) assuming V_{TH} threshold voltage for each transistor are the same:

$$\sqrt{\frac{2I_1}{\beta}}+\sqrt{\frac{2I_2}{\beta}}=\sqrt{\frac{2I_3}{2\beta}}+\sqrt{\frac{2I_4}{2\beta}} \tag{5}$$

According to Figure 3, the drain currents of M3 and M4 are the same and taking the square on both sides of (5), the equation can be rewritten as:

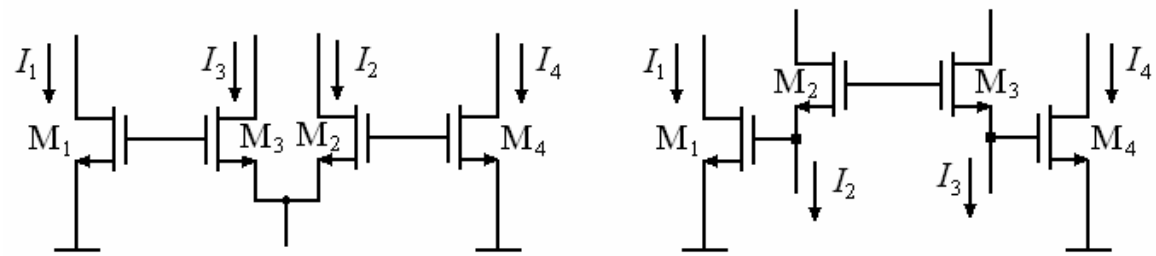
$$I_3=\sqrt{I_1I_2}+\frac{1}{2}\left(I_1+I_2\right) \tag{6}$$

Using the KCL equation at the output node, (7) can be obtained as:

$$I_{out}=I_5=I_3-\frac{1}{2}\left(I_1+I_2\right)=\sqrt{I_1I_2} \tag{7}$$

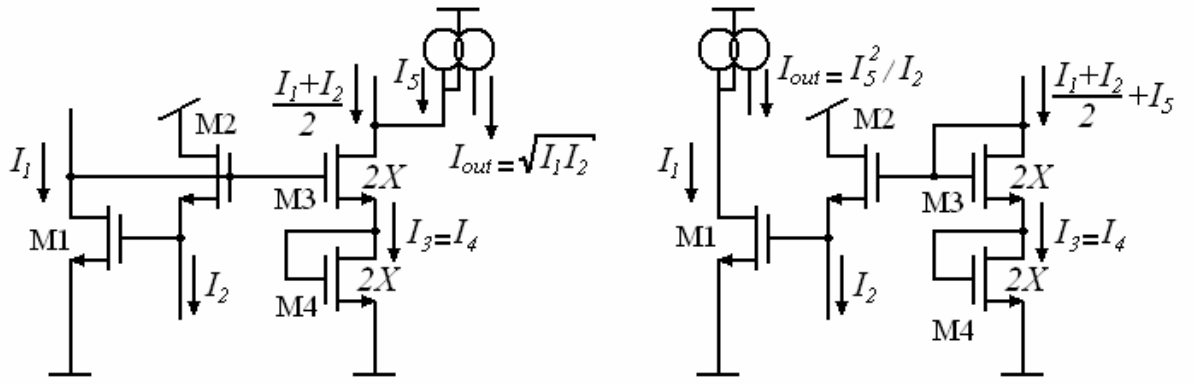
Equation (7) indicates the function of the current-mode square-root circuit.

Hence, a square-root circuit can be obtained if I_1 and I_2 are the input currents and the output current is a copy of I_5. Alternatively, a squarer/divider circuit is obtained if the output is a copy of either I_1 or I_2 and the inputs are the remaining two currents [14-15]



(a) (b)

Figure 2. (a) Up-down VTL loop. (b) Stacked VTL loop.



(a) (b)

Figure 3. Applications of the stacked VTL loop (a) Square-root cell (b) Squarer/divider cell.

III. PROPOSED CURRENT-MODE MULTIPLIER/DIVIDER CIRCUIT

Nowadays, due to the decrease in dimensions of MOS transistors in IC fabrication technologies, second order effects cause more errors in the MOSFET performance. Actually drain current expression includes effects of W, L and V_{DS} on effective threshold, velocity saturation effects, effective mobility dependence on normal field and channel length modulation. Especially, the short-channel effects become more important in MOS transistors at channel lengths of about 1μm or less and require modifications to the MOS models as well as the circuits that are designed using these MOS transistors [16-18].

Due to the second order effects small sized MOS transistors don't operate properly and therefore errors may occur in the output current function of the current-mode circuits employing these transistors. From this point of view, square-root cell and squarer/divider cell which are given in Figure 3 are modified as shown in Figure 4.

The error of the output current function caused by second order effects can be reduced using the resistance R between the gates of the MOS transistors M2, M3 and letting the output current I_{out} flow through this resistance. In this case, a new voltage term that is added to the VTL loop function which eliminates the error of the output current function.

Thus the proposed current-mode multiplier/divider circuit can be realized as shown in Figure 5.

Resistances depicted in Figure 4 are realized with the transistors in Figure 5 and their value can be controlled by the V_C control voltages. By this way output current function of the circuit can be controlled and the function errors of the current can be eliminated.

IV. SIMULATION RESULTS

To verify the proposed circuit, SPICE simulations were performed using TSMC 0.35 μm LEVEL 3 CMOS process parameters. The device dimensions of transistors used in the proposed circuit is shown in Table 1. The power supply voltage is 3V.

Table 1. Transistor dimensions.

	W/L [μm]		W/L [μm]		W/L [μm]		W/L [μm]
Ma1	6/.7	**Ma11**	12/.7	**Mb1**	12/.7	**Mb11**	12/.7
Ma2	6/.7	**Ma12**	12/.7	**Mb2**	12/.7	**Mb12**	12/.7
Ma3	12/.7	**Ma13**	12/.7	**Mb3**	24/.7	**Mb13**	12/.7
Ma4	12/.7	**Ma14**	12/.7	**Mb4**	24/.7	**Mb14**	6/.7
Ma5	12/.7	**Ma15**	12/.7	**Mb5**	12/.7	**Mb15**	12/.7
Ma6	12/.7	**Ma16**	12/.7	**Mb6**	12/.7	**Mb16**	12/.7
Ma7	12/.7	**Ma17**	12/.7	**Mb7**	12/.7	**Mb17**	12/.7
Ma8	12/.7	**Ma18**	12/.7	**Mb8**	12/.7	**Mb18**	12/.7
Ma9	6/.7	**Ma19**	10/.7	**Mb9**	12/.7	**Mb19**	80/.7
Ma10	6/.7			**Mb10**	6/.7		

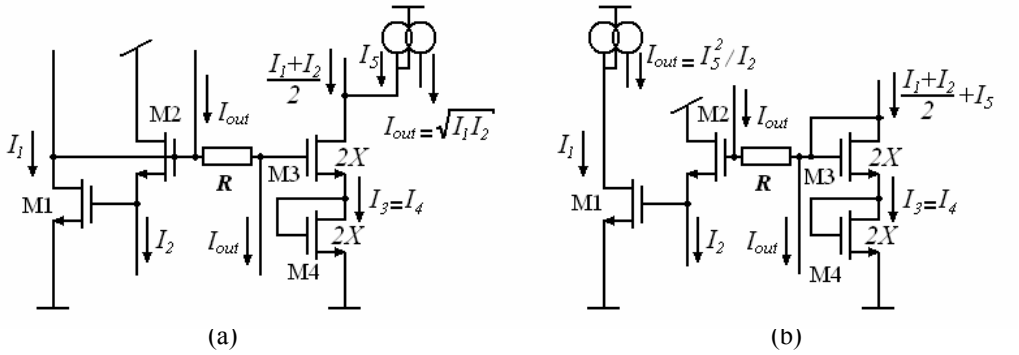


Figure 4. Modified current-mode circuits. (a) Square-root cell. (b) Squarer/divider cell.

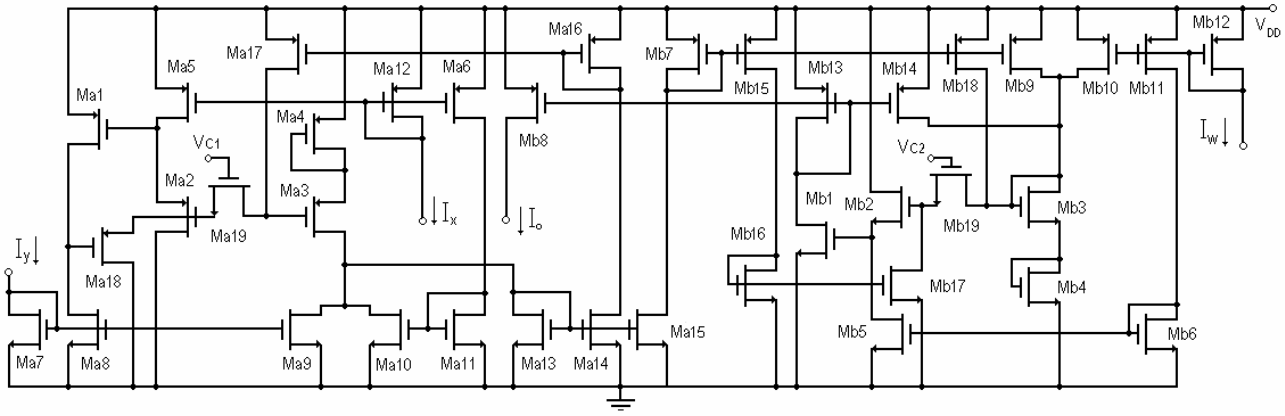


Figure 5. Proposed current-mode multiplier/divider circuit.

To obtain time domain SPICE simulation results of the proposed multiplier/divider circuit, the input current I_x is applied as a triangular wave with an amplitude of 5μA where the other input currents I_y and I_w are constant dc currents with a value of 8μA, as shown in Figure 6. The output currents of the proposed multiplier/divider circuit depicted in Figure 5, the conventional multiplier/divider circuit are observed and simulated with the ideal function as shown in Figure 7. In this simulation V_{C1} and V_{C2} are taken 2.09V and 5V respectively.

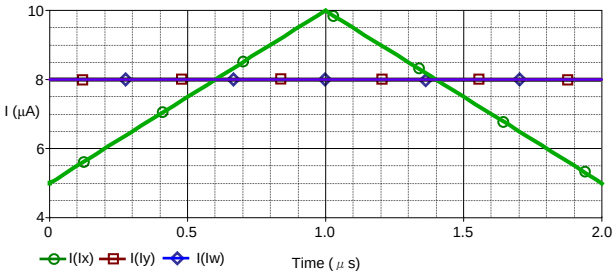


Figure 6. Input currents I_x, I_y and I_w of the proposed multiplier/divider.

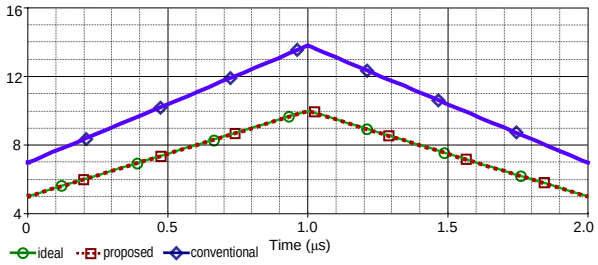


Figure 7. Comparison of the output currents and the ideal curve.

As expected, the characteristic of the output current function of the proposed multiplier/divider circuit shows approximately the ideal current function and the output current function of the conventional circuit is very different from the ideal curve. The output current function of the proposed circuit can be modified by changing V_{C1} and V_{C2} control voltage.

Figure 8 shows the absolute error of the simulated output, i.e., $(I_xI_y/I_w)-I_z$, where the input currents are $I_x=I_y=I_w=5(2+\sin 2\pi ft)$ μA with f=1MHz.

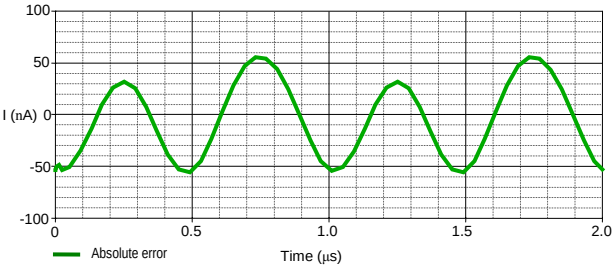


Figure 8. Simulated absolute error of the proposed multiplier/divider.

As shown in Figure 8, the simulated absolute error is less than 0.055μA, thus confirming the high precision of the proposed multiplier/divider circuit.

The small-signal bandwidth measured from the input I_x to the output (with $I_y=I_w=15$μA) is 44MHz as shown in Figure 9.

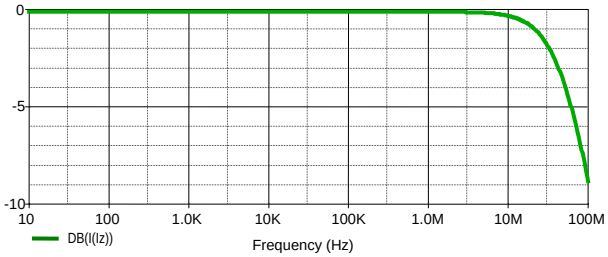


Figure 9. Frequency characteristics of the proposed multiplier/divider.

The DC transfer characteristics of the multiplier/divider circuit are shown in Figure 10. Input currents were $I_w=3$μA, I_y values ranging from 2μA to 10μA in 2μA steps and I_x swept from 0 to 10μA. As expected, the proposed multiplier/divider circuit shows approximately linear characteristics.

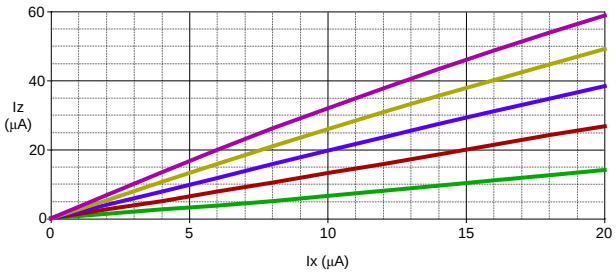


Figure 10. Simulated DC transfer characteristics of the multiplier/divider.

Figure 11 and Figure 12 shows the use of the multiplier as an analog amplitude modulator. Input currents are taken as $I_x=5(1+\sin 2\pi ft)$ μA with f=0.2MHz, $I_y=5(1+\sin 2\pi ft)$ μA with f=2MHz and I_w is taken as a fix current of 5μA as shown in Figure 11.

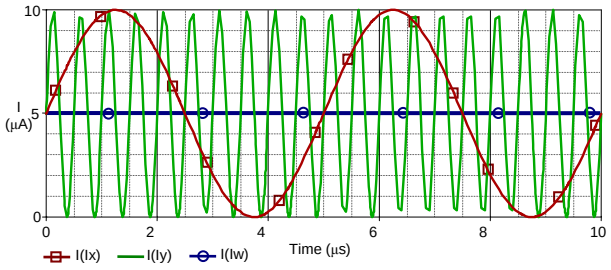


Figure 11. Input currnets of the multiplier/divider as an amplitude modulator.

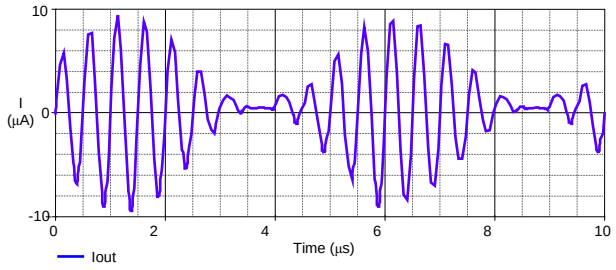


Figure 12. Modulated ac output current of the multiplier/ divider as an amplitude modulator.

The main parameters of the proposed multiplier/divider circuit are shown in Table 2.

Table 2. Performance parameters of the proposed circuit.

Parameter	Value
Technology	0.35 μm CMOS
Supply voltage	3 V
THD (input: 10 μA_{pp} at 1 MHz.)	0.144 %
BW (simulated)	44 MHz.
Area	0.01 mm^2
Power consumption (10 μA DC inputs)	0.538 mW

V. CONCLUSION

In this paper, a method which reduces the errors generated by the second order effects in the current-mode circuits using MOS translinear loop is proposed, also high-precision multiplier/divider circuit is designed using this method. It presents interesting features such as very small area, power efficiency and precision. Hence, it is shown that proposed multiplier/divider circuit is suitable for fuzzy logic controllers, artificial neural networks, modulators, phase discriminators, adaptive filters, cryptography systems, RMS-DC converters, sine/cosine synthesizers etc.

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