# Analysis of Shunt Active Power Filters Using PSCAD for Parallel Operation

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## Abstract

**The modularity of shunt active power filters (APF) is considered to be the most advantageous feature that allows parallel operation of a number of modules. From the viewpoint of reliability, flexibility, and efficiency, modular filtering approach is quite appropriate for high power applications. This configuration allows various control schemes to be employed, namely power and frequency splitting and capacity limitation control. In this paper, these configurations and methods for parallel operation of APFs will be analyzed in PSCAD and results will be discussed.**

## 1. Introduction

The power rating and switching frequency of active power filter (APF) converters are determined by the magnitude of harmonic currents and required filter bandwidth. In high power applications, filtering task cannot be performed for the whole spectrum of harmonics by using a single converter due to limitations on switching frequency and power rating of the semiconductor devices [1]. These limitations on the converter power rating and bandwidth affect the filtering performance as a result. The solutions suggested in the literature to this typical design problem of APFs are hybrid configuration, which reduces converter power rating; step-down transformer, which usually increases the cost; series or parallel connection of switching devices, which results in more complex gate drives; multilevel inverter, which reduces voltage rating of the switches; or splitting filtering on spectrum range among a number of APF [2-6].

The modular structure of shunt APF is the most advantageous feature of them. This feature allows parallel operation of number of modules to increase the kVA rating. Such an operation is also suitable especially when APFs are located in power distribution systems from the viewpoint of reliability, flexibility, and efficiency. In parallel operation of APFs; any fault in one or more APF modules is not expected to degrade the operation of whole system since other modules can tolerate it, hence system is fault tolerant and more reliable. Also, expansion capability of the APFs is an important factor depending on the increase of the harmonic polluting loads connected to the distribution system. In addition, APFs can be operated not only for harmonic compensation but also for other disturbances such as current imbalance and reactive power compensation. Finally; APFs can be optimized to minimize the switching losses as well as the total harmonic distortion of the supply currents. Because of these reasons, modular filtering approach is quite appropriate for high power applications.

The control techniques used in parallel connection can be classified in three major categories. These are power splitting, frequency splitting, capacity limitation techniques [1,7-10]. Of these methods, power and frequency splitting method requires detection of the load harmonic content and sharing the compensation currents among APF modules via a central controller. As an alternative to this approach, in a master/slave controller scheme, each APF has its own current sensor to obtain load current harmonics and master module shares the compensation currents among others [11]. The capacity limitation method aims independent operation of each APF module and provides a practical solution to power capacity enlargement problems.

In APF applications, the research has mainly concentrated on voltage-source active filters, while the current-source active power filters are preferred in some applications due to their fast response as an alternative. Both configurations can be implemented for effective compensation of current harmonics injected by the load or source. The main drawbacks of the voltage source APF is the switching ripple in the source current, while the current source APF has bulk and heavy dc link inductor with high power loss [12]. In this paper, the voltage source APF is considered and the reference current to the APF is obtained by using Fast Fourier Transform (FFT). The configurations and suggested methods for the parallel operation of APFs are analyzed in PSCAD and results will be discussed.

## 2. APF Control Schemes for Parallel Operation

In high power applications, the APFs are usually connected in parallel. There are mainly three types of techniques for parallel operation in practice. These techniques are based on power splitting, frequency splitting and capacity limitation on each module, which are summarized as follows:

### 2.1 Power Splitting Approach

In this approach, $N$ identical converter modules are connected in parallel and the compensating harmonic current is equally shared among these converters ($I_{Lh}/N$) as shown in Fig.1. This approach is also known as load current distributing approach or scheme of distributed control [7-8]. The advantage of this approach is its easiness for implementation and maintenance. The disadvantage is that any fault on the control signal bus may shut down the whole system, since it requires control interconnection among APFs for equally distributing the required compensating load current [8]. A central control scheme shares the total compensation currents equally among the APFs. Each APF can also be designed with its own harmonic detection and processing unit, that would eliminate dependency on single and reliable central control unit.

### 2.2 Frequency Splitting Approach

The block scheme that represents the operation of this method is shown in Fig.2. In this method, each APF is assigned to compensate a specific harmonic component of a nonlinear load. Since the harmonic current magnitudes of the nonlinear loads are inversely proportional to the harmonic order, the APF module that compensates the higher order harmonics have lower power rating and higher switching frequency, and vice versa. The switching losses of each converter are equal if the power-switching frequency product is kept constant. The main disadvantage of this scheme is that the APF modules are not identical and can be replaced only by a similar module [1]. Since a central control scheme that extracts load harmonic components and distributes to APF modules is required in this method, any fault on the current control signal will yield the whole system to shut down as mentioned in previous scheme.

## 2.3 Capacity Limitation Control

In this method, each APF module injects the harmonic and/or reactive compensation current to the electrical network with limited amplitude by its own power rating [8]. As shown in Fig.3, the APF modules are distributed along the power network and each APF detects the currents at the upstream of the node, where the previous APF nearer to the load is connected. Each APF nearer to the electrical supply treats the previous APFs as on its load side and compensate the remaining part of currents. The compensated current may be at limited amplitude depending on converter's capacity. Hence, the total harmonic current and/or reactive power is shared among the APFs. In this scheme, the APF modules are not necessarily to be identical, since each module is operated independently, therefore, allowing power capacity enlargement to be made easier. Also, there is no central control scheme that shares the total compensation currents among the APFs and as a result the APF system becomes more reliable. However, the dynamic characteristic of this method is poor [11].

## 3. Simulation Results

Simulations for the parallel operation of APF modules are performed by using the PSCAD package program. A three-phase diode bridge rectifier with resistive load has been used as a non-linear load. The current control loops of the APF modules contain hysteresis controller. Each APF has a switching ripple filter on its supply side and dc link PI controller. The system parameters are summarized in Table 1. In simulations, harmonic compensation of the load is performed by using single-converter and multiple-converter approaches and their performances are compared. The schemes given in Fig.1-3 are constructed in PSCAD package program for single-converter (N=1) and multiple-converter (N=2) approaches.

## 3.1 Single-Converter Approach

When a single converter unit is implemented, the power rating of the converter can be specified by defining the constraint on total harmonic distortion or specific harmonic compensation of supply current.

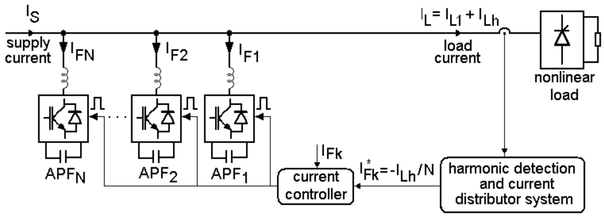


**Fig. 1.** Power splitting scheme consisting of identical APF modules

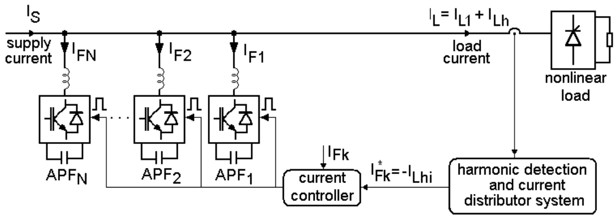


**Fig. 2.** Frequency splitting scheme consisting of APF modules with different power rating and switching frequency

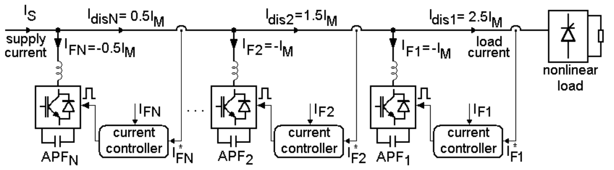


**Fig. 3.** Current sensing and capacity limitation control of multi-module cascaded APFs

**Table 1.** System Parameters

| | |
|---|---|
| Supply voltage (V, rms, line-to-line) | 380 V |
| Supply frequency (fs) | 50 Hz |
| Supply resistance (Rs) | 0.001 ohm |
| Supply inductance (Ls) | 0.1 mH |
| Diode rectifier load (10kW) resistance ($R_L$) | 25 ohms |
| APF inductance ($L_F$) | 1.8 mH |
| APF resistance of inductance ($R_F$) | 0.1ohm |
| APF dc link capacitor ($C_f$) | 2.35 mF |
| APF dc link reference voltage ($u_{dc}$*) | 650 V |
| APF hysteresis current controller bandwidth (HBW) | 0.2A |
| APF dc link voltage PI controller parameters | $K_P$=0.1<br>$T_I$=0.01s |
| Switching Ripple Filter Parameters | L=0.25mH<br>C=30 uF<br>$R_d$=3 sohm |

### 3.1.1 Total Harmonic Distortion (THD) Approach

In this method, PAPF reference currents are generated such that they compensate the whole harmonic components in the load currents. The fundamental components of the load currents are obtained by FFT method and multiplied by reference sine waveforms, which are obtained via PLL circuit that tracks the supply voltages. Hence, the required compensation currents are simply obtained by subtracting these fundamental current waveforms from the actual load current as follows:

$$i^*_{FC,i} = i_{L,i} - i_{Lh1,i} \qquad (1)$$

where $i$=$a,b,c$, and $i_{FC}$, $i_L$, and $i_{Lh1}$ are the PAPF reference compensation current, load current, and fundamental load current of each phase, respectively.

The waveforms of supply voltages, supply currents, APF current, load current, and APF dc link voltage at steady-state after APF begins to compensate the harmonics of a 10kW load at t=0.5s are shown in Fig.4a. The dc link voltage of the APF is almost kept constant at 650V with a peak-to-peak ripple voltage of approximately 1V. The reference currents are updated at a sampling rate of 10kHz considering the execution time for the process in real system. At this sampling rate, the total harmonic distortion (THD) is decreased from %29 to %11.4 after compensation. While calculating the THD, harmonic components of the supply currents upto 31$^{st}$ have been taken into account.

Since APF acts to compensate the whole harmonic content except the fundamental, reference current waveforms contain higher order harmonics. The current injected by the APF cannot track the reference current in a strict hysteresis band. Reducing HBW or decreasing the value of the filter inductance causes the switching frequency of IGBTs increase substantially. Also, the magnitude of the filter current has effect on the switching frequency due to hysteresis controller. Hence, the waveform tracking performance of the APF degrades due to increasing switching frequency and as a result THD increases.

The notches appear in the supply current waveform during commutation instants of the diode rectifier. It is seen that the APF currents are unable to track the quick variations. The reason that the supply current waveforms contain notches as shown in Fig.4b is the APF's current tracking error. It must be noted that the value of the supply reactance is taken as a small value in simulations. In practice, the notches in the supply currents are also affected by the magnitude of source reactance.

### 3.1.2. Specific Harmonic Elimination Approach

In this method, compensation of specific harmonics that the load current contains is aimed. The amplitude and phase information of specific harmonic components of the load currents are obtained by FFT method. A PLL circuit is used to obtain the phase information of the supply voltages. The reference compensation currents are obtained as follows:

$$i^*_{FC,i} = -\sum_h i_{Lh,i} \tag{2}$$

where $i=a,b,c$, and $i_{FC}$ and $i_{Lh}$ are the PAPF reference compensation current and specific harmonic component of the load current for one phase, respectively.

In simulations, APF is assigned for the compensation of 5$^{th}$, 7$^{th}$, 11$^{th}$, and 13$^{th}$ harmonics. The waveforms of supply voltages, supply currents, APF current, load current, and APF dc link voltage at steady-state after compensation are shown in Fig.4b. The dc link voltage of the APF is almost kept constant at 650V with a peak-to-peak ripple voltage of 4 V. THD value is decreased from %29 to %11.7 after compensation of 10kW diode rectifier load current harmonics.

### 3.2 Multiple Converter Approach

In this part, the methods of power splitting and frequency splitting are examined. Each converter is employed for predefined harmonic compensation or power sharing. In this simulation, two APFs are connected in parallel for the load.

### 3.2.1 Power Splitting Approach

In this method, reference compensation currents are generated in the same way as mentioned for single converter approach. This calculated reference current is divided by the number of APF modules and shared to APF modules equally as follows:

$$i^*_{FCk,i} = \frac{i_{L,i} - i_{Lh1,i}}{N} \tag{3}$$

where $i=a,b,c$, and $k=1,\ldots,N$ is the number of APF module. Simulations are performed with N=2 parallel APFs. The waveforms of supply voltages, supply currents, load current, and APF currents at steady-state after APFs begin to compensate the harmonics of a 10kW load at t=0.5s are shown in Fig.5a. THD value is decreased from 29% to 10.2%, which is slightly better than the one obtained from single-converter approach.

### 3.2.2 Frequency Splitting Approach

In this method, the waveforms of specific harmonic components of the load current are generated in the same way as mentioned in single converter approach. The required compensation current consisting of specific harmonic components is shared among the APF modules. In simulations, two APF modules are used; the APF1 is assigned to compensate 5$^{th}$ and 7$^{th}$ harmonics, while APF2 compensates 11$^{th}$ and 13$^{th}$ harmonics. The waveforms of supply voltages, supply currents, load current, and APF currents at steady-state after APFs begin to compensate the harmonics of a 10kW load at t=0.5s are shown in Fig.5b. The THD value of the supply current is decreased from 29% to 11.6% after both APFs compensates in simulations. The THD performance of this configuration is almost the same as the result obtained from single-converter specific harmonic elimination approach.

### 3.2.3. Capacity Limitation Control

In this method, reference compensation currents are generated in the same way as mentioned in single-converter approach. The peak value of the compensation currents is limited according to the current limit of each APF module. In order to limit the compensation currents in PSCAD simulations, the rms value of the reference compensation current is calculated first. The power rating of each APF module is determined by the following formula [6]:

$$P = \sqrt{3}\,\frac{V_{dc}}{\sqrt{2}}\,\frac{I_{F\,max}}{\sqrt{2}} \tag{4}$$

where $V_{dc}$ is the dc link voltage value and $I_{Fmax}$ is the peak value of the compensation currents. Under regulated dc link voltage conditions, the capacity of each APF module is determined by the peak (or rms) filter current. Hence, a gain factor for each APF, which represents the fraction of APF capacity, is calculated as follows:

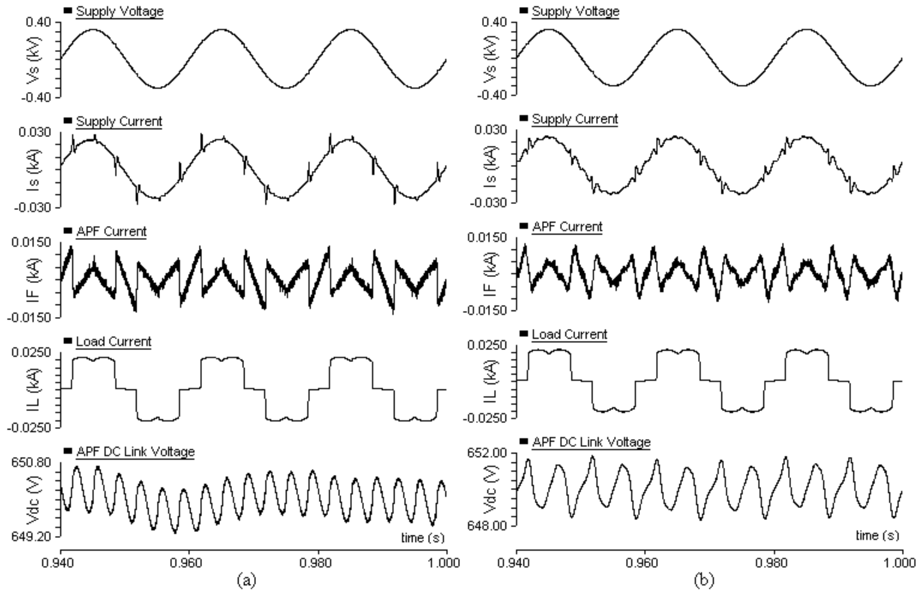


**Fig. 4.** Simulation results obtained from single-converter at steady-state a) THD approach b) specific harmonic elimination approach

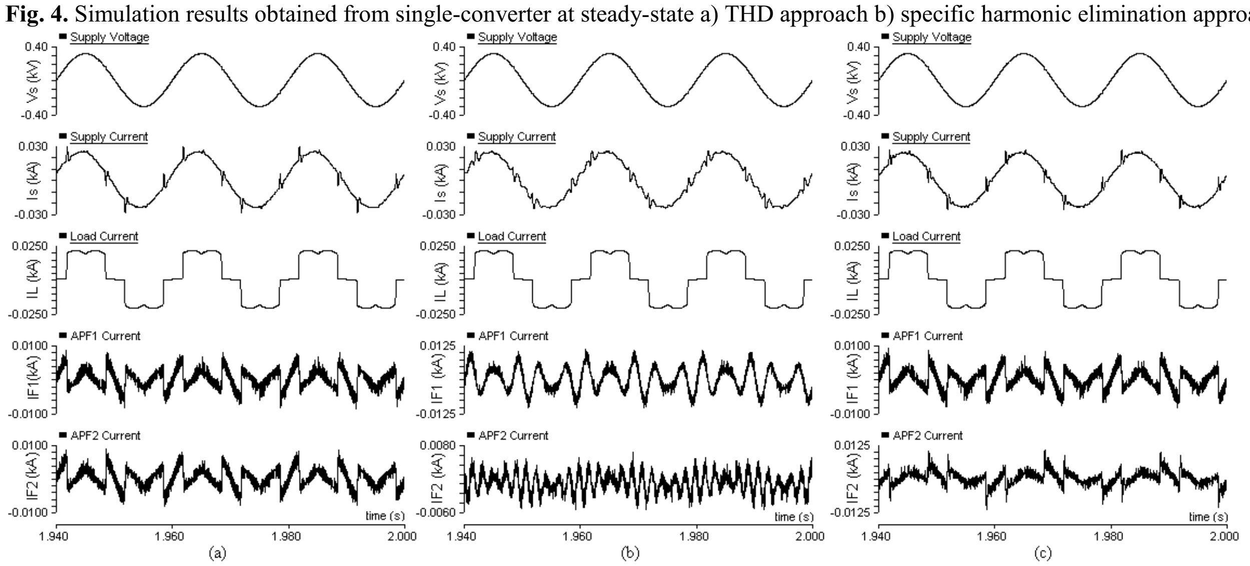


**Fig. 5.** Simulation results obtained from multiple-converter at steady-state a) power-splitting approach b) frequency-splitting approach c) capacity- limitation control approach

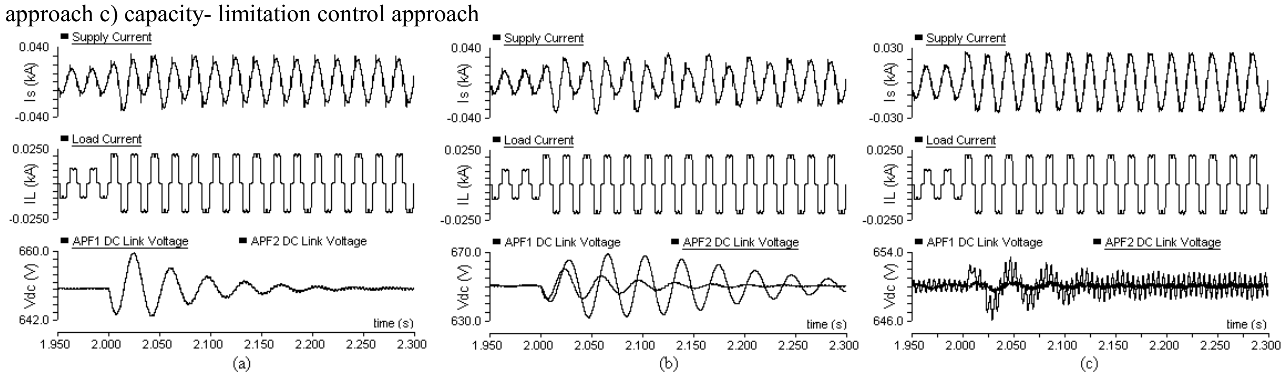


**Fig. 6.** Responses of the multiple-converter APF systems to a step load change a) power-splitting approach b) frequency-splitting approach c) capacity- limitation control approach

$$I_{Fk,\,gain} = \begin{cases} 1, & I_{FCk} \le I_{Fkmax,\,rms} \\ \dfrac{I_{Fk\,max,\,rms}}{I_{FCk}}, & I_{FCk} > I_{Fkmax,\,rms} \end{cases} \quad (5)$$

where, $I_{Fkmax,rms}$ represents the rms current limit of k$^{th}$ APF and $I_{FCk}$ is the rms value of the calculated reference compensation current.

In simulations, the rms current limit of each APF is chosen to be 2.5A. In Fig.5c, the waveforms of supply voltages and currents, the current waveforms on the APF2 load side, and APF compensation currents are shown at steady-state. THD value is decreased from 29% to 7.3%, which is slightly better than the one obtained from multiple-converter power-splitting approach.

For THD approach of single-converter and 10kW diode rectifier load, the peak value of the filter reference currents is approximately 10.7A (excluding the amount of fundamental current that is required for APF operation). Due to tracking error of APF, instantaneous filter currents may become higher than this value, which means required APF power rating is somewhat higher. For single-converter specific harmonic elimination approach, the peak value of the filter reference currents is approximately 9.4A (excluding the amount of fundamental current that is required for APF operation). For power splitting approach with multiple-converter, the peak values of the reference currents of both APF converters are at the half value of the single-converter. For frequency splitting approach with multiple-converter, the peak values of the reference currents of APF1 and APF2 are 7.4A and 3.2A, respectively. For multiple-converter capacity limitation control, the peak value of the reference currents of APF1 and APF2 are calculated as 6A and 10A in simulations, respectively. Although the rms compensating currents are limited such that both APFs almost equally share the compensating currents, the instantaneous filter current of APF2 is higher than that of APF1 in capacity-limitation control method. This is because of the supply currents' containing high frequency components that APF1 cannot properly compensate during diode rectifier commutation instants. As a result, the actual VA capacity of the APF2 is increased.

The performances of multiple-converter APF systems were also tested against a step load change from 5kW to 10kW at t=2s. The simulation results for three multiple-converter aproaches are shown in Fig.6, which includes the variations of supply current, load current, and APF dc link voltages. The specific harmonic elmination with frequency-splitting method gives the fastest transient response, while the capacity limitation is the slowest.

## 4. Conclusion

When the power ratings of the converters are considered for the compensation of diode rectifier load current harmonics, it can be seen that the total VA rating of the installed APFs are highest in multiple-converter capacity limitation control approach and lowest in single-converter specific harmonic elimination approach. Simulation results show that the multiple-converter power-splitting and capacity limitation control methods give the best THD performance in the suppression of the lower order dominant harmonics. Single-converter specific harmonic elimination and frequency-splitting methods give almost the same performance, however, since the peak amplitude of the sum of harmonics is lower than that of an individual harmonic, assigning an APF for the compensation of only one harmonic is not effective and this yields to a larger total APF VA rating. The THD performance of single-converter THD method worsens as the nonlinear load increases, because of the increase in required switching frequency of the converter. When the compensating currents are shared as shown in multiple-converter power-splitting approach, the THD performance of the system is observed to improve. The actual VA capacity of the forthcoming APFs is increased due to insufficient compensation of the previous APF modules in capacity-limitation technique, if the modular system is subjected to compensate high frequency components in the load currents such as in the case analyzed with a diode rectifier feeding a resistive load.

## Acknowledgment

This work was carried out as a part of project, "Power Quality National Projects", sponsored by Turkish Scientific and Research Council and Turkish Electrical Power Transmission Co. (TEİAŞ) under contract 106G012.

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