A HIGH QUALITY MULTI-LEVEL VSI SUITABLE FOR HIGH POWER/ HIGH VOLTAGE APPLICATIONS

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Abstract

In this paper a new magnitudes for dc side capacitors of a Multi Level Voltage Source Inverter (MLVSI) is used. These magnitudes of dc side capacitors makes it possible to produce $\sum_{k=0}^{N} 3^k$ steps ac output voltage by cascade connection of only N single phase full bridge inverter (FBI) which results in a very better output voltage waveshape compared with previous works. On the other hand, using approximated equal area pulse amplitude modulation (AEAPAM) technique to calculate the duration of each step of voltage not only has reduced the complexity of control circuit considrably but also has resulted in an almost sinusoidal output voltage waveform. A simple closed-loop controller to control the capacitors voltages is developed. Application of such an inverter for feeding a R-L load is studied using PSCAD/EMTDC program too.

Key Words Multi Level Voltage Source Inverter (MLVSI), Approximated Equal Area PWM

I. INTRODUCTION

New families of semiconductors have reached considerable levels of power ratings but their operation at very high power applications unless using series/parallel connection of them is impossible yet. series/parallel connection of these devices confirms to well known problems such as non uniform grading of voltage across, and current through them. On the other hand, the switching frequency of semiconductors at high power applicati ons is limitted too.

Up-mentioned subjects causes to serious problems in produsing of high quality output voltage and/or current waveshapes at high power applications. For some years, current source inverters were the most suitable way for dc/ac conversion at high power applications. But these converters usually produces notable distortions of voltage and current and have not good dynamic performances.

Recently, differnt power circuits are presented for MLVSIs that make it possible to reach really high power, very good quality of output waveshape and acceptable dynamic performance [1-3]. Principle of operation of these MLVSIs usualy is based on synthesize the desired output voltage from several steps of voltages typically obtained from dc side capacitors voltages. In this way, it is obvious that with more steps of voltages it is possible to produce bettre quality output voltage.

This paper presents a cascade connection of single phase full bridge inverter (FBI) units that can produce more steps of voltages compared with the previous works [4,5]. This is achieved by more suitable selection of dc capacitors sizes. This MLVSI eliminates excessively large number of bulky transformers required by conventional multi-pulse inverters and does not require voltage balance circuits or voltage matching of the switching devices too. Cascade connection of single phase FBI units reduces the rating of them and the MLVSI may operate at high voltages and power ratings by elimination of output transformer.

II. PROPOSED POWER CIRCUIT OF MULTI-LEVEL VSI (MLVSI)

Fig. 1 shows the single phase configuration of the proposed MLVSI with three number of dc sources (N=3). The power circuit consists of cascade connection of single phase FBIs. The voltages of dc sources is ordered at the power of three, i.e. 1, 3, 9 , 27, etc. In this way with N number of dc sources it is possible to generate $\sum_{k=0}^{N} 3^k$ step output voltage. This MLVSI does not require any clamping diodes or flying capacitors.

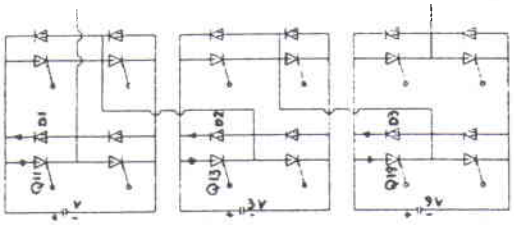


Figure 1. *The Single Phase Power Circuit Topology*

Fig. 2 shows the ability of presented circuit in producing the levels of output voltage compared with [4] and [5]. The power circuit in [4] and [5] are similar to fig. 1, but in [4] the dc side capacitors voltages are considered equal to each other and in [5] they are at the power of two.

This figure shows the considrable superiority of proposed method of capacitors voltage selection compared with the previous works.

In designing of MLVSIs, usually the voltages of dc side capacitors are kept constant by control circuit. This fact causes to decreasing of quality in low values of output voltage because of fewer number of accessible levels at these values.

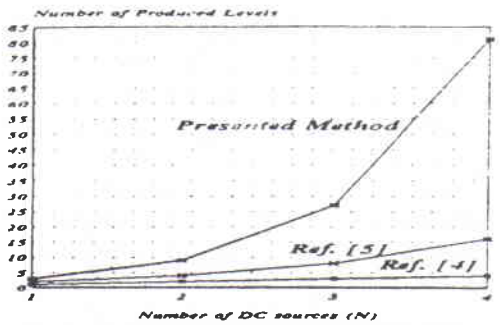


Figure 2. *Comparision of Generated Levels*

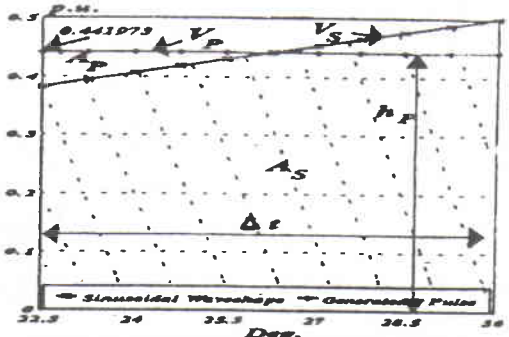


Figure 4. *Explanation of AEAPAM method*

Fig. 3 shows a quarter of output voltage waveshape of presented MLVSI with N=3 for two different magnitudes of this voltage. In this figure the sinusoidal waveshapes are references and stepped waveshapes are produced output voltages by MLVSI. This figure shows the better quality of output voltage at higher magnitudes. It is obvious that more available levels can better overcome this problem and this is another reason for producing as more levels number as possible in MLVSIs.

III. APPROXIMATED EQUAL AREA PULSE AMPLITUDE MODULATION (AEAPAM) METOHOD

Apart from the numbers of available levels, the duration of each step is an important factor in the quality of output waveshape and reducing the THD and DF. One fourth symmetry of sinusoidal waveshape makes it possible to compute the duration of each level only at a quarter of a period. Mathematical methods for completly elimination or minimization of harmonics and control of fundamental harmonic, confirms to simultaneous solving of large number of non-linear equations. Solving of up mentioned equations specially at large number of controlled harmonics is time consuming, difficult to do and in some cases impossible because of divergence problem or convergence to wrong values. Meanwhile, from the practical point of view the smallest deviation from the computed values, generates undesired harmonics and the method would be useless.

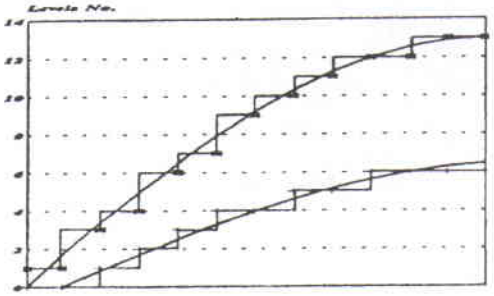


Figure 3. *Controlling the magnitude of a sinusoidal waveshape with a MLVSI at a quarter of a period*

A simple method for computation of the duration of each step is approximated equal area pulse amplitude modulation (AEAPAM) method [6,7]. In this method each 30 degree of ouput three phase sinusoidal voltage divides to equal time intervals, then in each interval the area under the waveshape calculates, now it is enought to produce a pulse with equal area in that interval. Fig. 4 shows such an interval with a segment of output voltage (V_s) and the equal area pulse (V_p). In this figure h_p is the heigh of produced pulse, A_s is the area under the output voltage waveshape and A_p is the area under the produced pulse. The number of intervals in each 30 degree determines the duration of interval (Δt).

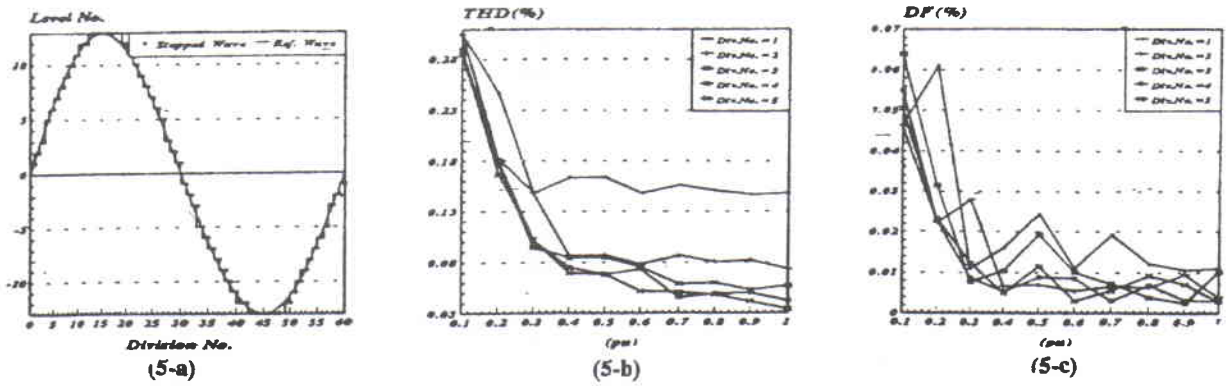
In this way it is possible to compute the h_p by following equation in a very simple manner.

$$h_p = A_s / \Delta t \qquad (1)$$

Unfortunatly, the number of accessible levels is limited and it is usually impossible to produce exactly the condition of $A_p = A_s$. According to AEAPAM method, the computed magnitude of hp (by eq. 1.) modifies to the closest available level. Fig. (5-a) shows a sinusoidal waveshape with N=3 which is produced by this method. In this figure the number of divisions in each 30 degree (Div. No.) is equal with five. Fig.s (5-b) and (5-c) show the variation of THD and DF versus the magnitude of fundamental harmonic respectively. These figures show that the quality of output waveshape decreases at low magnitudes of voltage that is because of decreasing the number of accessible levels. The increasing of Div. No. (that is the parameter of figures) increases the quality of output waveshape. Fig.s (6-a), (6-b) and (6-c) show the operation of inverter for Div. No. equals with five and N=4. Comparition of Fig. (5-b) with Fig. (6-b) and Fig. (5-c) with Fig. (6-c) show that the increasing of N, increases the quality of output waveshape. In addition, the quality of output waveshape with N=4 remains almost fix in a wider range relation to the case of N=3.

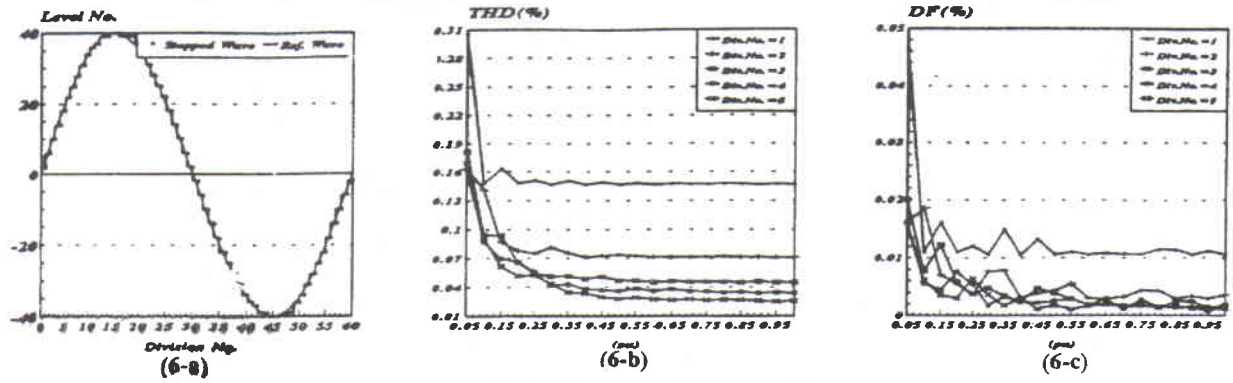
IV. HARMONIC ANALYSIS

Harmonic content of the inverter output voltage can be obtained from the fourier analysis. Fig. 7 shows a generalized stepped waveform. For equally steps with no dewell at zero voltage, i. e. $\theta_1=0$, output voltage is given by:



(5-a) (5-b) (5-c)

Figure 5. Stepped output voltage using AEAPAM and its THD and DF vs. the fundamental harmonic



(6-a) (6-b) (6-c)

Figure 6. Stepped output voltage using AEAPAM and its THD and DF vs. the fundamental harmonic

$$v(t) = 4/\pi \sum_{n=odd} \sum_{k=1}^{p} [V_k \cos((k-1)n\theta)] \sin(n\theta)/n \quad (2)$$

where $\theta=\pi/2p$ and $V_k=2\ V_1*\cos((k-1)\theta)$ and $p=3*$(Div. No.). For equally steps with dewell at zero the output voltage is given by:

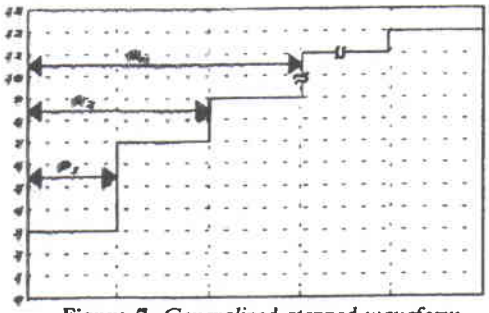


Figure 7. *Generalized stepped waveform*

$$v(t) = 4/\pi \sum_{n=odd} \sum_{k=1}^{p} [V_k \cos((2k-1)n\theta)] \sin(n\theta)/n \quad (3)$$

where $\theta=\pi$ / 2p and $V_k=2\ V_1*\cos(\theta_k)/\cos(\theta_1)$

V. COMPUTATION OF CAPACITORS

The dc side capacitors are sized such that the voltage ripple on the dc bus is within acceptable limits. The values of individual capacitance C_i can be calculated as:

$$C_i = \frac{\Delta q_i}{\Delta V_{Ci}} = \frac{\Delta q_i}{V_{Ci,max} - V_{Ci,min}} = \frac{\Delta q_i}{2\,\epsilon\, V_{Ci}} \quad (4)$$

where Δq_i is the deviation in the charge on the capacitor which depends upon the capacitor current waveform, V_{Ci} is the average capacitor voltage, and ϵ is the regulation factor of capacitor voltage. The value of ϵ may range from 5 - 20% for practical use. V_{Ci} and ϵ are defined as:

$$V_{Ci} = \frac{V_{Ci,max} + V_{Ci,min}}{2} \quad (5)$$

$$\epsilon = \frac{V_{Ci,max} - V_{Ci,min}}{2V_{Ci}} \quad (6)$$

The deviation in the charge on any capacitor can be formulated as:

$$\Delta q_i = \int_{\theta_i}^{T/4} \sqrt{2}\, I\, \cos(\omega t)\, dt \quad (7)$$

where I is the rated rms phase current of the inverter and T is one cycle time period. From (4) and (7)

$$C_i = \frac{1}{2\,\epsilon\, V_{Ci}} \int_{\theta_i}^{T/4} \sqrt{2}\, I\, \cos(\omega t)\, dt \quad (8)$$

Using (7) the capacitance values of the MLVSI shown in Fig. 1 are calculated as:

$$C_1 = \frac{\sqrt{2}\, I}{2\,\omega\,\epsilon\, V_{dc}} [1 - \sin\theta_1 + \sin\theta_2 - \sin\theta_3 + \sin\theta_4 - \sin\theta_5 + \sin\theta_6 - \sin\theta_7] \quad (9)$$

$$C_2 = \frac{\sqrt{2}\, I}{4\,\omega\,\epsilon\, V_{dc}} [1 - \sin\theta_2 + \sin\theta_4 - \sin\theta_6] \quad (10)$$

$$C_3 = \frac{\sqrt{2}\, I}{8\,\omega\,\epsilon\, V_{dc}} [1 - \sin\theta_4] \quad (11)$$

VI. CAPACITOR VOLTAGE CONTROL

According to the symmetry of sinusoidal waveshape, the operation of each individual single phase is in such a way that the average charge to its dc capacitor over every half cycle is equal to zero and the dc voltage on all of the capacitors remain theoritically balanced. However, due to the power losses in the inverter and an unbalanced operation of the three-phase system, the cpacitor voltages may drift away from their set values.

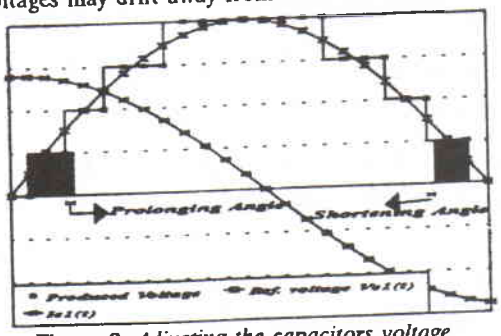


Figure 8. *Adjusting the capacitors voltage*

To keep the voltage of dc capacitors at specified magnitude, it is possible to prolonging or shortening the current flow through them. In this way, it is possible to regulate the voltages of dc capacitors by the source. This causes to absorbing or injecting a small amount of active power by or from the capacitors. The sum of necessary active power in each phase may be obtained by phase shifting of switching pattern relation to the source voltage Fig. 8 shows the method of increasing the dc voltage of capacitor C_1 by prolonging of switching duration at positive and shortening it at negative values of the current flow through C_1. In this figure $i_{C1}(t)$ is the current passing through C_1, $V_{C1}(t)$ is the generated voltage by single phase bridge of C_1 and $\Delta\theta_1$ is the necessary regulating phase angle. The summery of control scheme is illustrated in table 1.

Table 1. *Summery of control scheme*

$V_{C1}(t)$	$i_{C1}(t)$	$\Delta\theta_1$
+	+	Prolonging
+	–	Shortening
–	+	Shortening
–	–	Prolonging

Fig. 9 shows the voltage control circuit of capacitor C_1. In this figure the phase angle $\Delta\theta_1$ is used to prolong or shorten the conduction time of capacitor C_1 by shifting of switching patterns.

The sign of $\Delta\theta_1$ is according with table 1 and its magnitude is propotional with Δv_{c1}. The output of comparator is only high (as +1) or low (as -1). Similar control circuits are used for each of capacitors.

VII. SIMULATION RESULTS

The operation of three-phase MLVSI with N=3 (27 stepped output voltage) is evaluated using PSCAD/EMTDC. The MLVSI connects to a

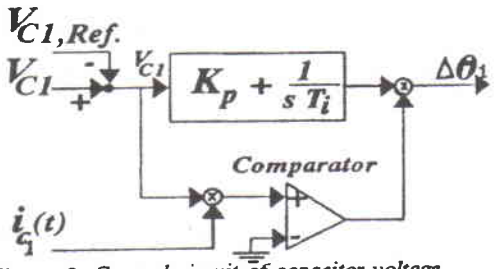


Figure 9. *Control circuit of capacitor voltage*

R-L load. The power circuit is as shown in fig. 1 and the control method is based on AEAPAM method. The objective of this simulation is to study the harmonic contents of output voltage, load current and the ratings of semi-conductor devices. The dc side voltages of capacitors C_1, C_2 and C_3 are set to 10, 30 and 90 volt respectively. R_L and L_L are the load parameters and are 10 (Ω) and 0.002 (H) respectively. Fig.s 10 and 11 show the output stepped voltage and its pectrum frequency respectively. Fig. 12 shows the load current. The inductive part of load causes to readuction of curent harmonics considerably. Fig. 13 to 15 show the current of Q_{11}, Q_{13} and Q_{19} and Fig. 16 to 17 show the current of I_{D1}, I_{D2} and I_{D3} respectively.

VIII. CONCLUSION

In this paper a new magnitudes for dc side voltages of capacitors of a MLVSI has been proposed. Proposed MLVSI produces more levels of voltages compared with previous works. This causes to better quality of output voltage. The AEAPAM method as a very fast and simple method is used to compute the duration of each step of output voltage waveform. The PSCAD / EMTDC simulation results is used to verify the suitable operation of presented power circuit and control strategy.

IX. REFERENCES

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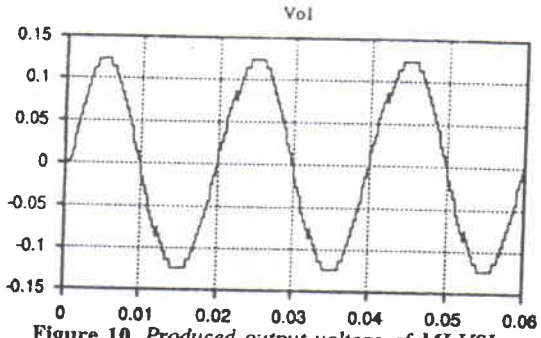

Figure 10. *Produced output voltage of MLVSI*

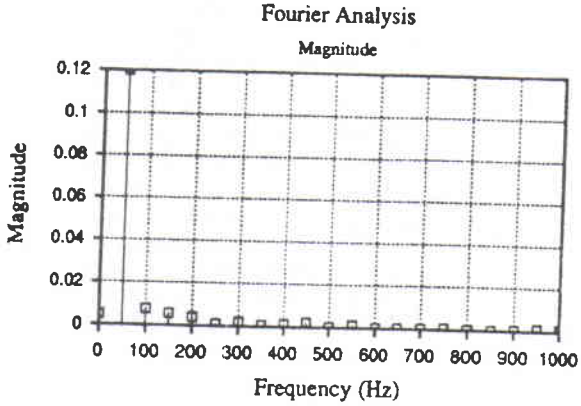

Figure 11. *Spect. Freq. of produced output voltage*

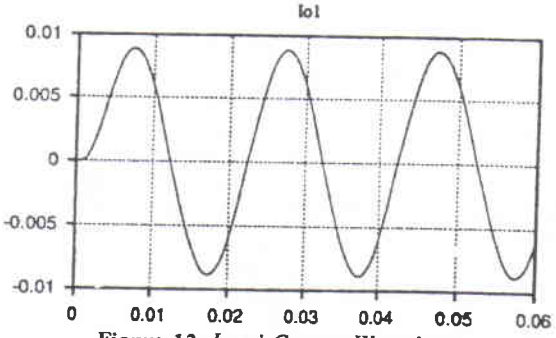

Figure 12. *Load Current Waveshape*

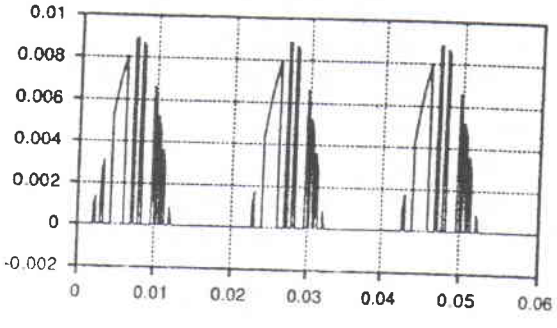

Figure 13. *Current waveshape of* I_{Q11}

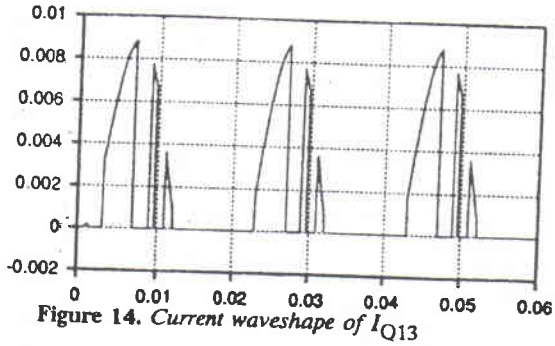

Figure 14. *Current waveshape of* I_{Q13}

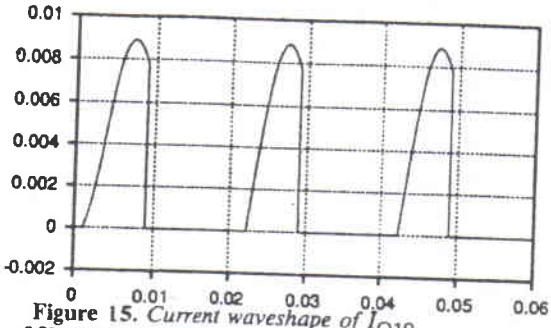

Figure 15. *Current waveshape of* I_{Q19}

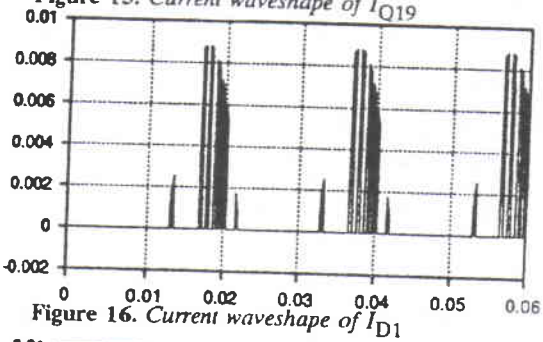

Figure 16. *Current waveshape of* I_{D1}

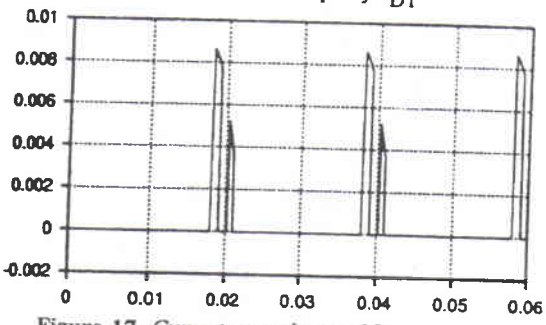

Figure 17. *Current waveshape of* I_{D2}

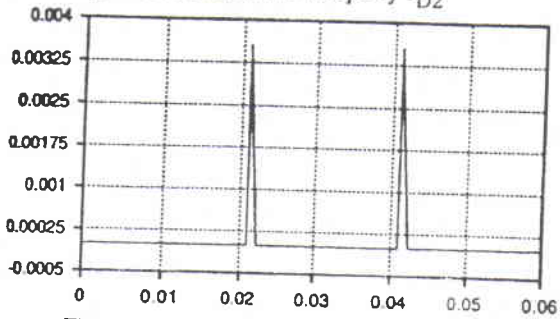

Figure 18. *Current waveshape of* I_{D3}