OPTIMAL HARDWARE ALGORITHM FOR IMPROVED SPIKE AND OVERLOAD ERROR OF ADAPTIVE DELTA MODEM

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ABSTRACT

This paper proposes an efficient and optimal hardware algorithm for realizing adaptive delta modulator and demodulator which would result in reduced slope overload error and improved spike performance compared to earlier adaptive delta modulators. The digital circuits used in the hardware realization are simple in nature and hence makes the system cost effective finding wide ranges of applications in several instrumentation and data communication systems.

I.INTRODUCTION

Delta modulation is an important modulation technique employed for data communication. Since slope overload error is a big problem in delta modulation, adaptive delta modulation became more important. Several algorithms were proposed in the past[1,2] for realising different forms of adaptive delta modulators. A cost-effective adaptive delta modulator and demodulator with improved slope overload performance has been reported in the past[3] where in the step size is doubled on every clock until there is a cross over between the input signal and the accumulated signal. While improving the slope overload error, this process has admitted spikes to be generated in the accumulated signal which represents the transmitted version of the original analog input signal. This has two reasons for the spikes generated. Since the step doubles on every clock, the increased step at the instant of transition of accumulated signal with the analog input signal has large excess voltage at most instances. Furthermore, it takes few clocks for the increased analog voltage to come down to the level of the analog input voltage as the step size after cross over is made as unity. This being a random process, the average value of the spike voltage at the crossover instants has been found a value that is not insignificant. Later, a modification to the step generating algorithm was made [4] to have further reduction in spikes. Herein for any sudden transition in analog signal, the step size is doubled on every clock until the accumulated signal reaches the half of the overall analog range of the input signal and afterwards the rate of step is decreased. Although the spike level has reduced, it still needs a consideration for further reduction. Now in this paper, we propose a modification to the previous algorithms and by selective operation of a special register for 2-bit or 3-bit operation such that the spike is contained to very low value.

II. HARDWARE ALGORITHM FOR THE ADM

A simple block diagram of the ADM is shown in Fig.1. The accumulator generates a data based on the past ADM pulses transmitted, which would always try to approach the given analog signal vi(t). The sampled form of the analog signal vi(nT) and the analog equivalent of the accumulator AC(nT) are compared in an analog comparator C and the present ADM pulses are produced. The step generator produces the new step at every clock. The proposed algorithm for generating the step size can be stated as follows.

When the accumulated signal doesn't cross the analog signal in the comparator, the step size is doubled so that it would catch the input analog signal quickly and when once it crosses it, the step size is made as half the previous step and not made unity step. If there is another crossover by the next clock the step again reduces to half of the previous value. Nevertheless, the minimum step size that can be reached is kept as unity. If the accumulated signal is continuously above(or below) the given analog input signal the step size doubles every time and it is made as half of the previous step after reaching three consecutive increase in step size and thereafter the step doubling process would continue. Fig.2 shows the algorithm for step generation. The average spike level resulted for this algorithm is shown to be less than the previous cases.

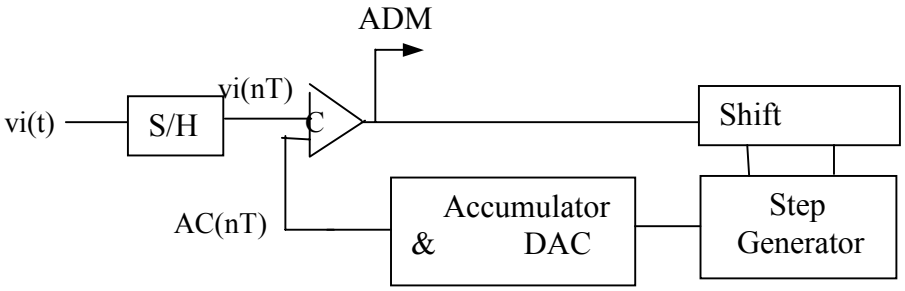

Fig.1.Basic block diagram of ADM

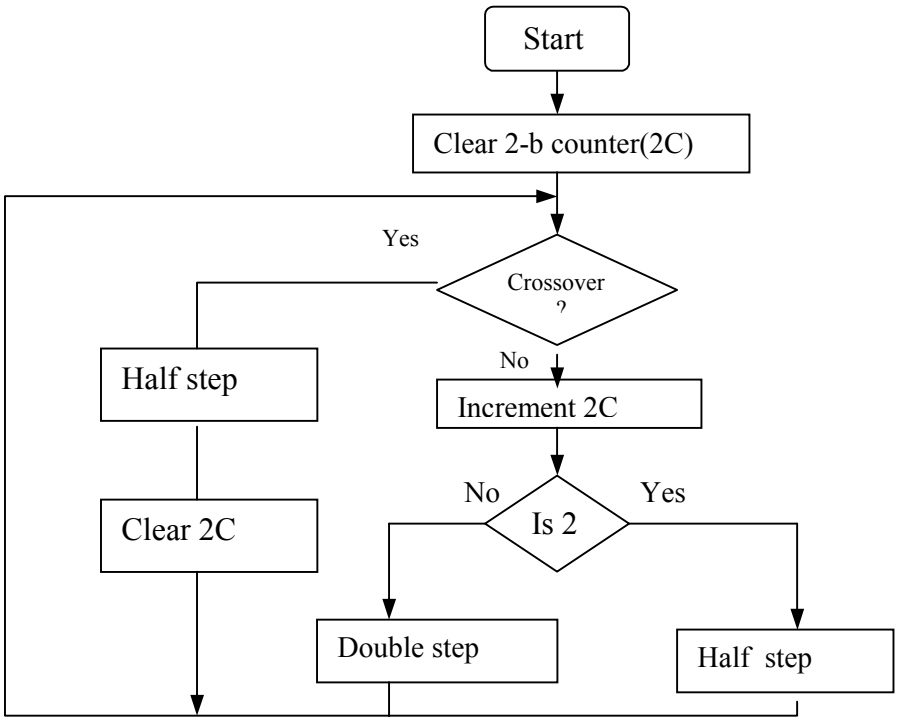

Fig.2. Hardware algorithm for step generation

III. IMPLEMENTATION OF THE ADM ALGORITHM

The block diagram of the proposed ADM modulator is shown in Fig.3. It has the architecture similar to the ones reported earlier[2]. This employs a 4-bit Adder/ Subtracter(4AS), a 4-bit parallel shift register working as accumulator (AC), a 4-bit Digital to Analog Converter(DAC), an analog comparator (C), a 3-bit serial shift right register(SP) to find the trend of the step, a 4-bit step register STR and logic gates. The STR register is a serial shift register whose contents could be shifted right or left at any moment by issuing the commands SR or SL respectively. If the STR is shifted left, the new step would become twice the previous step and if shifted right, the step size would be half the previous step. The 4AS circuit either adds the STR register to the accumulator AC or subtracts STR from the AC by the ADD/SUB command. The data at the accumulator builds up to the level same as that of the given analog input, the status of which being above or below the analog input is represented by the bits of ADM pulse train. The ADM demodulator has a similar circuit as shown in Fig.4. The receiver also follows the same algorithm as that of the transmitter and the accumulator at the receiver at any time would build the same pattern of signal generated by the accumulator of the transmitter. The received ADM pulses are given to the SP register and used as the instantaneous command for the ADD/SUB input of the 4AS. If this is of logic '1' it adds up the STR register to the accumulator (AC) otherwise it would subtract it from the AC.

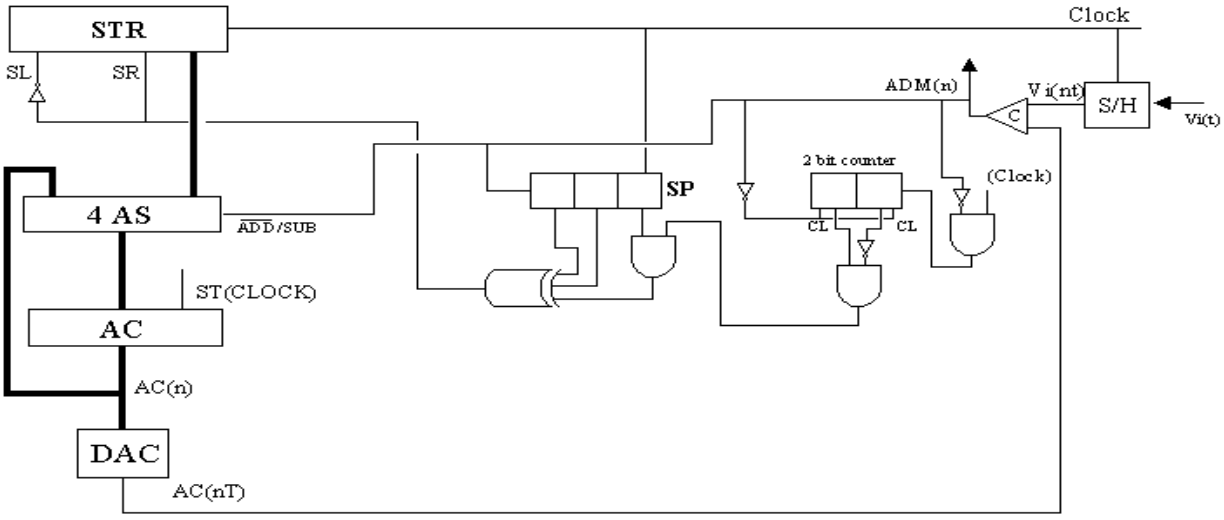

Fig.3. Block diagram of the proposed ADM modulator

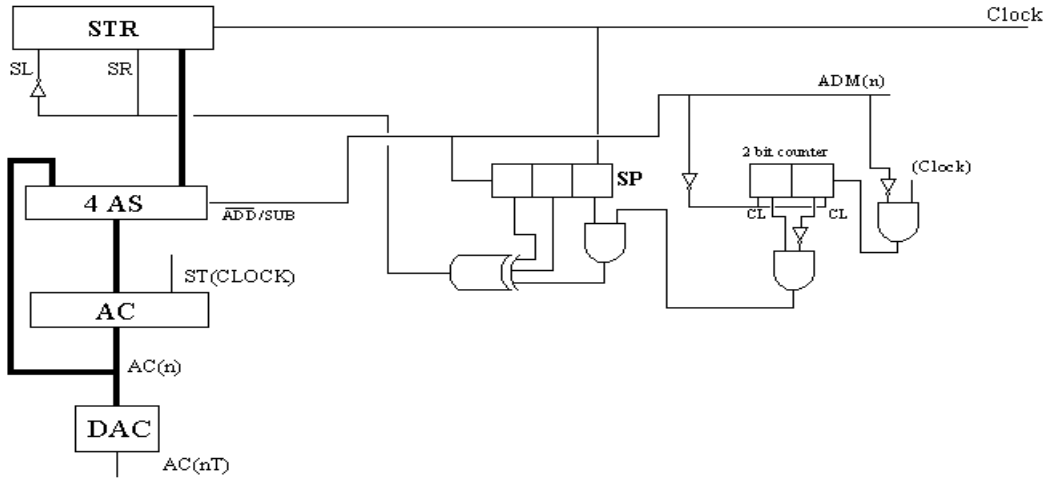

Fig.3. Block diagram of the ADM demodulator

When the ADM data is of '1' it clears the 2-bit counter also. This arrangement in the circuit, therefore, generates the accumulated signal same as that of the transmitter reproducing the original analog signal used in the transmitter. The rapid growth of the accumulated signal enables it to catch the given analog signal quickly and this reduces the slope overload error. Whenever there is a crossover, the spike generated is reduced by making the step size half of the value of step generated at the instant of crossing. Therefore, the time domain signal area of the spike exceeding the original analog signal level is contained to a low value.

IV. PERFORMANCE CHARACTERISTICS THE ADM

The 3-bit SP register in the modulator stores the status of the past three ADM pulses transmitted. The step

size for the new step need be decided based on the status of bits in the SP register. The SR and SL commands are given by an exclusive-OR gate connected to the SP register. By taking only the first two most significant bits of the SP register and controlling the shift operations of the STR register we make a decision based on only two bits. The performance of the ADM for this process is shown in Fig.5a for a standard analog input signal shown. Although the spike performance is good at the regions where transition is steep, the performance is not so good at the regions where the analog input signal keeps a constant value. Alternatively, by taking all the three bits of the SP register for the exclusive-OR gate, the performance gets improved as shown in Fig.5b.The performance is further improved with the proposed algorithm, by selectively operating 2-bits or 3-bits of SP register as shown in Fig.5c. The selective operation of the 2-bits or 3-bits is decided by a 2-bit status counter included in the Fig.2. The present ADM pulse if it has logic '1' the 2-bit counter is cleared so as to start a fresh count. If the present ADM pulse is of logic '0' then counter increments its state. For successive three '0's of the ADM, the counter would reach a state '1 0' and at this stage, the third bit of SP register would also come into action and hence the command to STR register is made based on all the three bits of the SP register. Fig.5d shows the performance of the ADM for triangular wave input by selectively operating the 2-bits or 3-bits activity of the SP register. This system therefore has improved performance over the spikes and the slope overload error.

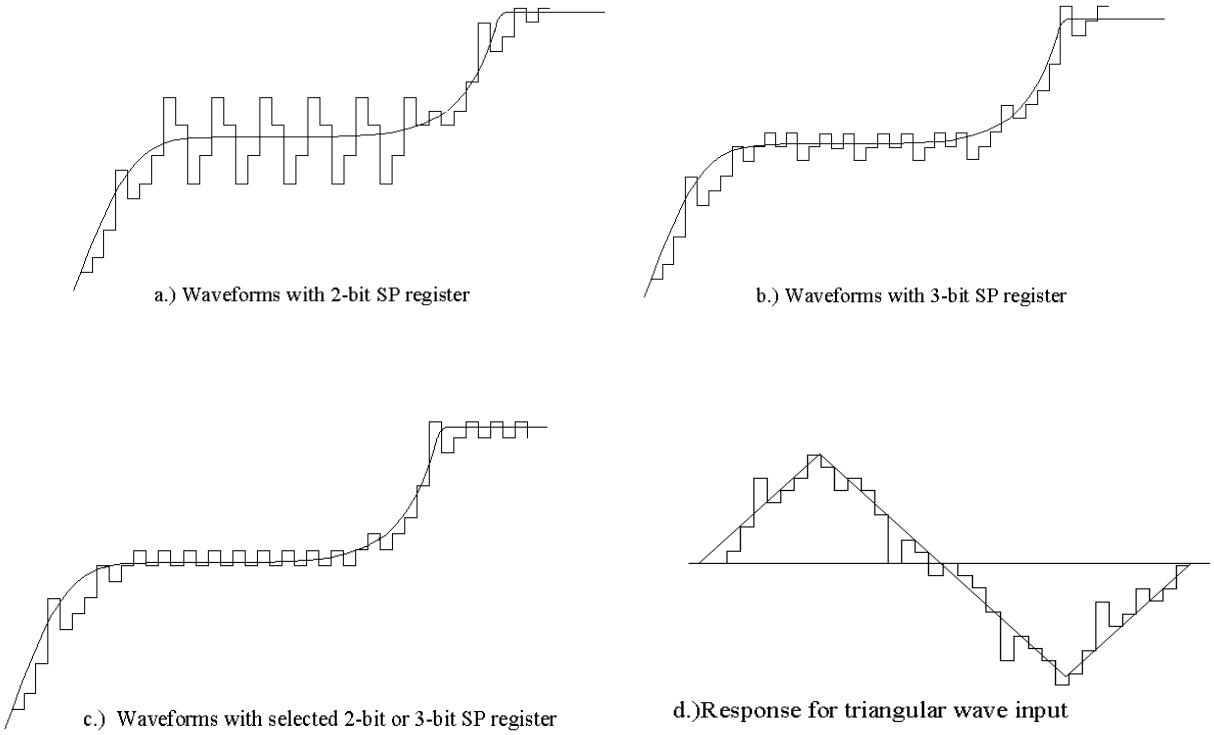

Fig. 5.Response of the ADM for different types of input

In order to estimate the error involved in frequency spectrum, an error analysis has been made using matlab and the results are given in Fig.6. The red plotted lines in each graphic shows us the errors of the respective ADM. As seen in the curves the error incurred in the ADM system operating selectively 2-or3-bits is the lowest.

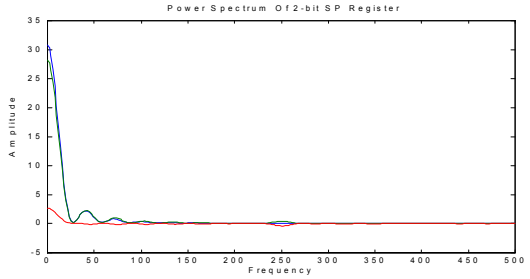

Fig. 6.a. Power Spectrum of 2-Bit SP Register

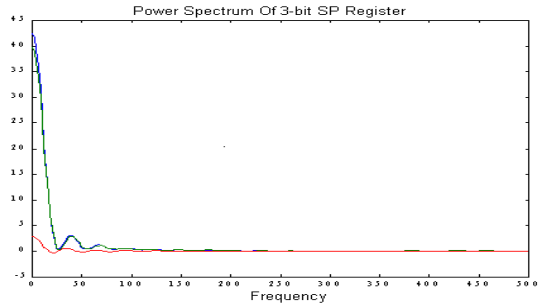

Fig. 6.b. Power Spectrum of 3-Bit SP Register

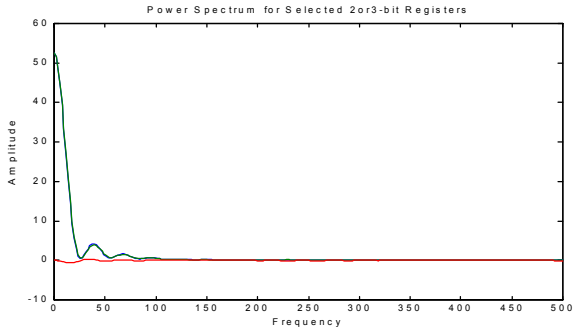

Fig. 6.c. Power Spectrum for Selected 2 or 3-Bit Register

In Fig.6 a, b and c the power spectrum of each given signal according to their used method is plotted. Fig.6.a gives the power spectrum of the signal which is plotted by using 2-bits SP register. Fig. 6.b shows the power spectrum of the signal which is plotted by using 3-bits sp register, and finally Fig.6.c shows us the power spectrum of the signal output by using the selectively 2-bits or 3-bits SP register. The red plotted lines are showing the errors of each used ADM according to their used SP registers. As seen on the graphics, by checking the red line of Fig. 6.c, the selectively 2-bit or 3-bit ADM is giving a much lower result in error then the other used methods in the ADMs.

As specified before this shows that the system has improved the performance over the spikes and the slope overload error.

V. DISCUSSIONS

The proposed adaptive delta modem is implemented based on an efficient hardware algorithm and it is cost effective since the circuits involved are simple in nature. All decisions in step generation and rebuilding the are done by hardware. The simplicity in the hardware realization makes the unit suitable for any data communication and instrumentation systems. For instance, it find applications in process industries where the instantaneous process parameters at the plant need be transmitted to the control room at a distance for monitoring purposes. It also finds applications in several telemetering and tele-control systems where several data need be multiplexed and transmitted. Data compression is inherent in the system since only one bit is needed for the sample and this makes added advantages for its suitability to many systems.

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