ROBUST INTERNAL MODEL CONTROL
OF ASVC-BASED VAR FLOW COMPENSATION

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Abstract

Var compensators should be properly controlled to provide fast and continuous reactive power to meet a certain load demand. This ensures improved transmission performance and enhance the transient stability of the power system. This paper deals with the application of the internal model control technique to an advanced static var compensator. The controller is evaluated under a variety of operating conditions and the simulations results demonstrate instantaneous and robust var flow with the ac transmission system and superior performance as compared to a conventional proportional-integral controller.

I. INTRODUCTION

Power transmission performance with higher long line transmission capacity and improved transient stability is achieved through a rapid and continuous reactive power support to the power system following large, fluctuating load demands.

Static Var Compensators (SVCs) are high power electronics based devices used to provide fast variable reactive power compensation. By controlling the device switches, the equivalent susceptance is varied and hence the reactive current injected or absorbed from the transmission line is controlled.

The introduction of modern semiconductor devices in the design of power electronic converters has resulted in a solid-state Var source with a more simple structure namely the Advanced Static Var Compensator (ASVC) [1], [2]. The ASVC uses a PWM controlled dc/ac voltage-source inverter (VSI) with a capacitor as a dc power storage device.

The effectiveness of these compensators depends on the choice of the control strategy. Conventional voltage regulation loops are based on a proportional-integral (PI) controller. These produce satisfactory performance only for limited operating range conditions. Various control approaches have been proposed in the literature [3], [4].

This paper considers the application of the internal model control (IMC) [5] concept to adjust the ASVC Var flow with the ac system. The performance of the closed loop control system is analysed and the effectiveness of the ASVC proposed controller is demonstrated and compared to a conventional PI controller.

II. OVERVIEW AND MODELLING OF THE ASVC

The basic ASVC scheme is illustrated in Fig. 1. The ASVC circuit consists of six-pulse VSI with a dc capacitor and a PWM modulator. Connection of the ASVC to the transmission line is via a coupling transformer. With reference to Fig. 1, R_s and L_s represent the coupling transformer active losses and leakage respectively.

Basically, the ASVC supplies reactive power to the ac transmission system if the magnitude of the inverter voltage is greater than the ac terminal voltage. It draws reactive power from the ac transmission system if the magnitude of the ac terminal voltage is greater to the inverter voltage. Var exchange is zero when the two voltages are equal.
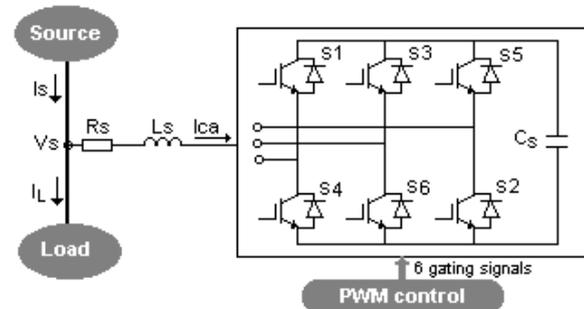

Fig. 1 Circuit diagram of the ASVC

It is assumed that the source is a balanced sinusoidal three-phase voltage supply with frequency ω.

The equivalent circuit of the ASVC connected to a transmission line is shown in Fig. 2.

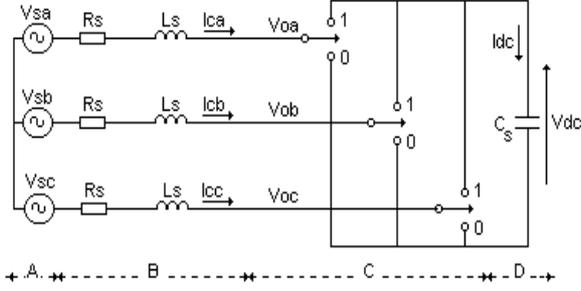
Fig. 2 Three-phase equivalent circuit of the ASVC
A : three-phase source voltage.
B : coupling transformer.
C : PWM voltage source inverter.
D : dc-side capacitor.

Where

I_s, I_L : source and load currents.
I_{ca}, I_{cb}, I_{cc} : ASVC currents.
V_{sa}, V_{sb}, V_{sc} : source voltages
V_{dc}, I_{dc} : dc-side voltage and current.

Applying d-q transform to the ac circuit and combining the dc circuit equation, the ASVC model is obtained as

$$\frac{d}{dt}\begin{bmatrix} i_q \\ i_d \\ V_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} & -\omega & 0 \\ \omega & -\frac{R_s}{L_s} & -\frac{m}{L_s} \\ 0 & -\frac{m}{C_s} & 0 \end{bmatrix}\begin{bmatrix} i_q \\ i_d \\ V_{dc} \end{bmatrix} + \frac{V_s}{L_s}\begin{bmatrix} \sin\alpha \\ \cos\alpha \\ 0 \end{bmatrix} \quad (1)$$

The modulation index (MI) relates the maximum phase voltage to the dc link voltage

$$MI = \sqrt{\frac{2}{3}}m = \frac{(V_0)_{peak}}{V_{dc}} \quad (2)$$

The state equation is non-linear with respect to the control variable α which is related to the phase difference between the source voltage and inverter output voltage. In the range of small values of α ($|\alpha| < 5°$), the small signal equivalent state equations are expressed as

$$\frac{d}{dt}\begin{bmatrix} \Delta i_q \\ \Delta i_d \\ \Delta V_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} & -\omega & 0 \\ \omega & -\frac{R_s}{L_s} & -\frac{m}{L_s} \\ 0 & -\frac{m}{C_s} & 0 \end{bmatrix}\begin{bmatrix} \Delta i_q \\ \Delta i_d \\ \Delta V_{dc} \end{bmatrix} + \frac{V_s}{L_s}\begin{bmatrix} -1 \\ 0 \\ 0 \end{bmatrix}\Delta\alpha \quad (3)$$

The system input is the control variable deviation $\Delta\alpha$ and the output is the generated reactive power given by

$$\Delta Q_c = \begin{bmatrix} -V_s & 0 & 0 \end{bmatrix} \quad (4)$$

Hence the system transfer function is given by

$$\frac{\Delta Q_c(s)}{\alpha(s)} = \frac{V_s^2\left(\frac{1}{L_s}s^2 + \frac{R_s}{L_s}\frac{m^2}{L_s^2 C_s}s\right)}{s^3 + 2\frac{R_s}{L_s}s^2 + \left(\omega^2 + \frac{R_s^2}{L_s^2} + \frac{m^2}{L_s C_s}\right)s + m^2\frac{R_s}{L_s^2 C_s}} \quad (5)$$

III. CONTROL SCHEME OF THE ASVC

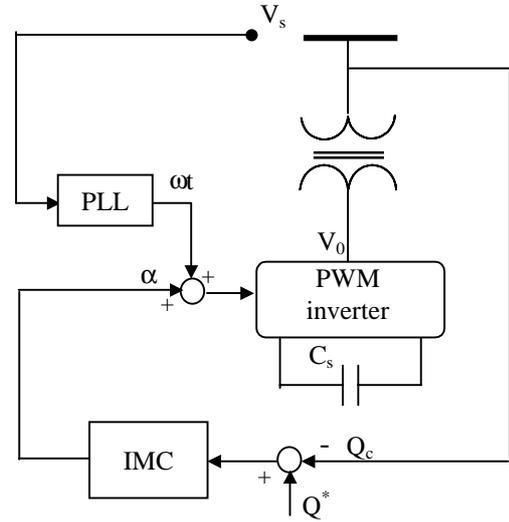The overall closed loop control system is pictured in Fig. 3.

Fig. 3 ASVC closed loop control system

The basic architecture of a classical IMC is illustrated by Fig. 4 [5]. A system model is placed in parallel with the actual system. The difference is used to adjust the command signal. An attractive feature of IMC is that it produces an offset-free response even when the system is subjected to a constant disturbance.
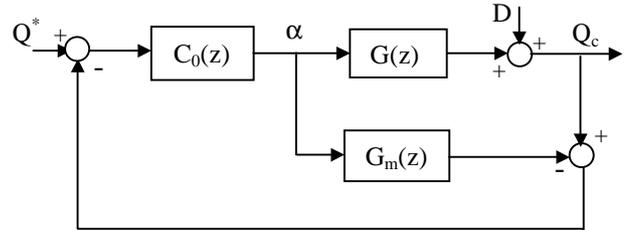

Fig. 4 Basic IMC structure

With reference to Fig. 4, the control and output signal are expressed as

$$\alpha(z)=\left\{1+C_0(z)\left[G(z)-G_m(z)\right]\right\}^{-1}C(z)\left[Q^*(z)-D(z)\right]$$

$$Q_c(z)=G(z)\left\{1+C_0(z)\left[G(z)-G_m(z)\right]\right\}^{-1}C(z)\left[Q^*(z)-D(z)\right]+D(z)$$

If a perfect model is assumed ($G(z) = G_m(z)$) then the closed loop system is stable if the controller $C(z)$ and the system are stable. However under mismatch conditions ($G(z) \neq G_m(z)$), a low pass filter is introduced in the feedback loop to improve the controller robustness with respect to modelling errors.
The design filter has the following transfer function

$$F(z)=\frac{(1-\beta)z}{(z-\beta)} \qquad 0 < \beta < 1 \tag{6}$$

In what follows β has been fixed to 0.002. Since the controller is the inverse of the system model (i.e. $C_0(z) = G_m(z)^{-1}$) then $Q_c(z) = Q^*(z)$ and the system model should be inverse stable. Furthermore if $C_0(1)=G_m(1)^{-1}$ the controller produces an offset-free response.

With a sampling period of T_s=0.005 sec, the discrete-time transfer function of the system is obtained as

$$G(z)=\frac{200^2(0.3441z^2+0.3819z+0.2207)}{z^3+0.269z^2-0.187z-0.1353} \tag{7}$$

By taking $G_m(z) = G(z)$ then the poles and zeroes of $G_m(z)$ are $p_{1,2} = -0.407 \pm j0.2943$, $p_3 = 0.5404$ and $z_{1,2} = -0.5549 \pm j0.5775$.

Following the steps described in the Appendix the controller transfer function is given by

$$C_0(z)=\frac{1}{200^2}\left[\frac{z^3+0.269z^2-0.187z-0.1353}{0.9467z^3}\right] \tag{8}$$

IV. PERFORMANCE EVALUATION

Simulations were performed under Matlab/Simulink environment with the following ASVC parameters

$R_s = 1\ \Omega$ $\qquad L_s = 5.10^{-3}H$ $\qquad C_s = 500.10^{-6}\ F$
$V_s = 220\ V$ $\qquad m = 0.646$ $\qquad \omega = 100\pi$ rad/sec

The PI parameters are obtained using root locus design as shown in Fig. 5. For a desired damping factor of 0.7 the following controller gains are obtained

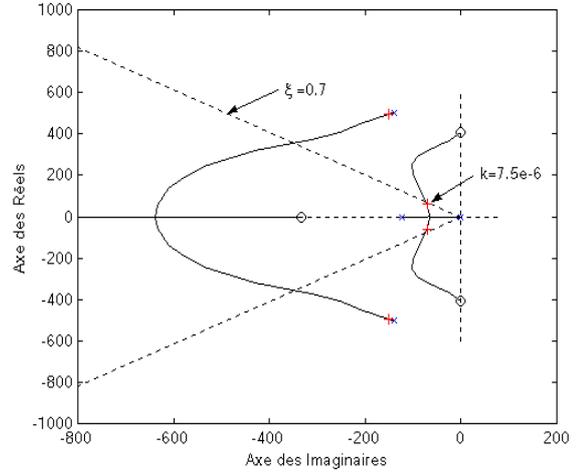$$K_p=7.5\times10^{-6} \qquad K_i= =2.5\times10^{-3} \tag{9}$$

Fig. 5 Root locus of the closed-loop control system

IMC controller design was based on the linearised model of the ASVC and then applied to the non-linear one.
In Fig. 6 is shown the ASVC transient response in the case of the linear model. The var command was varied from 10 Kvar (inductive) to –10 Kvar (capacitive) to cause the system to swing from leading to lagging mode at time 0.2 sec.
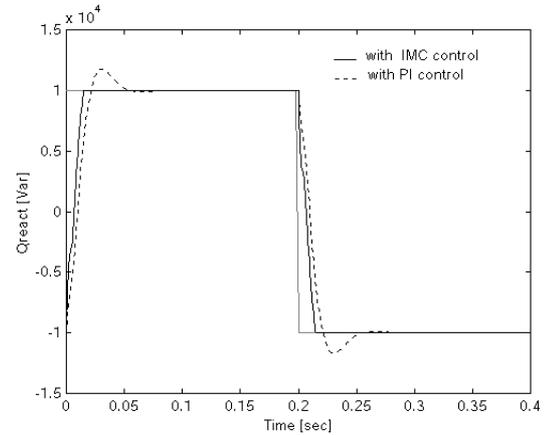

Fig. 6 Reactive power response under step change from inductive to capacitive with the linear model IMC (solid), PI (dotted)

IMC leads to a faster transient response with a shorter settling time and with no overshoot.
In the next simulation result the controllers are tested with the non-linear model of the ASVC under the same conditions. Again, from the responses of Fig. 7 it can be observed that IMC produces a better performance than PI control which demonstrates its robustness under model mismatch situations.
Finally, the controllers are evaluated under more realistic simulation conditions by considering the PWM control circuit. Fig. 8 and 9 show the reactive power responses under IMC and PI controls and the current waveforms respectively.
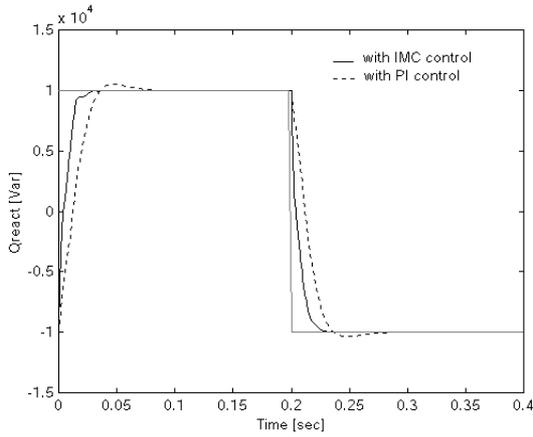
Fig. 7 Reactive power response under step change from inductive to capacitive with the non-linear model IMC (solid) , PI (dotted)
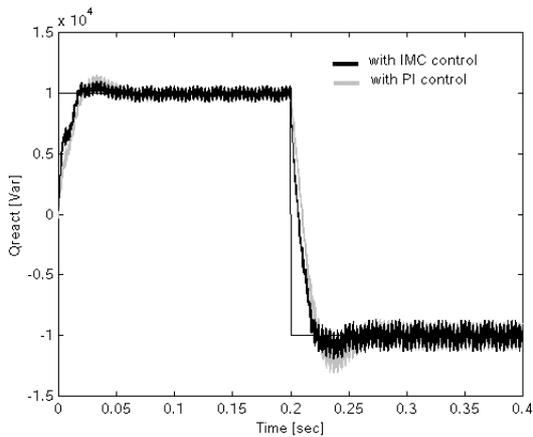

Fig. 8 Reactive power transient response under a step change from 10 Kvar leading to 10 Kvar lagging.

It is observed from Fig. 9 how the current injected into the transmission line swings instantaneously in response a capacitive var demand.
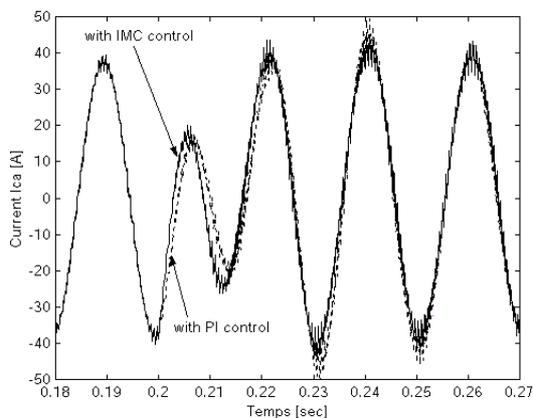

Fig. 9 Phase a current response

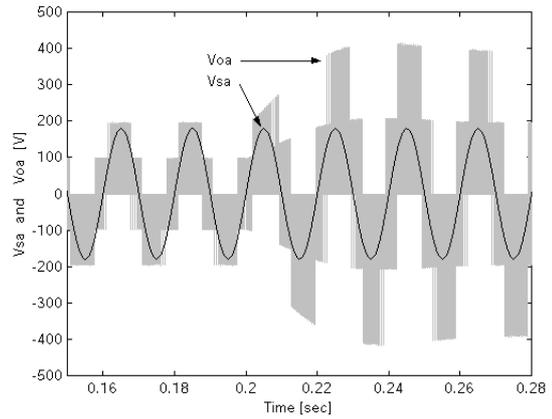Fig. 10 and 11 show the source voltage and inverter output voltage waveforms with PI and IMC respectively.

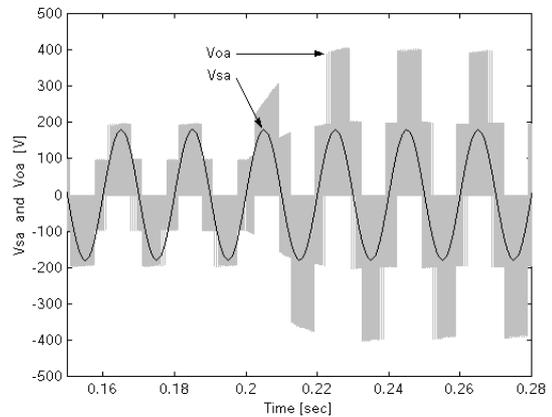Fig. 10 Source voltage and inverter output voltage (PI)

Fig. 11 Source voltage and inverter output voltage (IMC)

V. CONCLUSIONS

In this simulation study the performance and robustness of IMC has been evaluated and compared to a conventional PI controller in the control of an ASVC. From the results presented it can be concluded that IMC leads to improved transient response and hence provides fast reactive power compensation to the ac transmission network. IMC controller is easily tuned and is very suitable for real time implementation.

APPENDIX

Let assume that the system model be given of the form

$$G_m(z) = K \frac{\prod_{i=1}^{n}(z-z_{i-1})}{\prod_{i=1}^{n}(z-p_i)} z^{-d} \qquad (10)$$

where n is the system order, p_i and z_i are the system poles and zeroes respectively, d is the discrete time-delay equal to an integer number of sampling periods.

Assuming a stable model $G_m(z)$ (i.e $|p_i| < 1$), the design procedure is performed through the following rules:

<u>Rule 1</u> : The zeroes of $C_0(z)$ are equal to the poles of G(z).

<u>Rule 2</u> : The poles of $C_0(z)$ are chosen as follows :
- the zeroes of G(z) with positive real part and inside the unit circle (Fig. 12, zone 1)
- the inverses of the zeroes of G(z) with positive real part and outside the unit circle (Fig. 12, zone 2)
- A pole at the origin for each zero with negative real part (Fig. 12, zone 3)
- It can be shown that this rule ensure a stable controller minimises the sum of the squared errors.
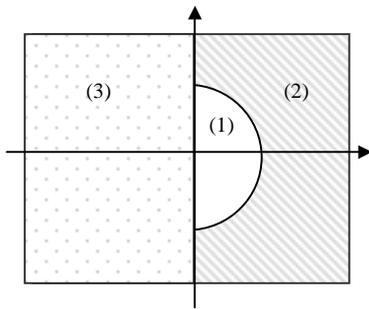

Fig. 12 Zeroes of G(z) in the z-plane

<u>Rule 3</u> : Include an extra pole at the origin to $C_0(z)$ to compensate the inherent delay introduced by the sampling process.

<u>Rule 4</u> : The gain of $C_0(z)$ is chosen such that $C_0(1)\, G(1)=1$

<u>Rule 5</u> : Introduce the design filter F(z) to $C_0(z)$ to allow for modelling errors with a cut-off frequency such that $0 < \beta < 1$.

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