A NEW VOLTAGE SCALING TYPE DIGITAL-ANALOG CONVERTER USING ONLY DDCCS

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ABSTRACT

In this paper, a new voltage scaling type digital-analog converter (DAC) circuit using only differential difference current conveyors (DDCCs) is presented. The circuit does not employ any other active or passive elements. Only biasing currents of the active element are present, thus the proposed circuit has low power consumption.

I. INTRODUCTION

One of the most important functions in signal processing is the conversion between analog and digital signals. The input to a digital-analog converter (DAC) is a digital word consisting of parallel binary signals that are generated from a digital signal processing system. These parallel binary signals are converted to an equivalent analog signal by scaling a reference. The analog output may be filtered and/or amplified before being applied to an analog signal processing system [1]. Voltage DACs converts a reference voltage, (say V_r), to a set of 2^N voltages that are decoded to a single analog output by the input digital word.

On the other hand, , because of its high input impedance and arithmetic operation capability of a recently proposed active element, differential difference current conveyor (DDCC) [2], the component number of the circuits using DDCCs can be lower than that of the circuits using other active elements like voltage operational amplifiers, operational transconductance amplifiers (OTAs), etc. [1,3].

Although a number of CMOS DACs have been published in the literature [4-6], they have complex circuit structure.

In this work, a simple DDCC-based DAC configuration is presented. The proposed circuit uses only DDCCs and is quite suitable for integration. Having only biasing currents of the active element involved the presented circuit consumes low power.

II. PROPOSED CIRCUIT

The DDCC, whose electrical symbol is shown in Figure 1, is a five-terminal network with terminal characteristics described by

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ I_Z \end{bmatrix} \quad (1)$$

where the plus and minus signs indicate whether the conveyor is configured as a minus or plus type circuit, termed DDCC- or DDCC+, respectively.

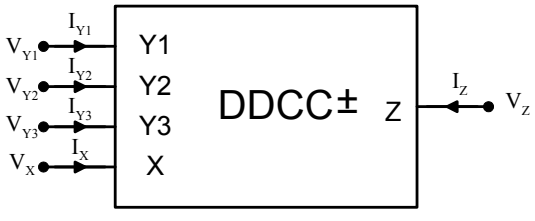


Figure 1. Electrical symbol of DDCC

A general block diagram for a voltage scaling DAC is shown in Figure 2. The decoder network simply connects one of the V_1, V_2, …., V_2^N voltages to v_{OUT}.

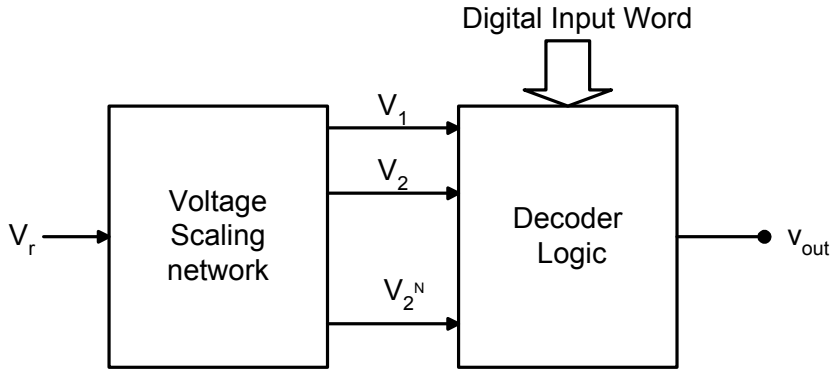


Figure 2. General voltage scaling DAC

According to the voltage relation between the Y1, Y2, Y3 and X terminals given in (1), the circuit configuration illustrated in Figure 3 has the following transfer function

$$V_{o1} = \frac{1}{2}V_{io} + \frac{1}{2}V_{i1} \tag{2}$$

Accordingly, the circuit configuration given in Figure 4 that consists of *N* cells from the one given in Figure 3 has the following transfer function

$$V_{oN} = \frac{1}{2^N}V_{i1} + \frac{1}{2^{N-1}}V_{i2} + ... + \frac{1}{2}V_{iN} \tag{3}$$

For $V_{i1} = V_{i2} = V_{iN} = V_r$ (3) can be written as

$$V_{oN} = (\frac{1}{2} + \frac{1}{2^2} + ... + \frac{1}{2^N})V_r \tag{4}$$

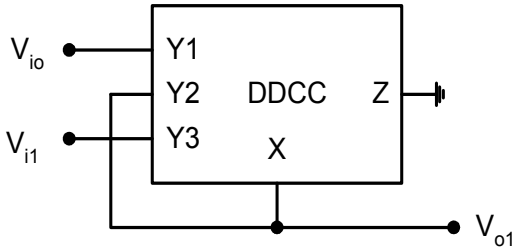


Figure 3. The DDCC-based cell used for the proposed DAC

From (4) it can be concluded that the V_{oN} is the analog output voltage for *N*-bit binary input and the circuit given in Figure 4 is a voltage scaling DAC circuit. The main advantages of the proposed circuit are that it includes *N* number of the active element DDCC to convert *N*-bit digital input to an analog output without any other active or passive elements and there is no output current passes through the cells of the DAC, thus it has low power dissipation.

III. SIMULATION RESULTS

In order to confirm the theoretical validity of the proposed DAC configurations given in Figure 4 it is simulated with SPICE simulation program. To implement the DDCC the CMOS structure shown in Figure 5 is used [2]. The aspect ratios of the MOS transistors are given in Table 1. The device model parameters used for the SPICE simulations are taken from MIETEC 0.5 µm CMOS process and given in Table 2. The supply voltages are selected as V_{DD}=5 V and V_{BB}=1 V and the reference voltage V_r is chosen as 4 V.

The output analog voltage of the proposed 8-bit DAC is deduced at rate of 50 MSample/s. The input code differs from 00000000 to 11111111 regularly. Figure 6 shows the LSB (least significant bit), MSB (most significant bit) and the analog output signals of the DAC. It is observed from that the analog output changes from 0.1 to 4 Volts and agrees with theoretical predictions. The errors seen near 0 V are due to the given CMOS structure of the active element, which is unsuitable for low input voltage operations. The total power consumption of the circuit is calculated as 1.76 mW.

Table 1. Transistor aspect ratios of the DDCC circuit given in Figure 5.

TRANSISTOR	W (µm)	L (µm)
M1-M4	0.8	0.5
M5-M6	10	0.5
M7-M8	4	0.5
M9-M10	14.5	0.5
M11-M12	45	0.5
M13-M15	9.6	0.5
M16-M18	45	0.5

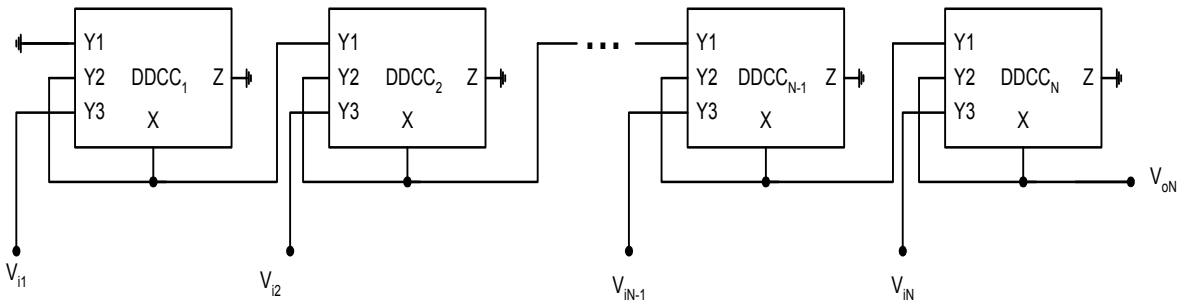


Figure 4. The proposed DDCC-based *N*-bit DAC

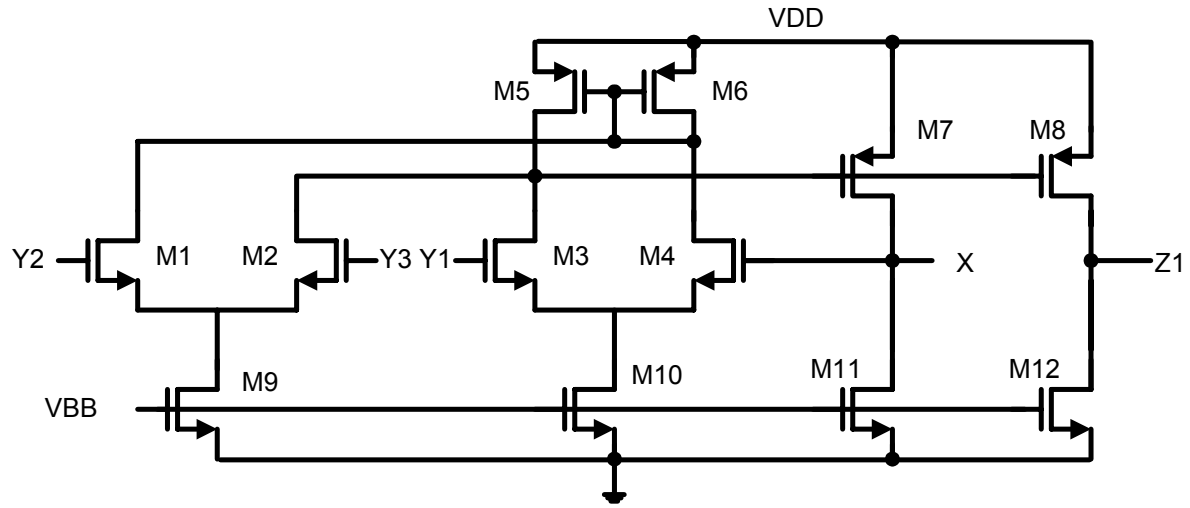
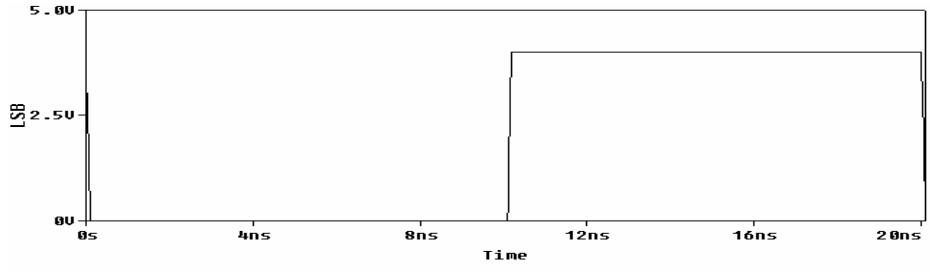


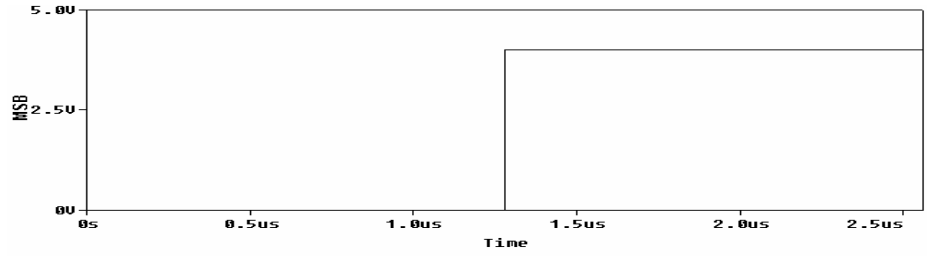
Figure 5. The CMOS structure of DDCC

Table 2. 0.5μm MIETEC CMOS process model parameters

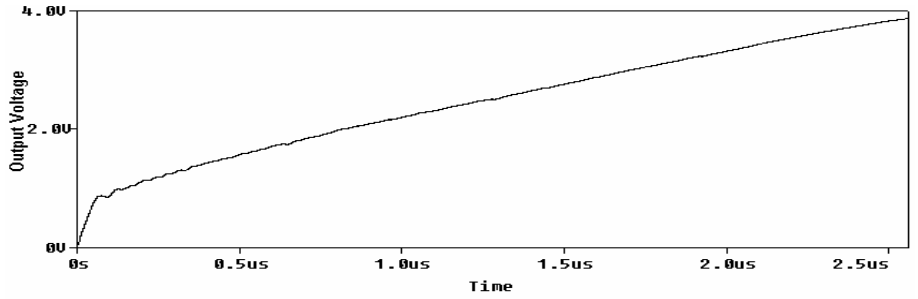
.MODEL NT NMOS LEVEL=3
UO=460.5 TOX=1.0E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73 LD=0.04E-6 ETA=0 VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=0.905 THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1 WD=.11E-6 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10 MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42 NFS=1.2E11
.MODEL PT PMOS LEVEL=3
UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=0.1E-6 RS=886 RSH=1.81 LD=0.03E-6 ETA=0 VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=0.905 THETA=0.120 GAMMA=.76 KAPPA=2 AF=1 WD=.14E-6 CJ=85E-5 MJ=0.429 CJSW=4.67E-10 MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81 NFS=0.52E11



(a)



(b)



(c)

Figure 6. The voltage signals of the proposed DAC a) LSB, b) MSB and c) output

IV. CONCLUSIONS

In this paper, a new N-bit voltage scaling DAC circuit configuration has been proposed. The proposed DAC is constructed using only the active element DDCC, which makes it suitable for integration. The performance of the DAC is tested using SPICE simulation program. It is seen that the simulation results verify the high performance of the proposed circuit.

REFERENCES

1. P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, Oxford University Press, New York, 2002.
2. W. Chiu, S.-I Liu, H.-W Tsao, and J.-J Chen**,** "CMOS differential difference current conveyors and their applications", IEE Proc. Circ. Devices Syst., vol. 143, pp. 91-96, 1996.
3. S. Minaei and S. Turkoz, "An 8-bit 50-MS/s CMOS digital-analog converter", Proc. of the 2nd International Conference on Electrical and Electronics Engineering, Bursa-Turkey, November 2001, (Electronics) pp. 82-85.
4. T. Miki, Y. Nakamura, Y. Nishikawa, K. Okada and Y. Horbia, "A 10 bit 50-MS/s CMOS D/A converter with 2.7 power supply", Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers, pp. 92-93, 1992.
5. D. Reynolds, "A 320 MHz CMOS triple 8 bit DAC with on-chip PLL and hardware cursor", IEEE J. Solid-State Circuits, vol. 29, pp. 1545-1551, 1994.
6. L. S. Y. Wong, C. Y. Kwok and G. A. Rigby, "A 1-V CMOS D/A converter with multi-input floating-gate MOSFET", IEEE J. Solid-State Circuits, vol. 34, pp. 1386-1390, 1999.