# A *2.5GHZ 0.35μm* CMOS MIXER WITH IMPROVED LINEARITY

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**ABSTRACT**

**A new linearization technique for a CMOS high frequency mixer will be presented. The reduction of the total harmonic distortion coefficient is achieved by replacing the simple differential amplifier from the basic multiplier circuit with a cross-connection differential amplifier, with the advantage of canceling the third-order harmonic from the output signal expression. The circuit was implemented in *0.35μm* CMOS technology and it was supplied at $V_{CC} = 3V$. The transient and Fourier analysis for high frequency input signals ($\omega_1 = \omega_2 = 2.5GHz$ and $\omega_1 = 2.5GHz$; $\omega_2 = 2.25GHz$) confirm the theoretical estimated results (an improvement in linearity of about *8dB*).**

## I. INTRODUCTION

Multipliers are important circuits for implementing various nonlinear functions in analog signal processing, such as multiplication/division, modulation /demodulation and rectification.

The common approach for implementing a voltage multiplier in CMOS technology is based on MOS transistors working in saturation. The linearity of the basic multiplier still remains poor because of the fundamental nonlinear characteristic of the MOS transistor. Thus, it results the possibility of achieving a relatively good linearity only for a restricted input voltage range, the amplitude of the input voltages being restricted below a few hundreds of $mV$.

Consequently, it is obviously the necessity of implementing a linearization technique for decreasing the superior-order nonlinearities of the MOS multipliers and for increasing the available range for the input voltage amplitudes. It exists in literature many circuit techniques used to improve the linearity of the MOS differential amplifier (the basic cell of the CMOS multiplier). It was presented in [1], [2] a third and fifth-order harmonics cancellation with good results and a relatively simple circuit implementation. A constant-sum of the gate-source voltages circuit connection was described in [3] and it allows an important reduction of the total harmonic distortions coefficient of the circuit. In [4], it was presented and implemented in CMOS technology a simple technique based on square-root circuits for improving the CMOS differential stage linearity, which compensate the quadratic characteristic of the MOS transistor working in saturation.

## 2. THEORETICAL ANALYSIS

The circuit proposed below is designed with the main goal of reducing *THD* and represents the result of a linearization technique applied to a basic multiplier using MOS transistors in saturation.

### *THE BASIC CIRCUIT*

Because of the quadratic characteristic of a MOS transistor in saturation, the linearity of the basic multiplier presented in Figure 1 is rather poor, resulting in a large value of the total harmonic distortion coefficient. The core of this circuit is a modified Gilbert cell, extended to realize the multiplication function.

Considering an operation in saturation of all transistors from Figure 1, the expressions of the drain currents for $Q_1 - Q_4$ transistors are:

$$I_{1,2} = \frac{I}{2}\left(1 \pm \sqrt{\frac{KV_1^2}{I} - \frac{K^2V_1^4}{4I^2}}\right) \quad (1)$$

$$I'_{2,1} = \frac{I'}{2}\left(1 \pm \sqrt{\frac{KV_1^2}{I'} - \frac{K^2V_1^4}{4(I')^2}}\right) \quad (2)$$

So, the output current expression will be:

$$I_o = (I_1 - I_2) + (I'_1 - I'_2) = \\ = V_1\left(\sqrt{KI - \frac{K^2}{4}V_1^2} - \sqrt{KI' - \frac{K^2}{4}V_1^2}\right) \quad (3)$$

Similarly, the drain currents of $Q_5$ and $Q_6$ transistors will have the following expressions:

$$I = \frac{I_0}{2}\left(1+\sqrt{\frac{KV_2^2}{I_0}-\frac{K^2V_2^4}{4I_0^2}}\right) \quad (4)$$

$$I' = \frac{I_0}{2}\left(1-\sqrt{\frac{KV_2^2}{I_0}-\frac{K^2V_2^4}{4I_0^2}}\right) \quad (5)$$

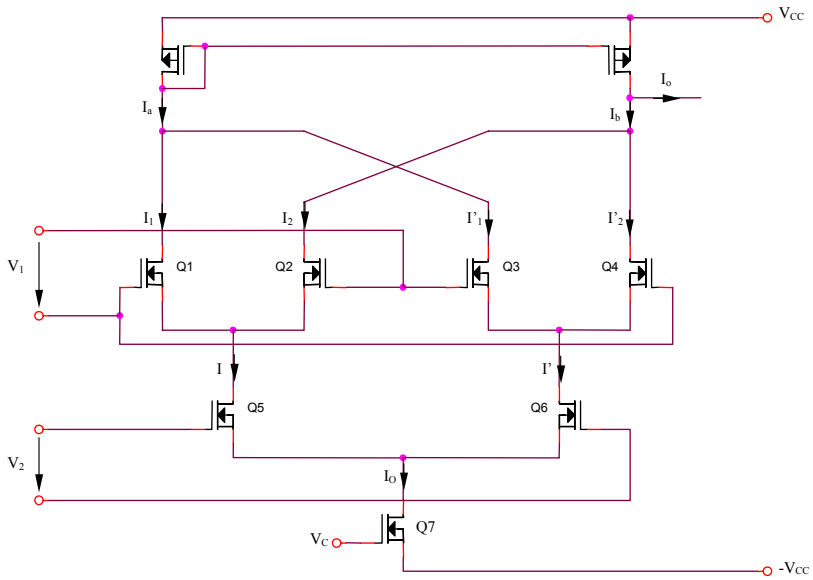


Figure 1: Basic CMOS multiplier circuit

All transistors from Figure 1 are supposed to be identical ($K$). Considering the limited expansion $\sqrt{1+x} \cong 1+x/2$, from the previous relations, it results the approximate expression of the basic multiplier output current:

$$I_o \cong \frac{K}{\sqrt{2}}V_1V_2 - \frac{K^2}{8\sqrt{2}I_0}V_1V_2^3 \quad (6)$$

Thus, the total harmonic distortion coefficient (approximated with the third-order one) will be expressed as:

$$THD_3 \cong \frac{KV_2^2}{8I_0} = \frac{1}{4}\left(\frac{V_2}{V_C - V_T}\right)^2 \quad (7)$$

In conclusion, $THD_3$ is directly proportional with the ratio of $V_2$ input signal amplitude and the effective gate-source voltage of the polarization transistor.

## *THE NEW CMOS MULTIPLIER WITH IMPROVED LINEARITY*

In order to improve the circuit linearity, the new proposed multiplier presented in Figure 2 replaces the differential amplifier $Q_5 - Q_6$ from Figure 1 by a cross-connected one, $Q_5 - Q_8$ from Figure 2.

The output current expression for the multiplier with improved linearity has the same form (3), but the expressions of $I$ and $I'$ currents become:

$$I = I_{p1} + I'_{p1} \quad (8)$$

$$I' = I_{p2} + I'_{p2} \quad (9)$$

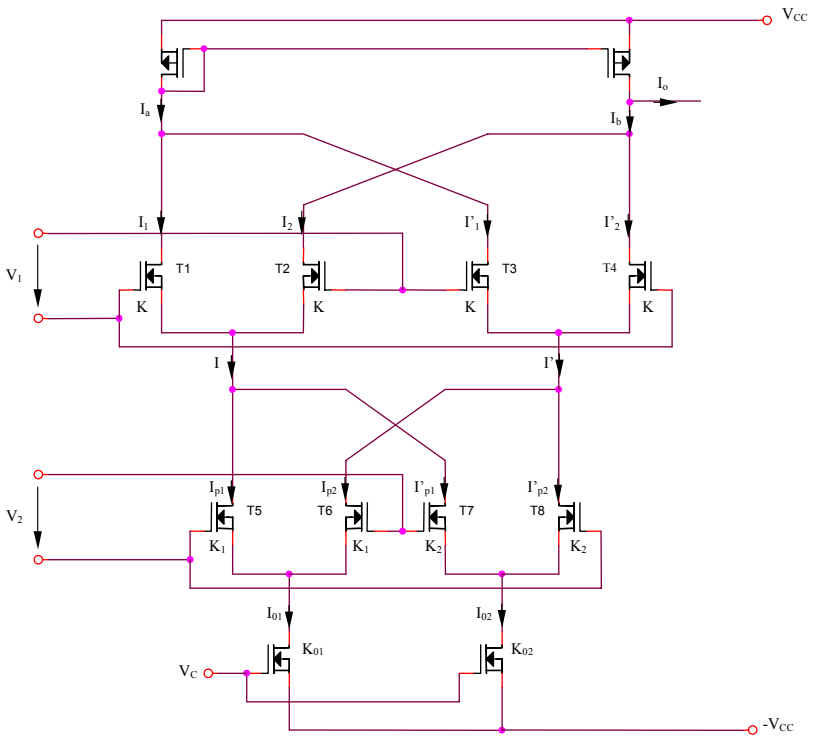


Figure 2: The new CMOS multiplier with improved linearity

where:

$$I_{p_{1,2}} = \frac{I_{0_1}}{2}\left(1 \pm \sqrt{\frac{K_1 V_2^2}{I_{0_1}} - \frac{K_1^2 V_2^4}{4 I_{0_1}^2}}\right) \tag{10}$$

$$I'_{p_{1,2}} = \frac{I_{0_2}}{2}\left(1 \mp \sqrt{\frac{K_2 V_2^2}{I_{0_2}} - \frac{K_2^2 V_2^4}{4 I_{0_2}^2}}\right) \tag{11}$$

Similarly with the basic circuit analysis, considering the more accurate expansion $\sqrt{1+x} \cong 1 + x/2 - x^2/4$, the output current of the multiplier from Figure 2 will have the following expression:

$$I_o \cong V_1 \sqrt{\frac{K}{a}}\left(bV_2 + cV_2^3 + dV_2^5\right) \tag{12}$$

where $b$, $c$ and $d$ are constants, expressed as:

$$b = \frac{K_1^{1/2} I_{0_1}^{1/2} - K_2^{1/2} I_{0_2}^{1/2}}{2} \tag{13}$$

$$c = \frac{K_2^{3/2} I_{0_2}^{-1/2} - K_1^{3/2} I_{0_1}^{-1/2}}{16} \tag{14}$$

$$d = \frac{K_1^{5/2} I_{0_1}^{-3/2} - K_2^{5/2} I_{0_2}^{-3/2}}{128} \tag{15}$$

Because the main nonlinearity from the output current expression is due to the third-order term of relation (12), the proposed linearization technique is referring to the cancellation of the third-order distortions, $c = 0$, equivalent with the following design condition:

$$\frac{I_{0_2}}{I_{0_1}} = \left(\frac{K_2}{K_1}\right)^3 \tag{16}$$

and, in consequence:

$$b = \frac{(K_1 I_{0_1})^{1/2}}{2}\left[1 - \left(\frac{K_2}{K_1}\right)^2\right] \tag{17}$$

$$d = \frac{K_1^{5/2} I_{0_1}^{-3/2}}{128}\left[1 - \left(\frac{K_1}{K_2}\right)^2\right] \tag{18}$$

The total harmonic distortion circuit for the new proposed circuit (approximated with the fifth-order one) will be:

$$THD_5 = \left(\frac{K_1^2}{8 K_2 I_{0_1}}\right)^2 V_2^4 = \left(\frac{K_1^2}{4 K_2 K_{0_1}}\right)^2 \left(\frac{V_2}{V_C - V_T}\right)^4 \tag{19}$$

Considering the particular case that $K_2 = K_{0_2}$ and $K_1 / K_2 = 1/2$, it results:

$$THD_5 = \frac{1}{256}\left(\frac{V_2}{V_C - V_T}\right)^4 \quad (20)$$

Thus, the linearity improvement of the new multiplier from the basic circuit is about two orders of magnitude:

$$\frac{THD_3}{THD_5} = 64\left(\frac{V_C - V_T}{V_2}\right)^2 \quad (21)$$

## III. EXPERIMENTAL RESULTS

### *THE BASIC CIRCUIT*

In order to estimate the circuit linearity, two identical sinusoidal signals $\omega_1 = \omega_2 = 2.5GHz$ were applied on the circuit inputs. The simulated output signal and its Fourier analysis are presented in Figure 3 and 4, respectively.

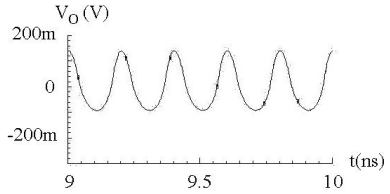


Figure 3: The output signal for the basic circuit ( $\omega_1 = \omega_2 = 2.5GHz$ )

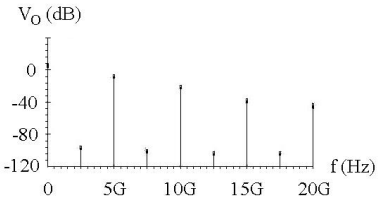


Figure 4: The Fourier analysis of the output signal for the basic circuit ( $\omega_1 = \omega_2 = 2.5GHz$ )

The simulated value of $THD$ for the basic circuit is $-16dB$. The multiplier supply voltage is $V_{CC} = 3V$.

The basic multiplier was also tested for different input signals, $\omega_1 = 2.5GHz$ and $\omega_2 = 2.25GHz$, resulting the output signals $\omega_1 - \omega_2 = 250MHz$ and $\omega_1 + \omega_2 = 4.75GHz$ (Figure 5).

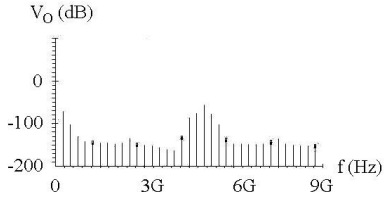


Figure 5: The Fourier analysis of the output signal for the basic circuit ( $\omega_1 = 2.5GHz$ and $\omega_2 = 2.25GHz$ )

### *THE NEW CMOS MULTIPLIER WITH IMPROVED LINEARITY*

The new proposed multiplier was tested for two different design conditions:

- The design condition (16) is respected by choosing $I_{0_2} / I_{0_1} = (K_2 / K_1)^3 = 8$ (balanced circuit); the effect is the canceling of the third-order harmonics; the simulation is presented in Figure 6;
- The design condition (16) is not respected by choosing $I_{0_2} / I_{0_1} = K_2 / K_1 = 1$ (unbalanced circuit); the effect is the impossibility of canceling of the third-order harmonics; the simulation is presented in Figure 7;

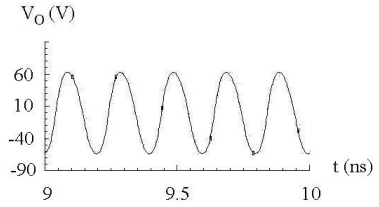


Figure 6: The output signal for the linearized balanced circuit

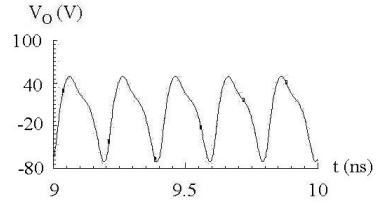


Figure 7: The output signal for the linearized unbalanced circuit

The total harmonic distortion circuit is increased for the unbalanced version even with respect to the basic circuit.

The Fourier analysis of the output signal for the balanced multiplier are presented in Figure 8 (for identical input signals $\omega_1 = \omega_2 = 2.5GHz$) and in Figure 9 (for different input signals, $\omega_1 = 2.5GHz$ and $\omega_2 = 2.25GHz$).

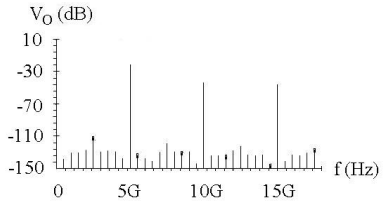


Figure 8: The Fourier analysis of the output signal for the linearized balanced circuit ( $\omega_1 = \omega_2 = 2.5GHz$ )

The simulated value of *THD* for the basic circuit is $-24dB$ .

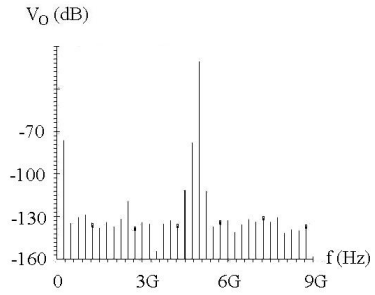


Figure 9: The Fourier analysis of the output signal for the linearized balanced circuit
( $\omega_1 = 2.5GHz$ and $\omega_2 = 2.25GHz$ )

The layout of the improved linearity multiplier is realized in $0.35\mu m$ CMOS technology (Figure 10). The utilization of the double-centroid structures and of the large transistor areas assures the reducing of the differential amplifiers' mismatches.

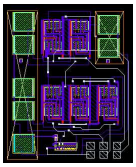

Figure 10: The layout of the improved linearity multiplier ( $0.35\mu m$ CMOS technology)

## IV. CONCLUSIONS

Based on a classical approach of a CMOS multiplier using MOS transistors in saturation, a new linearization technique has been proposed. It consists in replacing the simple differential amplifier from the basic circuit with a cross-connection differential amplifier. The result will be the reduction of *THD* by canceling the main nonlinear term (the third-order one) from the output signal expression.

The circuit was implemented in $0.35\mu m$ CMOS technology and it was supplied at $V_{CC} = 3V$ . The transient and Fourier analysis, made for high frequency input signals ( $\omega_1 = \omega_2 = 2.5GHz$ and $\omega_1 = 2.5GHz$ ; $\omega_2 = 2.25GHz$ ), confirm the theoretical results (a linearity improvement of about $8dB$ ). It is possible to obtain this reduction only for the balanced version of the improved multiplier, the unbalanced circuit showing an increasing of *THD* even with respect to the basic multiplier.

The reduction of *THD* for the balanced improved circuit is smaller than the theoretical estimated result because of the high frequency operation of the circuit, which introduce additional distortions due to the parasite capacitances, not considered in the previous analysis.

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