SYSTEMATIC IMPLEMENTATION METHOD OF LC-LADDER FILTERS BY MO-CCCII CIRCUITS

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ABSTRACT

The paper implements the well-known leapfrog method of LC-ladder filters simulation by circuits employing only multiple outputs second-generation current controlled conveyors (MO-CCCII) and grounded capacitors. The proposed method is general, because on a hand it implements any type of frequency behaviours and on the other side both all pole and finite-transmission-zeros passive filters are emulated. Using current controlled devices, the circuits are electronically tunable and do not require any matching constraints, making the approach extremely convenient for systematic design and dense layout. SPICE simulations made with circuits employing bipolar MO-CCCII demonstrate the validity of the approach.

I. INTRODUCTION

Over the last decade or so, current-mode (CM) filters using second-generation current conveyors (CCII) have received considerable attention owing to the fact that their bandwidth, linearity, and dynamic range performances are better than those of their op-amp based counterparts [1]-[3]. In many cases, the current conveyors simplify design in much same way as the op-amps, but it presents alternative ways for implementing analogue systems. It resulted in new methods which implement analogue transfer functions, giving advantages over voltage op-amp counterparts in terms of accuracy, bandwidth, convenience and simpler circuits.

With recently introduced second-generation current controlled conveyors (CCCII) [4], current conveyors' applications have been extended to the domain of electronically adjustable functions. Electronic adjustability is attributed to intrinsic resistance (R_o) at port X which depends on bias current I_o . Recently, designs of current controlled conveyors filters using multiple outputs CCCII (MO-CCCII) [3] [5], alleviate considerably the design of multi-loop filters. These devices have two or more high impedance positive/negative outputs and will be used in our designs.

This paper presents a general design method for CM ladder filters using only MO-CCCII and grounded capacitors. The method is based on operational simulation of RLC ladder prototypes. These active implementations share all the low sensitivity characteristics and low component spread of passive filter prototypes. These advantages are totally preserved in CM ladder active filter designs [6], [7].

Even if the technique of simulating LC ladder filters by their signal-flow graphs is very well established in the area of all-pole lowpass filters, our approach based on a systematic design procedure extends the applicability of leapfrog method to all types of frequency behaviours and transfer functions. The design procedure, designated by us as *Active Synthesis of Ladder Network Immitances*, was developed by Schaumann [8], [9] for voltage mode *Transconductor-Grounded Capacitor* (TGC) circuits and, as is shown in the paper, it can be successfully extended to the case of multi-output CM circuits.

The Schaumann approach is very methodical and simple to implement, attributes retained also in our MO-CCCII implementation. It synthesizes in our case, by simple and repetitive operations, the admittance/impedance of each arm of the passive network as a CM transfer function. As consequence, we are capable to emulate any passive ladder filter network configuration, which justifies the general character of the method. To demonstrate the validity of active synthesis method, one design example is presented, revealing some of the problems that arise during the synthesis process, due to the non-ideal character of bipolar devices used as current conveyors.

II. BIPOLAR DO-CCCII DESCRIPTION

A DO-CCCII or CCCII± is a MO-CCCCII with only two output terminals (Figure 1(a)). The ± sign indicates the output currents are in opposite direction. The ideal relationship between terminal currents and voltages is defined as:

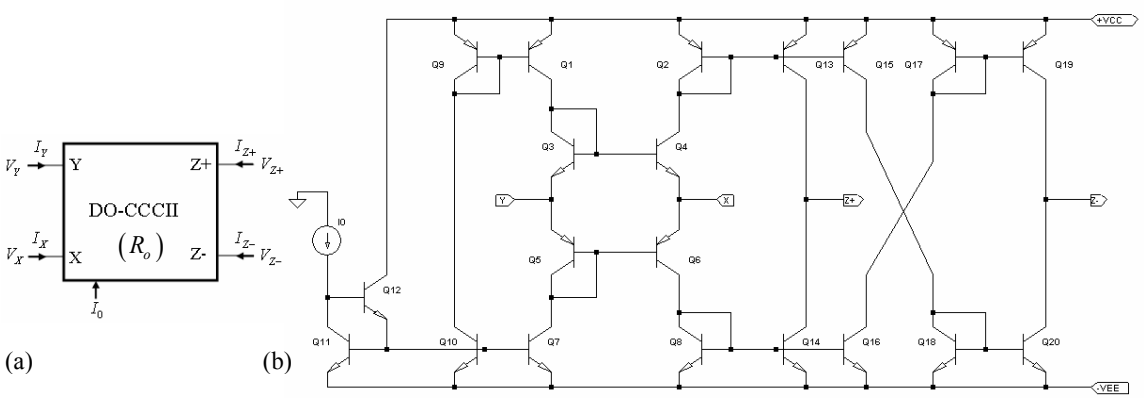

Figure 1(a) Block diagram of the dual-output second generation current conveyor (DO-CCII), (b) Schematic implementation of DO-CCCII using BJT.

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 1 & R_o & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

I_X, I_Y, I_{Z+}, I_{Z-} and V_X, V_Y, V_{Z+}, V_{Z-} in (1) denote currents respectively voltages at DO-CCCII terminals. By convention, a positive current indicates that the current flows in the device. R_o in (1) represents the input impedance at port X. For bipolar CCCII, the impedance is $R_o = V_T/(2I_0)$, where I_0 is the bias current of the conveyor and V_T is roughly 26mV at room temperature [4].

In an usual application, the current conveyor is used as a transconductance amplifier. The terminal X is grounded and the voltage input signal is V_Y, the output currents being given by

$$I_{Z\pm} = \mp V_Y / R_0 \quad (2)$$

If X becomes the input terminal and the port Y is grounded then the device acts as a current mirror with R_o as input impedance.

In order to estimate the correctness of the method and to evaluate the frequency domain performances of proposed circuits, we used the bipolar realization in Figure 1(b). The DC supply voltages are ±2.5V and the PNP and NPN transistors use the parameters of PR100N and NR100N bipolar transistors arrays [10].

A multi-output CCCII (MO-CCCII) has more than the two outputs of DO-CCCII, usually two (I_{Z1+} and I_{Z2+}) instead of I_{Z+} and other two (I_{Z1-} and I_{Z2-}) instead of I_{Z-}. All these outputs maintain ideally the same properties as the corresponding outputs of DO-CCCII, being obtained by current mirroring. Only the necessities of circuit synthesis dictate the number of outputs of a MO-CCCII.

III. ACTIVE SYNTHESIS METHODS

LEAPFROG SYNTHESIS PROCEDURES

As shown in Figure 2(a), an LC-ladder filter network can be characterized by the admittance blocks in the series arms and impedance blocks in the parallel arms. This representation leads to the corresponding signal-flow graph of Figure 2(b) in terms of node voltages ($v_i, v_2, v_4 \ldots$) and mesh currents ($i_1, i_3, i_5 \ldots$).

In our discussion throughout the paper, all RLC prototypes circuits are assumed to be normalized with respect to impedance level. Therefore the parameters and variables are dimensionless, the transmittances z_k and y_j in Figure 2(b) are current transfer functions and v_k is to be

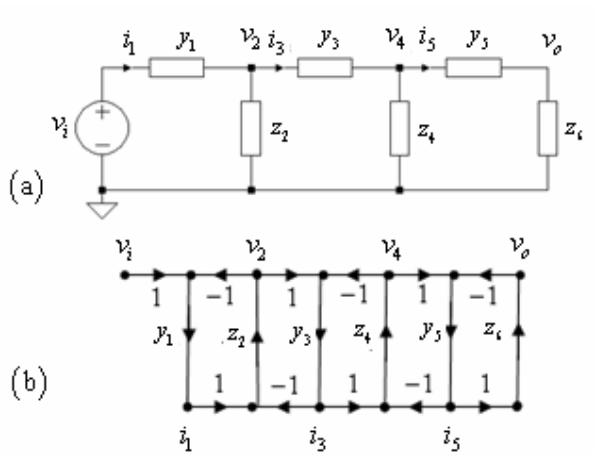

Figure 2 (a) General LC-ladder filter schematic (b) Its signal-flow graph.

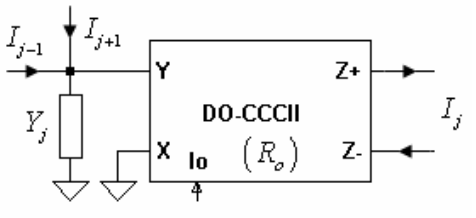

Figure 3. Basic MO-CCCII circuit block.

interpreted as a current signal regardless of notation. Any circuit realizing the same signal-flow graph as the LC-ladder filter independent of node variable names obviously realizes the same current transfer function. Thus, the design is reduced to the synthesis of active filter subcircuits that simulate the normalized immitance functions of RLC circuits (the transmittances in the graph) by current transfer functions. The synthesized circuit will implement also the subtractions in the nodes of the graph by using the opposite sign outputs of MO-CCCII circuits.

ACTİVE SYNTHESİS OF ONE-PORT IMMİTANCES

In this paper, the current summers and current transfer functions of Z_k and Y_j (which substitute z_k and y_j in passive network) are synthesized using MO-CCCII circuits and grounded capacitors. The basic circuit is built around a DO-CCCII and a grounded admittance as Figure 3 shows, and its current transfer functions emulates completely the operations realized across a node in the graph in Figure 2(b):

$$I_j = \frac{1}{R_o Y_j}\left(I_{j-1} + I_{j+1}\right) \tag{3}$$

In a practical LC-ladder filter, the circuit branches shown in Figure 2(a) typically consist of series and parallel combinations of inductors, capacitors and possibly resistors. In general, the branch immitances functions y_i and z_i of the RLC oneports under consideration can be mathematically expressed in the form of a continuous fraction expansion:

$$F(s) = k_{01}^r s + k_{01}^c + \cfrac{1}{k_{02}^r s + k_{02}^c + \cfrac{1}{k_{11}^r s + k_{11}^c + \cfrac{1}{k_{12}^r s + k_{12}^c + \cfrac{1}{k_{21}^r s + k_{21}^c + \cfrac{1}{k_{22}^r s + k_{22}^c + \cfrac{1}{\cdots}}}}}} \tag{4}$$

where k_{ij}^r and k_{ij}^c are real positive constants that correspond to inductor/capacitor and resistor/conductor, respectively depending on the position in the original network. In the same way, $F(s)$ represents the impedance/admittance of a parallel/series branch of the ladder. The expression (4) is general and some coefficients may be zero or infinity depending on the particular case.

The main goal of this paper is to prove the possibility to implement $F(s)$ in (4) by CM circuits containing grounded capacitors and MO-CCCII. On this basis resides the general nature of CM leapfrog procedure developed in this paper.

The realization of $F(s)$ in (4) as a current transfer function implies the possibility to perform repeatedly in the implementing circuit the mathematical operations

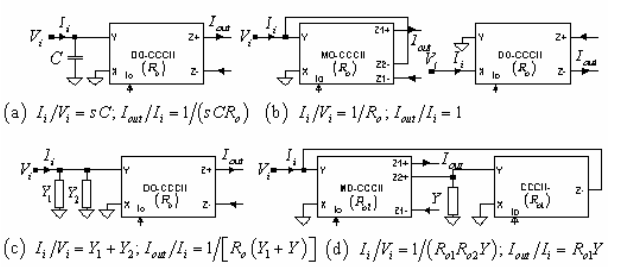

Figure 4. Fundamental circuit structures implementing (a) a grounded capacitor and (b) a constant. Realization of a CM transfer function by (c) addition and (d) inversion.

involved in writing the expression: addition and inversion. These operations are executed on two fundamental circuit structures presented in Figure 4(a) and (b). The transfer function of circuit in Figure 4(a) is inverse proportional with s while the circuits in Figure 4(b) are used to implement the equivalent of a grounded resistor of unity value or a unitary CM transfer function. If a different value resistor must to be implemented, a second CCCII circuit is needed, as will be shown further down. In this last case, the value of the resistor dictates the bias current ratio of conveyors.

As is obvious from our previous statements, the MO-CCCII-grounded capacitors circuit elements are important not only for their CM transfer function but also for the input admittance, the inverse of the first function. Addition of two or more admittances ensued by inversion as current transfer function is given quite simply by the circuit in Figure 4(c). Finally, Figure 4(d) presents the way used to invert the input admittance or the CM transfer function. As a conclusion, the active synthesis of a RLC immitance is made using the fundamental admittances presented in Figure 4(a) and (b) and alternating the operations of addition and inversion shown in Figure 4(c) and (d) performed with the object to implement the continuous fraction expansion of the one-port immitance in (4) by a current transfer function.

Figure 5 (a) and (b) illustrates a simple application of synthesis procedures. The first-order current transfer function from this case is the inverse of the sum of two fundamental admittances: a grounded capacitor and a grounded conductance represented by one of the circuits represented in Figure 4(b). Both circuits present very similar frequency characteristics, with a slight advantage for the circuit in Figure 5(a). Figure 5(b) is a good example for the benefits of the use of multi-outputs

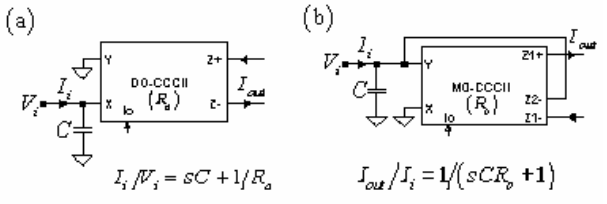

Figure 5. First order current transfer function circuits implemented by active synthesis procedures of one-port immitance.

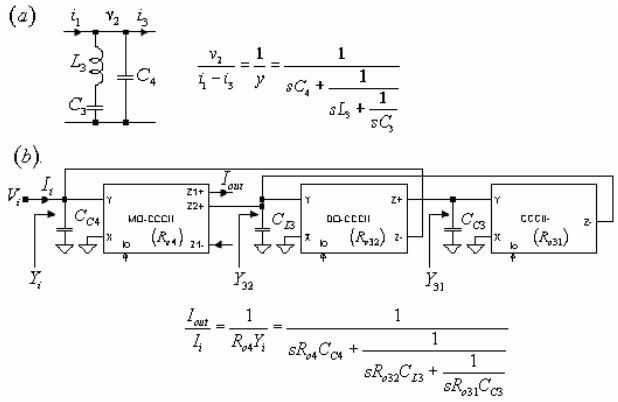

Figure 6 (a). Typical branch of an LC-ladder network and (b) MO-CCCII grounded capacitors subcircuit which implements the transmittance of (a).

current conveyors in active synthesis of one-port immitances. In place of two current conveyors, the first one needed to implement the active conductance and the second one to realize the addition of two conductances; it uses a single MO-CCCII to emulate both actions.

The next example shown in Figure 6 is taken from [8] and illustrates perfectly how the alternation between admittances and CM transfer functions realizes the synthesis process. The transmittance function of the ladder shunt arm in Figure 6(a) is given in the figure. The design starts with the "lowest" level of the immitance, (e.g. in our case with the admittance $Y_{31} = sC_{C3}$). It continues firstly by taking the reciprocal of the admittance by the circuit CCCII- (R_{o31}) and secondly by adding sC_{L3} to the first result. It gives

$$Y_{32} = sC_{L3} + \frac{1}{sC_{C3}R_{o31}R_{o32}} \tag{5}$$

The admittance Y_{32} is again inverted and converted subsequently in admittance to be finally added to sC_{C4} at the input of MO-CCCII (R_{o4}) as Figure 6(b) shows. The ratio between the output currents of the circuit and the input current represents the implemented transmittance function.

IV. EIGHTH-ORDER ELLIPTIC BANDPASS FILTER SIMULATION

In the following, a non-trivial example will be presented in order to prove the correctness of the synthesis method and to test the capabilities of the bipolar devices used to implement the current conveyors. The eighth-order elliptic bandpass LC-ladder prototype given in Figure 7(a) was used also in [8]; therefore we can compare the performances of our MO-CCCII synthesis method with the original synthesis realized with single output OTA and grounded capacitors both as efficiency of implementation and as performance of active devices involved.

The simulation of the passive network in Figure 7(a) means to synthesize MO-CCCII subcircuits that emulate

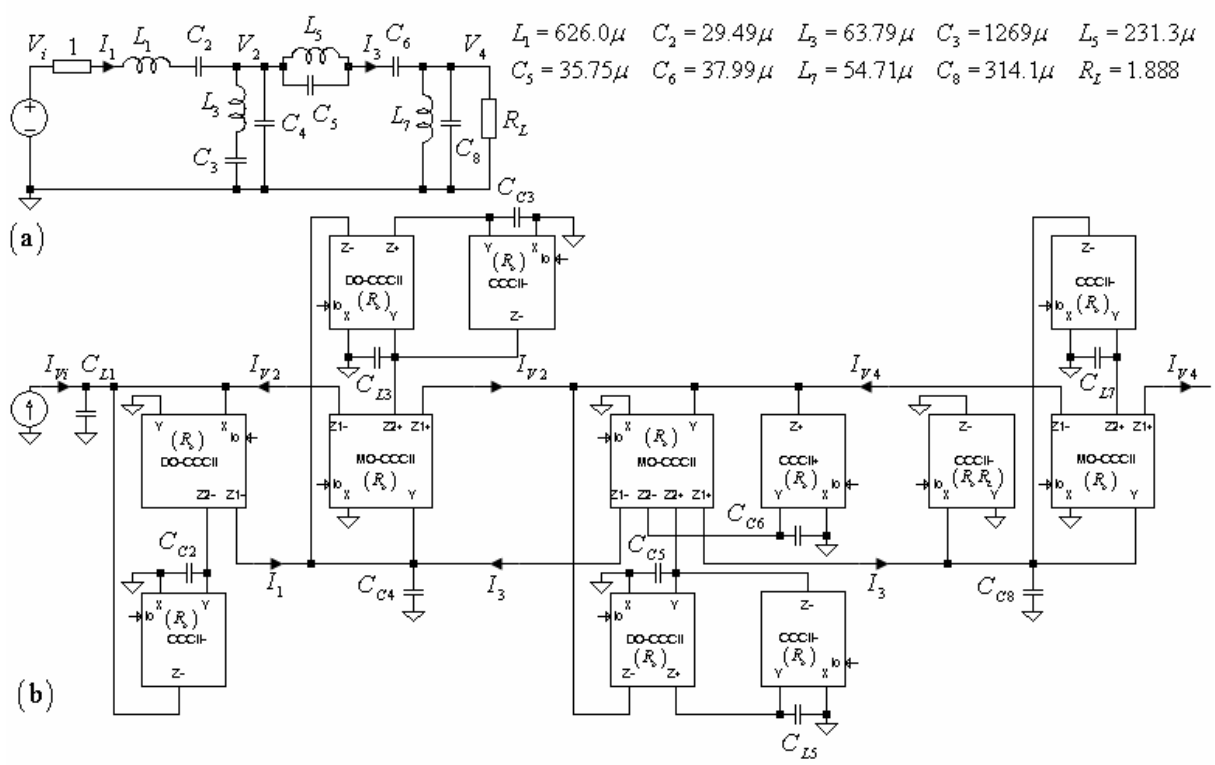

Figure 7. (a) Eighth-order elliptic bandpass LC-ladder prototype filter. (b) MO-CCCII-grounded capacitors filter simulation of the passive network.

the admittances of the series arms and the impedances of shunt arms as current transfer functions. The shunt arm consisting of C_3, L_3 and C_4 was realized in the earlier example of Figure 6. In the same way, i.e. alternating between implementations of input admittance functions and current transfer functions of MO-CCCII circuits by using addition and reciprocation as main synthesis operation, is obtained the active filter that implements the passive network. Figure 7(b) contains the final network. The design is made by choosing a unique value, I_o for the bias currents of all current conveyors in Figure 7(b), with the exception of final stage CCCII- which is used to emulate the non-unity termination resistor R_L. The bias current of this device is I_o/R_L. Once the bias current is established, denoting by C_{Lj} the capacitor in Figure 7(b) which corresponds to L_j in Figure 7(a), is

$$C_{Lj} = 2I_o L_j / V_T \tag{6}$$

The nominal passband is designed to be between 50kHz and 70kHz. The range of optimal values of bias currents for these frequencies is between 2μA and 20μA. Figure 8 shows simulated and ideal filter response obtained through a SPICE simulation of circuits in Figure 7 for $I_o = 7.5\mu$A. The window in Fig. 8 presents the results of simulation for three different values of I_o, revealing the sensitivity of magnitude characteristics in the passband to this parameter. Both the high sensitivity and the slanted character of the passband resides in the first place, in the input impedance at port Y, which is highly dependent on bias current and has an important capacitive character. In a certain extent to this result contribute also the non-ideal current gain of MO-CCCII and the finite output impedance of the device. The way to reduce these deviations is to use more performing devices as current conveyors.

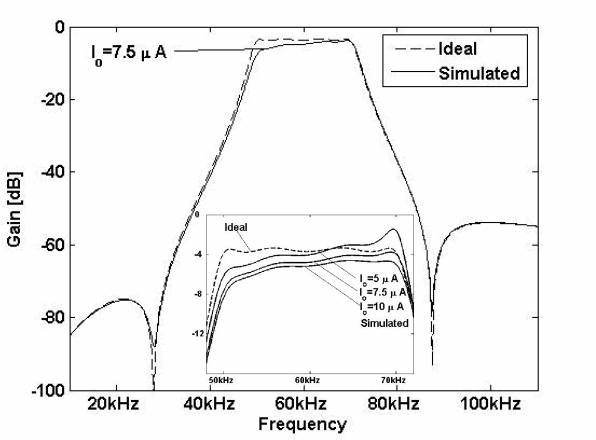

Figure 8. Ideal and simulated magnitude characteristics of MO-CCCII filter realizing the eighth-order elliptic LC-ladder prototype filter.

V. CONCLUSION

The main goal of this paper was the development of general simulation method of LC-ladder filters by active CM circuits containing only multi-output second generation current conveyors (MO-CCCII) and grounded capacitors. The validity of the design procedure was proved on some nontrivial design examples using bipolar current controlled conveyors as simulation vehicles. The deviations from ideal behaviour stem from the non-ideal performances of the bipolar devices and can be reduced by the use of better devices and active compensation techniques.

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