Four Quadrant FGMOS Multiplier

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Abstract

A novel four-quadrant analog multiplier using floating gate MOS (FGMOS) transistors operating in the saturation region is presented. The drain current is proportional to the square of the weighted sum of the input signals. This square law characteristic of the FGMOS transistor is used to implement the quarter square identity by utilizing only six FGMOS transistors. The main features of this remarkably simple multiplier circuit configuration are the large input signal range equal to 100% of the supply voltage, nonlinearity of 0.0078% and THD of maximum 2.74% (while the inputs are at their maximum values).

1. Introduction

Four quadrant analog multipliers are important building blocks in neural networks and many signal processing circuits like correlators, convolvers, adaptive filters, modulation detection, frequency translation, etc. Several techniques of implementing four-quadrant analog multipliers, using MOS technology, have been reported. They are the variable transconductance technique (modified Gilbert cell) [1]-[3], the voltage-controlled transconductance technique, which employs MOS transistors operating in the triode region [4]-[6], the bias feedback technique [7], techniques based on square-law characteristics of MOS transistors operating in the saturation region, implementing either the quarter-square identity [8]-[10] or other algebraic identity [11]-[12], and the technique based on linear transconductors [13]-[15]. The Gilbert six transistors cell (GSTC), using the variable transconductance technique, is very popular in bipolar technology since its output current has a linear relationship with the tail current source which allows the nonlinear relationship with the input signals, *Vx* and *Vy,* to be compensated simply by an appropriate predistortion circuit [16]. However, the output current of a MOS transistor multiplier, based on the modified GSTC, has a nonlinear relationship with the tail current source and makes compensation by a predistortion circuit very difficult [2]. This limits the linear input range of the multiplier to only a few hundred millivolts [l]. On the other hand, most of the square-law based multipliers reported so far have input signal range limited to about 50% of the supply voltage range. In this paper, a novel four-quadrant analog multiplier using floating-gate MOS (FGMOS) transistors operating in the saturation region is presented. The drain current is proportional to the square of the weighted sum of the input signals. This square law characteristic of the FGMOS transistor is used to implement the quarter square identity by utilizing only six FGMOS transistors. The main features of this remarkably simple multiplier circuit configuration are the large input signal range equal to 100% of the supply voltage, nonlinearity of 0.0078% and THD of maximum 2.74% (while the inputs are at

their maximum values). Rest of the paper is organized as follows. In Section II, the basic structure of the FGMOS transistor is described. The principle of operation of the FGMOS differential pair and four-quadrant analog FGMOS multiplier are presented in Section III and Section IV, respectively. Simulation results of the proposed circuit are shown in section V followed by conclusion in section VI.

2. The FGMOS Transistor

Floating gate (FG) MOSFETs are being utilized in a number of new and exciting analog applications [17]-[20]. These devices are available in standard CMOS technology because they are being widely used in digital circuits. Thus floating gate devices are now finding wider applications by analog researchers. As a result the floating gate devices are not only used for memories but are also being used as circuit elements. FGMOS transistors are used as analog memory elements, as part of capacitive biased circuits, and as adaptive circuit elements [17].

An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and electrically isolated from it. These inputs are only capacitively connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node [17]. The equivalent schematic for an n-input n-channel FGMOS transistor is given in Figure 1.
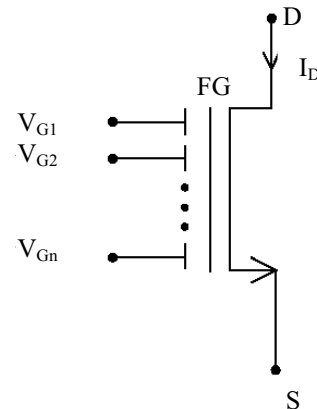

Fig. 1. n-input n-channel FGMOS transistor

3. FGMOS Differential Pair

There are two types of FGMOS differential pair. One of them is biased by floating voltage source and the other is biased by non-floating voltage source [18]. Differential pair which is biased by floating voltage source cannot have a rail-to-rail range and the

floating voltage source may limit its common mode swing range if the floating voltage source cannot swing out of the supply rails. Figure 2.a and 2.b shows the differential pairs biased by floating voltage source and non-floating voltage source, respectively.
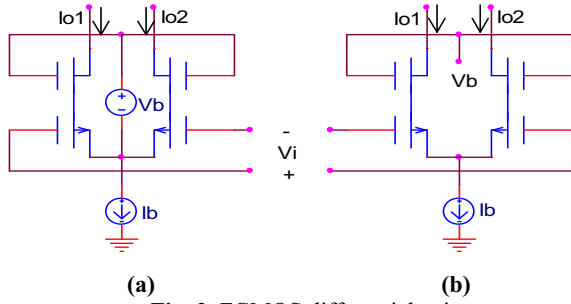

Fig. 2. FGMOS differential pairs

To derive under what condition we can get a rail-to-rail input common mode range for the differential pair biased by non-floating voltage source, it is known that for 2-input floating gate transistors $V_F = w_0V_0 + w_1V_1 + w_2V_2$ where $w_i = C_i / C_{tot}$, $i = 0, 1, 2$. Normally, C_i is much larger than C_0 which means w_0 is very small and the following approximation of $w_1 + w_2 = 1$ can be assumed. When V_{icm} (common mode input voltage) is V_{DD}, for N type transistor, the floating gate can be V_{DD}, as long as the V_{DRAIN} is greater than $V_{DD} - V_{TN}$. So, for the differential pair biased by non-floating voltage source, V_b can directly be V_{DD}. When V_{icm} is at the negative rail ($-V_{SS}$), for N type differential pair, there is a tendency that tail current transistor will have no room to work in saturation region. We should try to increase $V_{FG,cm}$, the common mode voltage on the floating gate. $V_{FG,cm}$ is given by $V_{FG,cm} = w_1V_{icm} + w_2V_b$. That is, one should have a high V_b, which has the maximum value of V_{DD}. Let $V_b = V_{DD}$; so, when $V_{icm} = -V_{SS}$, $V_{FG,cm} = w_1V_{icm} + w_2V_b = -w_1V_{SS} + w_2V_{DD} = -w_1V_{SS} + (1-w_1)V_{DD} = V_{DD} - w_1(V_{SS} + V_{DD})$. To make sure M_1, M_2 and tail current transistor work properly, the following inequality should be satisfied. $V_{FG,cm} \geq -V_{SS} + (V_{GS,M1,M2} + V_{dsat, MTAIL})$. So, we can get from these two equations, $(V_{DD} + V_{SS}) \geq (V_{GS,M1,M2} + V_{dsat, MTAIL}) / (1 - w_1)$. The minimum supply voltage is $(V_{GS,M1,M2} + V_{dsat, MTAIL}) / (1 - w_1)$ [18].

Figure 3 shows the output drain current of the differential pair biased by non-floating voltage source. As it is seen from the figure, input voltage swing is increased by using FGMOS transistors.
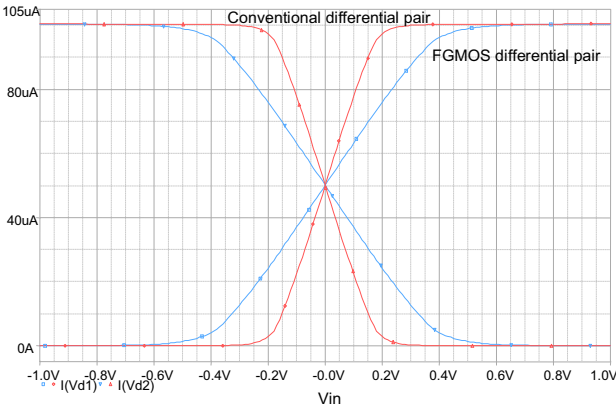

Fig. 3. Output drain current of the differential pair biased by non-floating voltage source

4. Four Quadrant FGMOS Multiplier

Figure 4.a shows the conventional multiplier circuit based on the folded CMOS Gillbert Cell while Figure 4.b shows the proposed floating gate multiplier circuit which is based on the topology given in [2], employing FGMOS differential pairs instead of conventional pairs to improve the circuit behaviour. M1a, M1b transistors form one differential pair where as M2a, M2b form the other. They are cross connected by connecting the drains of the transistors M1a, M2a and M1b, M2b together. A differential input V_X is applied to the cross connected differential pairs while the other differential input V_Y is applied to the differential pair formed by M3a and M3b. M3a and M3b transistors form tail transistors for the two differential pairs. The bias currents (I_{SS1}, I_{SS2}, I_{SS3}) are provided as tail currents to the differential pairs.
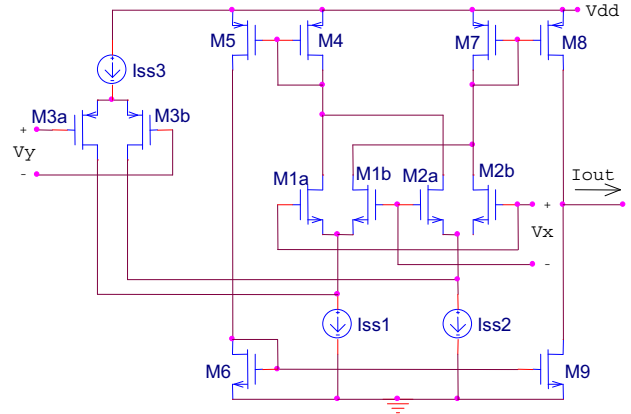

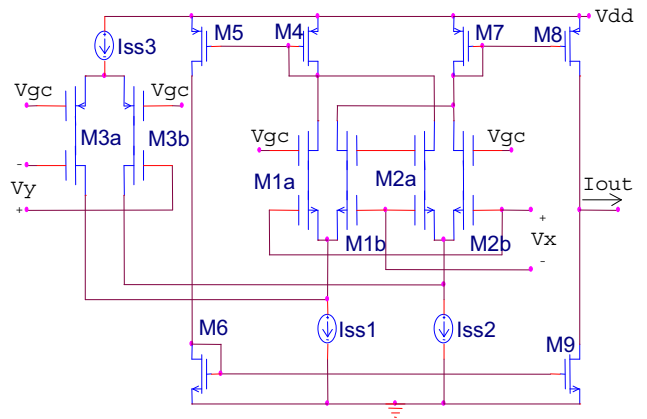**Fig. 4.a.** Conventional multiplier circuit

Fig. 4.b. Proposed floating gate multiplier circuit

Each transistor in differential pairs has two inputs which are applied through two equal sized capacitors, C_i. The differential signals of the inputs are applied to one of the floating gates in the differential pairs. V_X and V_Y act as input signals while V_{GC} as a control voltage to the floating gates. Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

5. Simulation Results

The proposed circuit of Figure 4.b was simulated using 0.5μm Mietec technology parameters. The supply voltage is $V_{DD}=2.5V$, V_{GC} is set to V_{DD} for n type FGMOS and is set to ground for p type FGMOS. The tail currents are $I_{SS1}=I_{SS2}=I_{SS3}=100$ μA. The input capacitor value is taken $C_i = 25$ fF while the C_{FGD} and C_{FGS} values are calculated as 0.14 fF and 2.45 fF, respectively. The dimension for cross connected differential pair transistors M1a, M1b, M2a and M2b is W / L = 1 μm / 1 μm, for M3a and M3b is W / L = 5 μm / 1 μm. The current ratio of the transistors M4, M5 and M7, M8 is chosen as $I_{D5} / I_{D4} = I_{D8} / I_{D7} = 5$.

Figure 5 shows the DC transfer characteristics of the proposed circuit. DC voltage V_Y was stepped between -1.25V and 1.25V with 0.5V step size while the DC voltage V_X was swept from -1.25V to 1.25V. The nonlinearity of the circuit was simulated as 0.0078% under full scale input conditions.
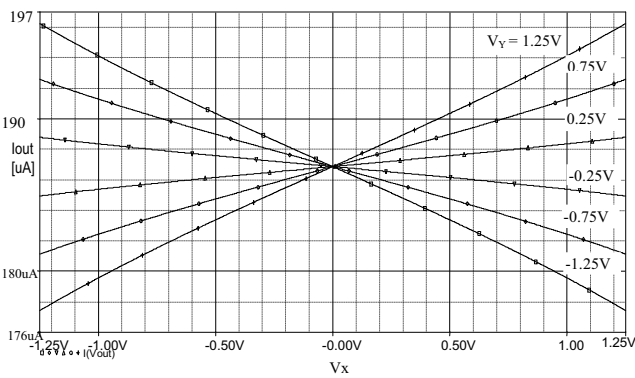

Fig. 5. DC transfer characteristics of the proposed circuit

Figure 6 shows the DC transfer characteristics of the proposed circuit and the conventional CMOS circuit together. During the simulation V_X is swept from -1.25 V to 1.25 V while V_Y takes the values of -1.25 V, 0 V, 1.25 V for proposed circuit and -0.11 V, 0 V, 0.11 V for the conventional CMOS circuit. As it is seen from the figure, input swing is increased by using FGMOS transistors.
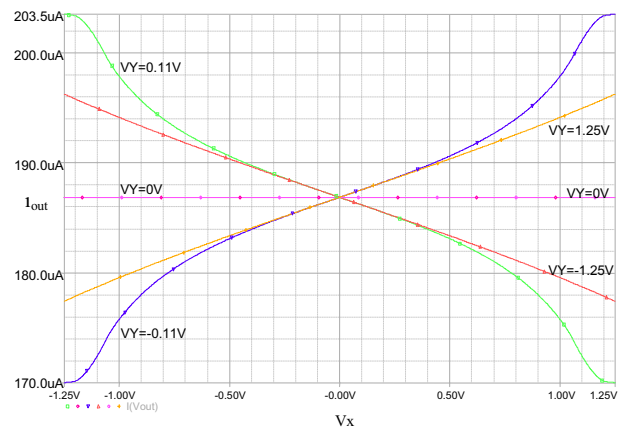

Fig. 6. DC transfer characteristics of the proposed multiplier circuit and the conventional multiplier circuit

Figure 7 shows the inputs of 10 kHz and 300 kHz sinusoidal signals with 2.5 V amplitudes applied at V_X and V_Y, respectively and Figure 8 shows the transient output waveform of the proposed circuit.
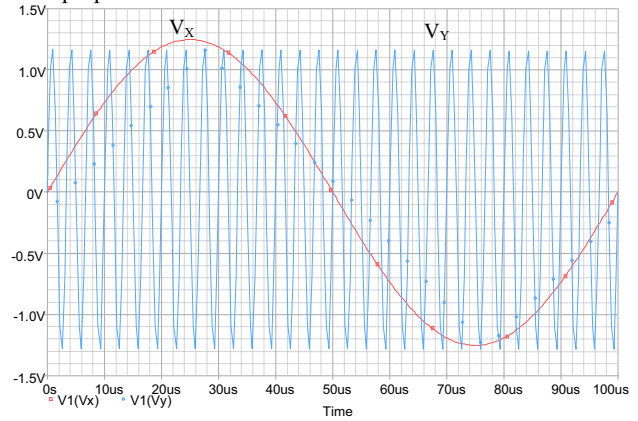

Fig. 7. Input signals V_X and V_Y of the proposed circuit
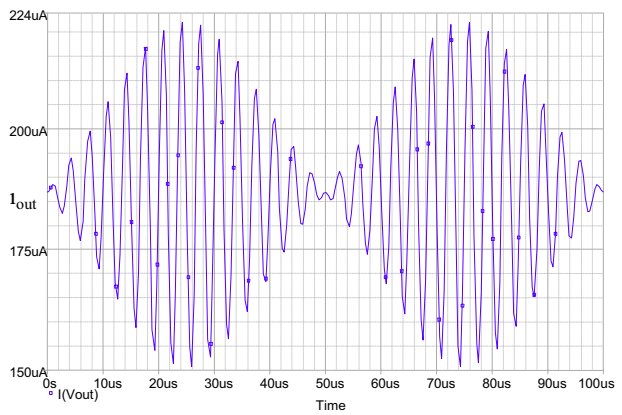

Fig. 8. Transient output waveform of the proposed circuit

Figure 9 shows the THD variation due to the input voltage swing of V_Y between 0 V and 2.5 V while V_X is set to 0.5 V, 1.5 V, 2 V and 2.5 V DC. As it is seen from the figure, if we consider a constant V_Y, THD increases while V_X increases or if we consider a constant V_X THD increases while V_Y increases.
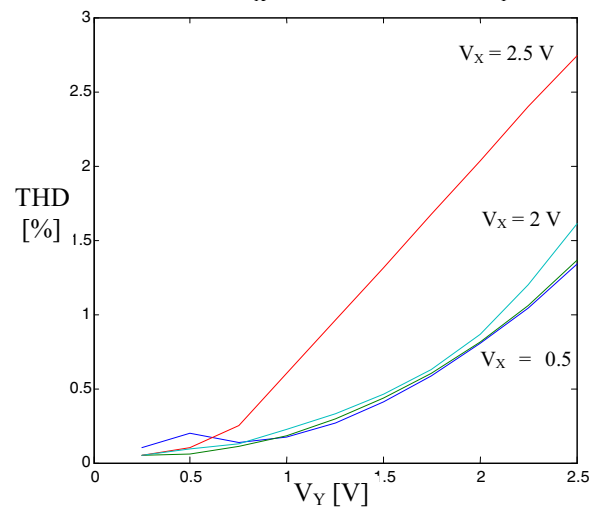

Fig. 9. THD variation due to the input voltage swing of V_Y while V_X is set to 0.5 V, 1.5 V, 2 V and 2.5 V DC

The extended linearity provided by the proposed circuit has been demonstrated on the intermodulation distortion properties by applying 10 kHz and 300 kHz signals of 2.5 V amplitude respectively to the X and Y inputs, the resulting output products are investigated by SPICE simulations. Intermodulation products of the frequencies f1 + f2 = 310 kHz and f1 - f2 = 290 kHz are taken as 0 dB and the other products are normalized to those values. The intermodulation products obtained are illustrated in Table 1. It is obvious from the results that the intermodulation products at the output of the proposed circuit of Fig.4.b are considerably lower than those at the output of the conventional multiplier topology of Fig.4.a.

Table 1. Intermodulation Products of the Proposed Multiplier and Conventional Multiplier

Frequency [kHz]	Proposed Multiplier	Conventional Multiplier
10	-78.96 dB	-45.3 dB
30	-81.88 dB	-52.01 dB
50	-83.86 dB	-49.32 dB
270	-22 dB	-13.32 dB
290	0 dB	0 dB
300	-77.21dB	-34.81 dB
310	0 dB	0 dB
330	-22 dB	-13.32 dB

6. Conclusions

A novel FGMOS four quadrant multiplier has been designed and simulated. It is based on the square law dependence of the drain current on the weighted sum of the input signals. The circuit configuration is remarkably simple. It has a large input voltage range equaling the supply voltage. The measured nonlinearity and total harmonic distortion are 0.0078 % and 2.74 % under full scale input conditions, respectively.

7. References

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