MOSFET MODELING WITH EKV 2.6 AND ANALOG CIRCUIT DESIGN STRATEGY FOR PERFORMANCE ESTIMATOR TOOL

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ABSTRACT

This paper describes a design methodology for a performance estimator which can be part of an analog design automation system. The method is based on using the analytical equations of the EKV transistor model to estimate the behaviour of some basic analog blocks. Extensive verification of the estimator has been performed and the estimates were shown to be reasonably accurate.

I. INTRODUCTION

Time to market is an important factor in IC manufacturing and a big pressure on all designers. However, analog design lacks Computer Aided Design (CAD) tools which reduce the effort for the design. These tools have been necessary to increase designer productivity and various analog design automation tools such as the tool proposed in [1] have recently started appearing in the open literature. This tool consists of seven major "hierarchical synthesis blocks" as observed from Figure 1.1.

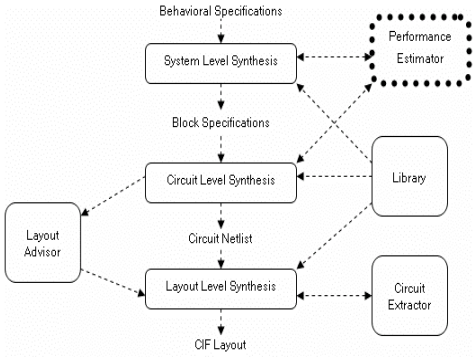

Figure 1 Analog Design Flow

The performance estimator is a crucial part of analog design automation. Utilization of the performance estimator is important to speed up the operation of the system level synthesis tool by allowing evaluation of design alternatives without having to synthesize each circuit. Thus, infeasible specifications can be eliminated straightaway and the other alternatives can be evaluated much faster and the best architectures at the system level can be obtained.

In this work, the main goal is to model the analog blocks which use the analytical design equations of the EKV 2.6 mosfet model parameters. After modelling the devices, our design strategy will be applied to some basic analog blocks and the results will be shown to be reasonably accurate

Section 2 defines the performance estimation problem briefly. Section 3 describes the EKV model, whereas Section 4 discusses the design methodology employed in this work. Details and results for each analog block are provided in Section 5. This section also illustrates the design strategy for a Basic Two Stage (BTS) OPAMP. Section 6 concludes the paper.

II. PERFORMANCE ESTIMATION PROBLEM

The performance estimator works on a pre-defined circuit topology, taking in some performance parameters as variables, and estimating the remaining parameters. One can denote P_i as a performance criterion of any analog circuit such as gain, bandwidth, slew rate, output resistance, etc. and I_i as an independent circuit parameter determining the performance such as the W or L of the MOSFET, etc. Performance of the circuit can be defined by (1) where f_i are the functions linking performance parameters to the independent variables.

$$\begin{aligned} P1 &= f1(I1,I2,.....Ij), \\ P2 &= f2(I1,I2,.....Ij), \\ &\vdots \\ Pi &= fi(I1,I2,.....Ij). \end{aligned} \quad (1)$$

The problem is to find an expression or at least an estimate for P_i in terms of each other without having to calculate I_j. In general, the functions f_i are non-linear and most of the time implicit. From this definition, the difficulty of the problem is obvious. One solution would be to form a look-up table for all combinations of I_j once and the required P_i must be searched from the table every

time. Although forming a look-up table should be the simplest solution, the size of the table is prohibitive and increases exponentially with the number of transistors. Furthermore, this table has to be generated for every technology change.

Prior to this work, different estimators have been developed by our research group. The estimator in [2] models transistors with neural networks, thus obtaining continuous and fast models for transistors. Using these models, lookup tables can be formed very efficiently. However, despite many heuristics employed, the performance tables turn out to be still too large. The estimator in [3] uses the same idea as in this work, but BSIM3v3 MOSFET models were used while modeling the analog blocks. The discontinuities and large number of parameters in the model created many problems for the estimator, thus providing the motivation for this work.

In this study, the performance estimator was shown to be quite accurate against the HSPICE simulator. The estimator equations are derived manually; however, infeasible solutions are eliminated immediately to obtain the feasibility region. Furthermore, linearization is used only for small signal analysis. While designing the performance estimator, the important part is how to model the devices and how to design analog blocks. In this paper, modelling of the devices and the design strategy will be described.

III. EKV MOSFET MODEL

EKV Mosfet Model is a fully analytical model dedicated to the design and analysis of low-voltage, low-current analog circuits [4]. Continuity is the significant point of the model. All the large and small signal variables such as the currents, the intrinsic capacitance, transconductance, etc. are continuous in all regions of operation including weak inversion, moderate inversion and strong inversion. The model is based on the inversion charge Q'_i. which is controlled by the voltage difference V_p-V_{ch}. The gate voltage where the inversion charge is zero is defined as the pinch-off voltage, V_p and the various operation points of transistors are then expressed in terms of voltages V_p-V_s and V_p-V_d [4]. Pinch off voltage and gate voltage equations are derived as in (2) and (3). ψ_0, γ, V_{to} are the model parameters.

$$V_P = V_G - V_{to} - \gamma \left[\sqrt{V_G - V_{to} + \left(\sqrt{\psi_o} + \left(\frac{\gamma}{2} \right)^2 \right)} - \left(\sqrt{\psi_o} + \left(\frac{\gamma}{2} \right) \right) \right] \quad (2)$$

$$V_G = V_{to} + V_P + \gamma \left[\sqrt{\psi_o + V_P} - \sqrt{\psi_o} \right] \quad (3)$$

Using classical BSIM models, one is faced with the disadvantage of three equations for three different operating regions and discontinuities. EKV model gives the opportunity of using a single I_D equation which is valid in all regions. . I_D is derived using the charge sheet model with the aasumption of constant doping in the channel and is expressed as the difference between I_F, forward current and a reverse component I_R. As mentioned before, I_D is also proportional to voltages V_P-V_S and V_P-V_D and a normalization current I_S.

$$I_D = \beta \int_{V_S}^{V_D} \left(\frac{Q'_i}{C'_{ox}} \right) dV_{ch} = \beta \int_{V_S}^{\infty} \left(\frac{Q'_i}{C'_{ox}} \right) dV_{ch} - \beta \int_{\infty}^{V_D} \left(\frac{Q'_i}{C'_{ox}} \right) dV_{ch} \quad (4)$$

$$I_D = I_F (V_P - V_S) - I_R (V_P - V_D) \quad (5)$$

V_P and N factors which are specific to the EKV model can be physically derived from the charge-sheet formulation . EKV model proposes the following I_D empirical expression valid and continuous for all regimes of operation [4].

$$I_D = 2N\mu C_{ox} \left(\frac{W}{L} \right) Ut^2 \left[\ln^2 \left(1 + e^{\left(\frac{VP - VS}{2Ut} \right)} \right) - \ln^2 \left(1 + e^{\left(\frac{VP - VD}{2Ut} \right)} \right) \right] \quad (6)$$

$$I_S = 2N\mu C_{ox} \left(\frac{W}{L} \right) U_t^2 \quad (7)$$

IC is the inversion coefficient given by I_D/I_S where I_S is the normalization current [5]. Large values of IC indicate strong inversion, whereas small values correspond to weak inversion.

IC > 10	Strong Inversion	
0.1 <IC< 10	Moderate Inversion	(8)
0.1 >IC	Weak Inversion	

Using the inversion coefficient IC, design parameters such as output conductance, bias voltages, width of the transistor, current etc can be derived. For example, the EKV model provides a simple expression for the G_m/I_D ratio of the MOS transistor. The formula;

$$\frac{G_m}{I_D} = \frac{1 - e^{-\sqrt{IC}}}{NUt\sqrt{IC}} \quad (9)$$

is precise and continuous throughout all the regimes. Experimental results show that G_m/I_D ratio is valid for all MOSFETs in a wide range of technologies [6]. Pinch off voltage and width of the transistor equations are given in (10) and (11).

$$V_P = 2U_t \ln(e^{\sqrt{IC}} - 1) \quad (10)$$

$$W = I_D L / (2N\mu C_{ox} IC U_t^2) \quad (11)$$

Although EKV 3.0 shows even better $(G_{md}.Ut)/I_D$ modelling with IC and L, we use EKV 2.6 model because EKV 3.0 parameters were not available at the time of the study.

IV. DESIGN STRATEGY

In our design strategy, we can estimate design parameters such as width of the transistors, bias voltages, current etc using gain, bandwidth, slew rate and output load. This technique gives the analog circuit designer the freedom of adjusting the other specifications such as phase margin, CMRR, offset voltages, noise etc. by evaluating the estimated solution set. In addition to this, this technique speeds up the design process by eliminating infeasible solutions automatically.

Supply voltages and MOSFET technology parameters are fixed throughout the design of the circuit. Although finding specific device sizes and bias voltages are not the point of the estimator tool, our design solutions are quite accurate and adjusting some estimated values in a very small range, we can find specific device sizes. However, this should rather be performed by a circuit synthesizer as shown in Figure 1. Nevertheless, the estimated solutions can be used as a starting point for the circuit synthesizer.

The 'divide and conquer' method, which means partitioning the main analog circuit into its analog building blocks, can be utilized to this end. Modeling each analog block with its simple equations analytically, it is easier to translate the input specifications of the main analog system to its blocks so that the problem will be partitioned to its lowest parts. For example, a typical BTS OPAMP (Figure 3) is composed of four analog building blocks; namely, differential input pair, current mirror, common source driver and a current source. Shifting the focus to one higher level, only two blocks are present: a differential input pair and a push-pull output stage. The methodology when designing a large circuit will be to begin from the last block and move backwards until the first one. A performance estimator that can work on most typical circuits should model several versions of common source gain stages, current mirrors, differential pairs, source followers, and cascode structures. Based on these blocks, two typical circuits were modeled; namely, a BTS and a cascode OPAMP. In this work, only the BTS OPAMP is presented.

Using IC, design parameters such as I_D, G_m, W etc can be calculated. For instance, by sweeping IC values from 0.1 to 100, a huge number of G_m/I_D values can be found related to (9).

The design strategy was coded in the C++ programming language. Model equations are implemented in the code which takes the performance parameters as input and provides the estimation results, solution sets, or optimum results as output.

```
Chose one of the below options
        1. Display Results for fixed IC values
        2. Create Output Files Solution Set
        3. Create Output Files Optimum Solution Set
        4. Exit
2
Chose one of the below options
                1. Area-Power solution set
                2. Area-Power solution set for a given condition
                3. Exit
1
Output file is created
                1. Av
1000
                2. Cl
1e-12
                3. Pt
1e5
                4. SR
2e6
Area,Power and design parameters' output files are created
```

Figure 2. Sample from Design Flow Code

As depicted in Figure 2, three options are available to the user. Selecting one of them, the user can find the design parameters of an analog block with respect to the given four specifications. In this example, the second option is chosen. Here, the output file can be area and power consumption values. Furthermore, the output files can be limited by giving a condition statement such as power consumption values being smaller than 30μW. After the design decisions, the software requests gain, output capacitance, 3dB cut-off frequency and slew rate specifications.

V. ANALOG BLOCKS

While building the analog blocks, current source load gain stage will be taken into account first. The analog block is simply a single common source amplifier loaded by a single transistor current source. Using simple performance parameter equations (12) and (13), the G_m and I_D value of the block is found. Then W's of the transistors are found from which the areas are obtained. The equations utilized are first-order approximations. However, the advantage of the methodology lies in the elimination of infeasible solutions during operation and very fast evaluation of design alternatives. In addition to this, second order effects are included automatically into G_m and r_{ds} while using EKV based modeling. Assume that f_{3dB} is taken as 100 kHz, gain is 20, load capacitance is taken as 1pf and IC's are fixed.

$IC_1 = 2.5$ $IC_2 = 3$	I_D	G_m	A_v
Estimation	0.9u [A]	12.5u [A/V]	20
Simulation	0.6u [A]	10u [A/V]	17

Table 1. Comparison between estimation and simulations results

The design solution predicts a current of 0.6μA for the amplifier transistor having an IC of 2.5 and the load transistor with IC of 3. Table 1 gives some idea about the design parameters of a current source load gain stage.

$$A_V \approx \frac{G_{m1}}{(G_{ds1} + G_{ds2})} = \frac{G_{m1}}{G_{out}} \quad (12)$$

$$F_t \approx \frac{G_{out}}{2\pi C_L} \quad (13)$$

The differential input stage is composed of a current mirror and a differential pair. The G_m of the differential input stage can be calculated using gain, bandwidth and load capacitance as in the current source load inverter.

Current source load and differential pair sub blocks have already been modeled. Now, these two stages will be combined to form a BTS OPAMP given in Figure 3. Av, f_{3dB}, SR, and C_L are the performance criteria of the BTS OPAMP that consists of a differential stage and an output stage

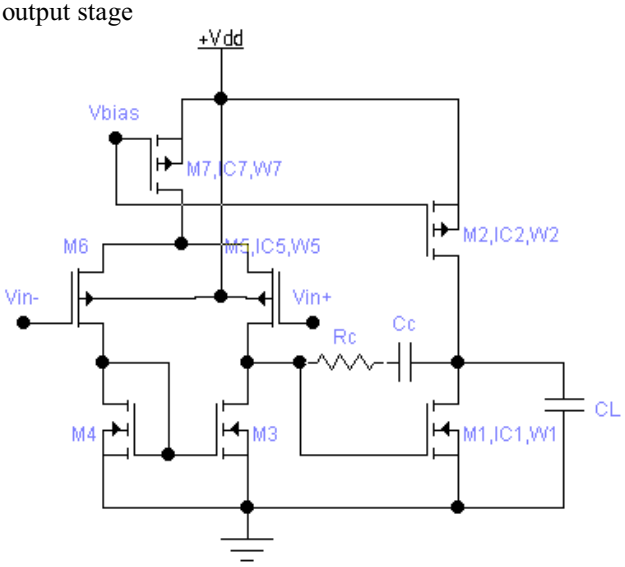

Figure 3. Lead Compensation BTS Opamp

The product of A_{V1} and A_{V2} which are the gain of the differential and output stages, respectively will give the overall gain. First of all, current of the output stage is fixed due to the slew rate given in (14). After that, using IC1, IC2 sweeping process and (9), Gm of the transistors can be found. In addition to this, W, V_P, V_{bias}, V_{gn} etc can be estimated using IC_1 and IC_2 values.

$$SR \approx \frac{I_D}{C_L} \approx \frac{I_{Dif}}{C_c} \quad (14)$$

In the differential part, one can easily find the value of IC_3 while V_{gn} value has already been calculated using (3) and (10). After that, we have to determine the Gm or current of the mosfets in the differential stage. Here, the important part of the design is to find out the compensation capacitance. Analog designers know that C_c must be smaller than the output capacitance and must be higher than the parasitic capacitances which appear on the drain of M3 and M5. Assume that the load capacitance C_L is taken as 1pf. Cc can be chosen around 0.2pf. Varying C_c can definitely affect to the opamp's stability. In our design, C_c varies between 0.2pf to 0.4pf. Due to the value of capacitance we can determine the Gm of the M5 as in (15).

$$GBW = F_t A_V = \frac{G_{m5}}{2\pi C_c} \quad (15)$$

Since we calculate the Gm, current of the differential part can be easily found using (9). Rest of the circuit can be designed as in the output stage. After modeling the BTS OPAMP, the accuracy must be verified. In order to achieve this end, the target parameters were chosen as A_V = 1000, f_{3dB} = 100 kHz, C_L = 1pf, SR = 2 V/µs. Estimation and simulation results can be observed in Tables 2 and 3.

The overall gain of the BTS OPAMP was distributed in several alternate ways to its two constituents and the resulting performances were analyzed. IC's were again fixed. In our design space, supply voltage is fixed to 3.3V so that it is easy to set the output voltage to any desired point. Our estimations give correct solutions with a tolerance on W of less than 10%.

$IC_1 = 2$ $IC_2 = 2$ $IC_5 = 2$	I_{Dout}	I_{Diff}	G_{out}
Estimation	2u [A]	9u [A]	0.65u [1/Ω]
Simulation	1.73u [A]	8.8u [A]	0.55u [1/Ω]
$A_{V1} = 20$ $A_{V2} = 50$	G_{mdiff}	G_{mout}	Power consumption
Estimation	125u [A/V]	27.6u [A/V]	66 u W
Simulation	126u [A/V]	25.3u [A/V]	64.3 u W

Table 2. Comparison between estimation and simulations results of BTS OPAMP

$IC_1 = 2$ $IC_2 = 2$ $IC_5 = 2$	W_1,W_2 u[m]	W_3,W_4 u[m]	W_5,W_6,W_7 u[m]
Estimation	1.6-6	9-9	27-27-61
Simulation	Vout = 1.9V		
Simulation	After changing W1 to 1.8 um Vout = 1.6 V		

Table 3. Estimation results of the width of the mosfets given in Figure 3.

In Table 3, it can also be observed that by modifying W_1 slightly, the desired V_{out} of 1.6 V can easily be attained. The effectiveness of the method can be demonstrated by graphical analysis. Assume that IC_1, IC_2, and IC_5 are swept from 1 to 2 by 0.1 steps. In addition to this, the differential gain stage A_{V1} varies from 20 to 50 with steps of 1. Each IC has 11 and A_{V1} has 31 different values. When one tries to form a look-up table for current and area solutions, 11x11x11x31 different values have to be calculated. In Figure 4, a solution set surface graph is illustrated for all values of IC and A_{V1}. There

are many area values for different IC and A_{VI} but they are not useful solutions for end users. Optimum solution for the end users can be selecting the minimum area values while satisfying the given specifications. In Figure 5, the same procedure was applied. However, minimum area was selected as an output parameter so that only one curve is obtained for the end users.

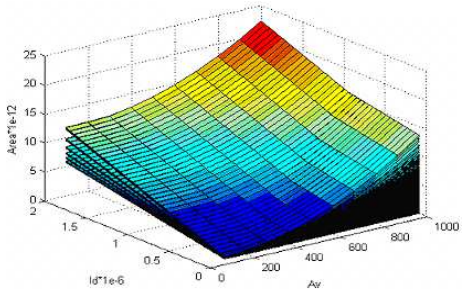

Figure 4. A_V-Area-I_D surface graph

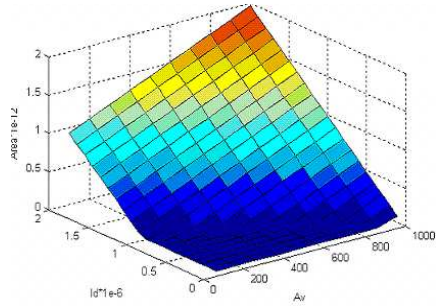

Figure 5. A_V-Area-I_D surface graph

Similar work was carried out for a cascade OPAMP. For this case, estimation and simulation results were compared and found to be close to each other.

VI. CONCLUSION

A design strategy is described and coded into C++ programming language. We implement each analog block such as BTS opamp, cascode opamp etc. into performance estimator tool. While calculating design parameters of the circuits, the analytical design equations of the EKV transistor model are used. Extensive verification of the estimator has been performed and the estimates have been shown to be reasonably accurate. Performance response graphs, which give ideas of circuit tradeoffs to the designers, were obtained.

The future work will proceed in several directions. One direction is the incorporation of more subblocks and more circuits into the estimator. The second direction is better incorporation of the estimator into the analog design automation flow described above.

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