# LEVEL RESTORATION FOR MULTI-VALUED LOGIC CIRCUITS

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## ABSTRACT

Compared to binary logic, the multi-valued logic circuits provide very small chip size, higher speed, and small number of interconnections and simpler realization of logic functions. However, the main drawback of these circuits is the lower noise margin. The noise margin decreases as the radix of multi-valued system increases. Due to the low noise margins, it is necessary to restore or recover the nominal levels of the signal after a certain number of cascaded stages. In this paper a new current mode CMOS restoration circuit is presented and evaluated.

## 1. INTRODUCTION

The multi-valued logic, MVL, is an alternative to common binary logic. The arithmetic operations can be performed more efficiently, and faster by increasing the radix of the system or the number of levels used, in the expense of reduced noise margin. The MVL system becomes equivalent to an analog system if the radix is very large. So, it suffers from the noise and parameter variations of the components used in the realization.

The current mode design can be successfully applied to higher-radix or multi-valued logic circuit design, abbreviated as CM-MVL. Despite some attempts in different technologies, [2]…[6], and a well-known switched-current CMOS design, [1], based on the current comparator scheme [7], full current-mode MVL structures are presented in [8][9].

In current-mode design, incorrect logic levels may be obtained due to the parameter variations of the components and the noise, if the number of cascaded stages exceeds a certain value. Because, the variations at each stage are added up. Therefore, it is unavoidable to restore the tabulated levels after a certain number of stages, unless the gates are self restored types [10]. In this paper a new full-current mode CMOS-MVL restoration circuit is presented. The relevant circuitry is extracted from an iterative-like algorithm, thus, leading regularity. Simulation results are given for fully extracted circuit realizations, using Mietec's 0.7μm HSPice level 6 parameters.

## 2. DEFINITIONS

In a radix-$r$ MVL system, any $m$-variable logic function, $f(X)$ may be represented in terms of basic operations. Here, $X=\{x_1, x_2,\ldots, x_m\}$ and each $x_i$ takes a value from the set $R=\{0,1,\ldots, r\text{-}1\}$. The radix, $r$, corresponds to the number of discrete values or number of possible signal levels. In current mode MVL logic, levels are represented by current levels in terms of a *base current*, $I_b$. The base current is set to 10μA for this study.

Thus, MVL variable $x$=0 is associated with the current level value, $l_0$, of null, $x$=1 is associated with $l_1=I_b$=10μA and so on. However, in the circuits, a logic current level, $l$, actually corresponds to an interval of the continuous quantity $y$, such that

$$y \rightarrow l: \quad \{y \mid (l-05)I_b \le y < (l+0.5)I_b\} \qquad (1)$$

This means that a total variation plus noise of ± ½$I_b$ may be tolerated.

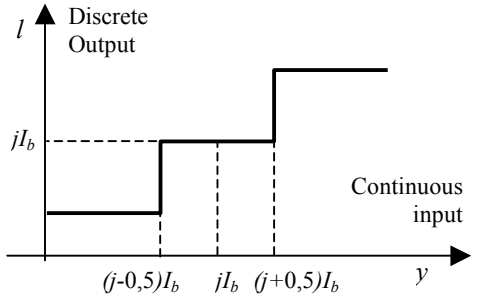



**Figure 1**. Conversion of continuous input signal to discrete MVL levels.

The definitions of basic MVL operations are given below[7][8][11]:

$$\min(x,y)=x\cap y=x\bullet y$$

$$\max(x,y)=x\cup y=x+y \qquad (2)$$

*Complement* of $x$:

$$\bar{x} = r-1-x \qquad (3)$$

*Truncated difference,*

$$x\Xi y = \begin{cases} x-y & \text{if } x \geq y \\ 0 & \text{otherwise} \end{cases} \qquad (4)$$

It can be shown that

$$\begin{aligned} \min(x,y) &= x\Xi(x\Xi y) = y\Xi(y\Xi x) \\ \max(x,y) &= \overline{\min(\bar{x},\bar{y})} = x+(y\Xi x) \end{aligned} \qquad (5)$$

The *literal*, (L),

$$L(k,{}^{a}x^{b}) = \begin{cases} k & \text{if } a \leq x \leq b \\ 0 & \text{otherwise} \end{cases} \qquad (6)$$

The clock-wise *Cyclic*

$$k\text{-}CWC: \; x^{\overset{k}{\rightarrow}} \equiv (x+k) \mod r \qquad (7)$$

The *upper* and *lower threshold* operations

$$upper-threshold,\ th_u: \; a|_b^c = \begin{cases} c & if\ a \geq b \\ 0 & otherwise \end{cases} \qquad (8)$$

$$lower-threshold,\ th_l: \; {}_b^c|a = \begin{cases} c & if\ a \leq b \\ 0 & otherwise \end{cases} \qquad (9)$$

## 3. IMPLEMENTATION

Although there are many techniques to realize MVL circuits [2]-[9], in this work, the current mode CMOS implementation is preferred due to the advantages mentioned before [8][9]. The building blocks of any MVL gate or function are mostly based on primitives, such as, current mirrors and truncated difference circuits shown in Figure-2. The secondary blocks such as *literal* and *threshold* circuit may be constructed by using the primitives or these circuits may be implemented by simpler special circuits as shown in Figure 3. *Min*, *max* gates and other more sophisticated circuits may be constructed by using primitives and secondary blocks.

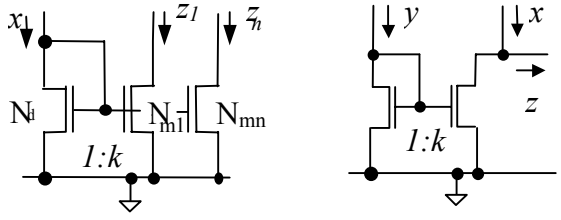
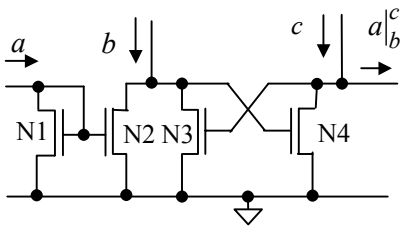



**Figure 2**. The building blocks of current mode CMOS MVL circuits. (a) Current mirror, (b) Truncated Difference circuit.




| Trans. | W/L |
|---|---|
| N1,2 | 1.75/1 |
| N3 | 4/1 |
| N4 | 1/4 |

**Figure 3**. The new feedback type Threshold circuit

Due to mismatch, parameter variation and other non-idealities the current levels at the output of gates may deviate from tabulated logic levels. Since a current mode CMOS MVL circuit may be treated as cascaded structure of similar gates the statistical analysis may be based on the typical circuit given in Figure 4. In [12], Ungan and Askar, showed that the current level variation can be minimized with $\alpha>>1$.

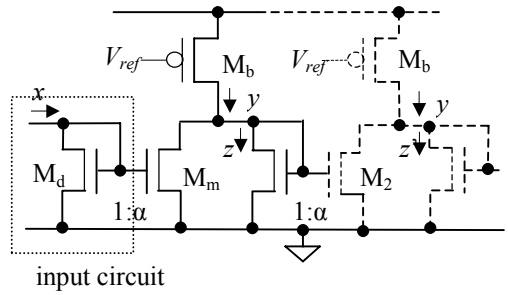



**Figure 4**. A typical interconnection stage.

## 4. LOGIC LEVEL RESTORATION

Basically, the level restoration sets the current levels to the pre-defined logic levels, i.e. it performs the operation given in Equation 1. In an *r*-valued logic, the conversion requires *r*-1 threshold detectors [7], and necessary binary decoding circuits. Despite some binary-logic associated level restoration schemes proposed in [1][7], the topologies assume lower radices, such as maximum 4. In [10], a *self-restoration* architecture is presented with similar limitations, despite some improvement. However, for higher radices, the restoration imposes extra cost, and conversion between current-mode and binary logic circuitries becomes very complicated. Thus, a low-cost design for this purpose is essential for current-mode MVL circuits.

A better noise performance description of current-mode MVL implementation can be assessed with the maximum count of identical structures that can be cascaded without loosing a predefined input logic level at the output.

Maximum radix of a given MVL function implementation depends on logic level degradations of *min* and *max* gates, $\Delta_{min}$, and $\Delta_{max}$, respectively. Adjusting that $\Delta_{min} \approx \Delta_{max}$, allowable logic level degradation or a standard deviation for each *m*-input gate can be determined by

$$\sigma_{\min,\max} \le \frac{(I_b/2)}{\sqrt{\left\lceil \log_2(m-1) + m\log_2 r \right\rceil}} \qquad (10)$$

For example, if $m$=2, $r$=8, and $I_b$=10μA, then $\sigma_{min,max}$ ≤2.25μA. However, in most cases, an MVL function may not contain all variables available. For example, if a function can be minimized into two max terms with two-variable product terms, then $\sigma_{min,max}$ ≈1.5μA. For *min* and *max* gates described in [9] Monte Carlo analysis have been carried out with 100 iterations using parameters $\sigma_{\Delta\beta/\beta}$=%5 and $\sigma_{VTO}$=50mV where β is the device transconductance and VTO is the threshold voltage. Table 3.3 summarizes analysis results measured at $I=I_{max}$ , for different process dimensions.

A *gate count*, GC, for a given gate description, is defined as the maximum allowable number of cascaded identical gates. It can be determined by

$$GC \le \left(\frac{I_b/2}{\Delta_{\min,\max}}\right)^2 \approx \left(\frac{I_b}{2\sigma_{\min,\max}}\right)^2 \qquad (11)$$

In order to validate Equation 10, HSPice DC simulations are carried-out. The results are given in Fig. 5 for a *Max* gate described in [9].

**Table 3.3**. Monte-Carlo analysis results of design

| Process $(W/L)_n$,; $(W/L)_p$ | $\%\sigma_{\Delta z/z}$ $z$=min($x$,$y$) | $\%\sigma_{\Delta z/z}$ $z$=max($x$,$y$) |
|---|---|---|
| 1.75/1; 5.5/1 | 3.1 | 4.3 |
| 2.25/1.5; 8/1.5 | 2.5 | 2.7 |

In this paper we propose a novel generalized restoration algorithm for current-mode MVL designs. The algorithm eliminates conversions used by other circuits and restored level is obtained directly. Consider a variable $x \in R$ and $x_i \in R_i = \{0,1,2,..,r/2^i-1\}$ with $r$ even and $i$ from 1 to $\log_2 r$-1.

The following quantities are used to obtain the intermediate restored levels:

$$\begin{aligned} x_0 &= x \\ &\cdot \\ &\cdot \\ x_i &= x_{i-1} \pmod{r/2^i} \end{aligned} \qquad (12)$$

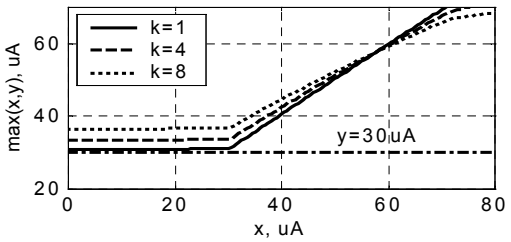



**Figure 5.** Monte-Carlo DC simulation results of cascaded of *Max* gates with W/L=1.75/1 feature size. Parameter k indicates the number of cascaded gates. k=1 corresponds to single stage (near ideal characteristic).

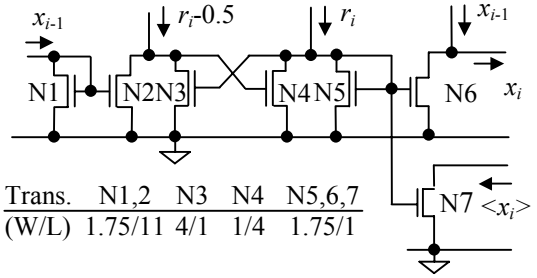



**Figure 6**. Current restoration circuit for single level, based on threshold circuit.

It is obvious that the restored value of $x_i$ , <$x_i$>, can be generated from $x_i$ by using the cyclic operator with $k$=0, and radix $r_i=r/2^i$. Each iterative stage can be realized by using the modified threshold circuit shown in Fig. 6 where <$x_i$> is the restored output of the corresponding stage.

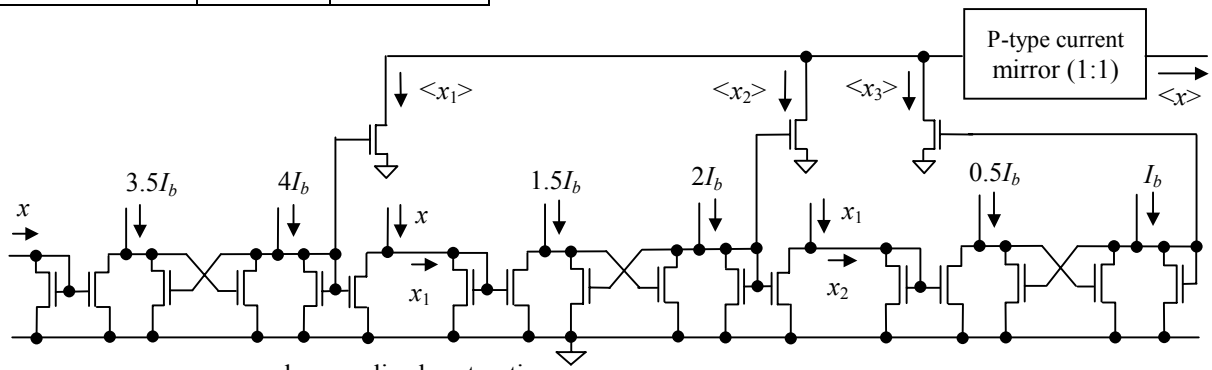



**Figure 7.** Detailed schematics of 8-level restorer circuit.

The total restored level current can be established by cascading stages for $i$=1 through [$\log_2 r$-1], and summing up individual restored level currents, as:

$$< x >= \sum_{i=1}^{log_2 r - 1} < x_i > \qquad (13)$$

The algorithm for $r$=8 is realized with 38 transistors, Fig. 7, while 48 transistors are required for for a direct binary decoding scheme with the same radix. HSPice simulation results shown in Fig. 8, indicate better transient response compared to previous schemes. The delay and power dissipation are 2.75ns 0.25mW respectively. Since similer circuits may be cascaded, there is no limitation for the radice. So this new circuit is very suitable for higher radix applications and it is more technology independent.

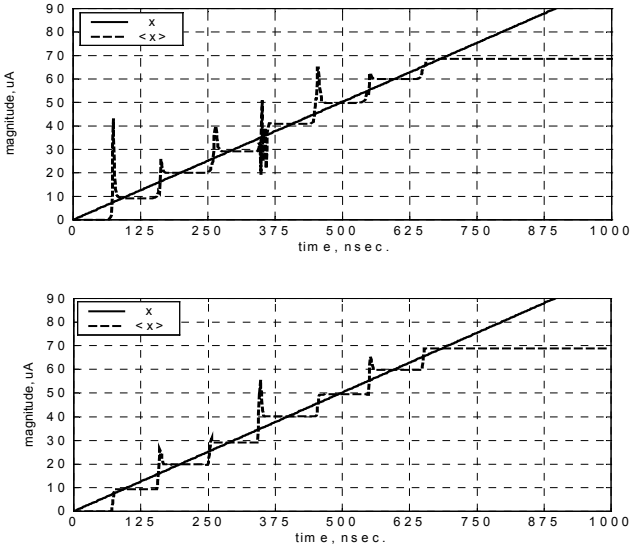



**Figure 8.** Transient simulation results of two restoration circuits. (a) Switched current type. (b) Full current-mode level restorer of Fig.7.

## 5. SUMMARY

Although the circuit complexity may be drastically simplified by using multi-valued logic, MVL, instead of binary logic, MVL suffers from low noise margin and static power dissipation. Static power dissipation may be unimportant for continuously running high speed circuits, but it is necessary to use level restoration circuits in multi valued logic circuits, to overcome the signal degradation and wrong logic level generation problems.

In this paper the level degradation problem is explained and a new, full current mode CMOS level restoration circuit, based on feedback type threshold circuit is presented. This circuit is very suitable for high radix MVL realizations. It is simpler than previously proposed counterparts. Simulation results show that the new circuit exhibits better transient behavior while the power consumption and delay are similar to previous designs.

## 6. REFERENCES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