Time Delay Calculation in Current-Mode Circuits

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Abstract

In this paper time delay calculations for a current-mode circuit are considered and an equivalent circuit model for delay estimation is developed. The relation obtained for the time delay can be adapted to any CMOS current-mode circuit. The proposed calculation method is verified with SPICE using 0.35 µm TSMC MOSIS technology parameters.

1. Introduction

Nowadays, modern integration technologies are in a serious development stage, because of the requirements of higher speed, lower power consumption and lower power supply values. Due to the reduction in the dimensions of integration devices, maximum voltage ratings are reduced as well. The reduction in supply voltage values does not limit the design of digital circuits; but the design of high performance analog integrated circuits with low supply voltages becomes more complicated.

Current-mode circuit design can be considered as a solution to design high-performance analog circuits with lower supply voltages. A literature survey shows that current-mode circuits have many advantages in comparison with voltage-mode circuits in terms of speed, bandwidth, accuracy, etc. In current-mode circuits, high voltage gain amplifiers, passive components with high sensitivity, summers are not required and that is why these circuits can be designed completely with transistors. This advantage provides the compatibility of current-mode circuits with digital processes as well [1]-[2].

Generally, in the literature, dynamic characteristics of CMOS inverter circuits are investigated. Calculations of CMOS inverter delay were presented primarily by Burns in 1964 [3].

One of the first studies on the time delay calculations is about series connected MOSFET structures (SCMS's) [4]. The delay calculation of the CMOS inverter using new short channel MOS transistors has been investigated in [5].

In recent years, some studies on the delay performance of the current-mode circuits have been performed. In 2004, a current-mode delay-line with all-pass filters is presented which can be used as a compensation method in Laguerre adaptive filters. The proposed method enables the use of minimum length for the transistors which enlarge the bandwidth without considerably increasing the power consumption [6].

In another work, time delay model of Pulse Width Modulation (PWM) in current-mode control is presented in [7]. The stability, dynamic behavior, and the time delay in the modulation process are also investigated in [7].

In [8] the analytic step response of an NMOS current mirror has been examined. The settling time of the current mirror has been derived analytically. However, the output resistances of the transistors were not taken into account.

The aim of this paper is to give a general calculation of time delay in current-mode circuits. There are two phases in the calculation of the time delay. Firstly, an equivalent circuit model has to be created. Secondly, analyzing the obtained equivalent circuit model, time delay formula is extracted in terms of circuit element's parameters. Then simulations have to be performed to confirm the theoretical analysis. To further investigate the delay issue in current-mode circuits, a CMOS Core Circuit reported in [9] has been simulated and time delay results given.

The sequel of the paper is organized as follows: in Section 2, a simple current-mode current mirror circuit and its large-signal equivalent circuit model are given. In Section 3, the time delay formulation of the equivalent circuit model is extracted. In addition the effects of the parasitic capacitances on the delay calculations are considered. SPICE simulations are presented in Section 4. Finally, some concluding remarks are given in Section 5.

2. Equivalent Circuit Model

As a simple current-mode circuit PMOS basic current mirror is selected for time delay investigation.

In Fig. 1a, a PMOS current-mirror which is widely used in complex current-mode circuits is shown. Both of the transistors are assumed to operate in saturation region. The large-signal equivalent circuit model of the PMOS transistor M_1 is shown in Fig. 1b; it consists of a capacitor in parallel with a non-linear resistor. The capacitor C in Fig. 1b represents the total parasitic capacitances of MOS transistors (including the loading capacitors of M_2.) The non-linear resistor stems from the dependent current source of the MOS transistor model working in saturation region. r_o is the output resistance which will be taken into account in Section 3.

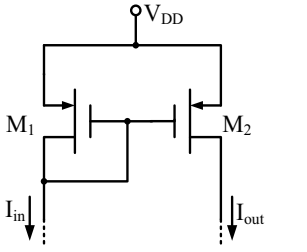

Fig. 1a. PMOS circuit model.

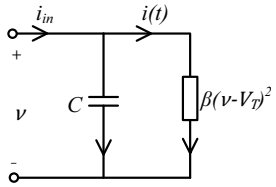

Fig. 1b. Large-signal Equivalent circuit model without r_o.

According to Kirchhoff's current law the following equation can be written for the circuit of Fig. 1b.

$$C\frac{dv(t)}{dt} = -\beta\,(v(t)-V_T)^2 + i_{in}(t) \qquad (1)$$

where $\beta = 1/2\mu_p C_{ox}\ W/L$ is the gain factor of MOS transistors, the parameters μ_p, C_{ox}, W, L have their usual meanings and V_T is the threshold voltage.

3. Time Delay Calculations

The Input-Output (I-O) waveforms of the current-mirror circuit are shown in Fig. 2. As can be seen from Fig. 2, low to high time delay τ_{PLH} of MOS transistors can be defined as time duration between the initial time t_0 (the output current is at its minimum value) and the time t_1 (the output current increases to half of its maximum value). Similarly high to low transition propagation delay τ_{PHL} is the time duration required for the output to decrease to half of its maximum value from its maximum value. Thus, the propagation delay times τ_{PHL} and τ_{PLH} are found from Fig. 2 as:

$$\tau_{PLH} = t_1 - t_0 \tag{2}$$

$$\tau_{PHL} = t_3 - t_2 \tag{3}$$

The average propagation delay (τ_P) is defined as the average of the two delays in (2) and (3):

$$\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2} \tag{4}$$

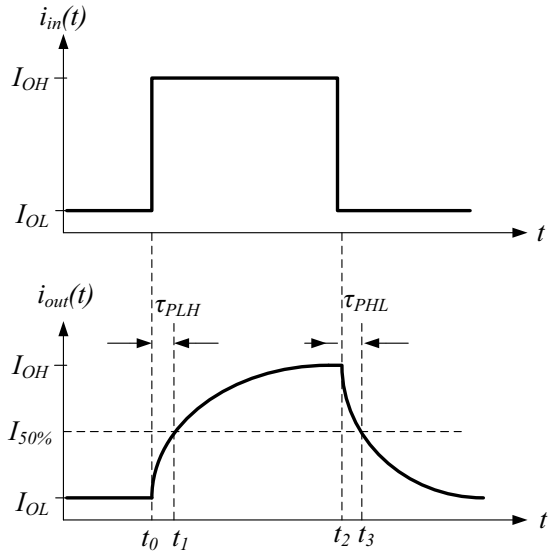

Fig. 2. I-O current waveforms

The next step is to calculate the time delay τ_{PLH} from the equivalent circuit model. To do this, the value of the current $i(t)$ at time t_1 must be equated to half of the value of the input current (I_{OH}). To find the time t_1 Eq. (1) must be used; that is at t_1 Eq. (5) must be satisfied.

$$i(t_1) = \frac{I_{OH}}{2} \Leftrightarrow C\frac{dv(t_1)}{dt} = \frac{I_{OH}}{2} \tag{5}$$

By substituting Eq. (5) into Eq. (1), the following set of equations can be reached.

$$C\frac{dv(t_1)}{dt} = -\beta\,(v(t_1)-V_T)^2 + I_{OH} = \frac{I_{OH}}{2} \tag{6}$$

$$\beta(v(t_1) - V_T)^2 = \frac{I_{OH}}{2} \tag{7}$$

$$v(t_1) - V_T = \mp\sqrt{\frac{I_{OH}}{2\beta}} \tag{8}$$

$$v(t_1) = V_T \mp \sqrt{\frac{I_{OH}}{2\beta}} \tag{9}$$

Eq. (9) shows the input node voltage at time t_1. Taking $t_0 = 0$ and solving Eq. (1) with initial value of $v(0) = V_T$, one can find the following expression for the $v(t)$:

$$v(t) = V_T + \frac{\sqrt{I_{OH}}\tanh\left[\frac{\sqrt{I_{OH}}\sqrt{\beta}}{C}t\right]}{\sqrt{\beta}} \tag{10}$$

From Eq. (10), t can be found as:

$$t = \frac{arctanh\left[\frac{v(t) - V_T}{\sqrt{I_{OH}/\beta}}\right]}{\frac{\sqrt{I_{OH}}\sqrt{\beta}}{C}} \tag{11}$$

Substituting $v(t_1)$ from (9) into (11) for $v(t)$, the time delay is obtained as:

$$t_1 = 0.8814 \times \frac{C}{\sqrt{I_{OH}\times\beta}} = \boldsymbol{\tau_{PLH}} \tag{12}$$

Thus, with Eq. (12) a very simple time delay formulation is achieved for the current mirror. In fact, the propagation delay $\tau_{PLH} = t_1$ depends on the value of the total parasitic capacitances (C), the input current initial value I_{OH} and the parameter β. Thus by minimizing the total value of the parasitic capacitances the propagation delay can be reduced.

To see the effect of the output resistance of the transistors on time delay, similar analyses can be performed. The equivalent circuit model with transistor output resistance is shown in Fig. 3.

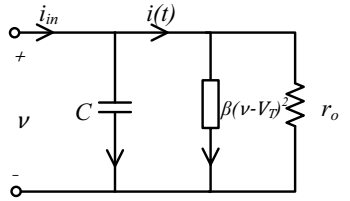

Fig. 3. Large-signal equivalent circuit model with r_o

Adding the output resistance and writing the KCL at the input node, the Eq. (1) is modified as:

$$C\frac{dv(t)}{dt} = -\beta(v(t)-V_T)^2 + I_{OH} - \frac{v(t)}{r_o} \quad (13)$$

Solving the above differential equation for the time value t_1 at which $i(t_1) = \frac{I_{OH}}{2}$ results in:

$$t_1 = \frac{\left(ArcTan\left[\frac{-v(t_1)2r_o\beta - 1 + 2r_oV_T\beta}{\sqrt{-1+4r_o(-I_{OH}r_o+V_T)\beta}}\right] - ArcTan\left[\frac{-1+2r_oV_T\beta - 2r_o\beta V_T}{\sqrt{-1+4r_o(-I_{OH}r_o+V_T)\beta}}\right]\right) * 2Cr_o}{\sqrt{-1+4r_o(-I_{OH}r_o+V_T)\beta}} \quad (15)$$

where

$$v(t_1) = \frac{-1+2r_oV_T\beta \mp \sqrt{1+2r_o(I_{OH}r_o-2V_T)\beta}}{2r_o\beta} \quad (16)$$

As mentioned before, the total parasitic capacitance has the main effect on the value of the time delay. So a precise calculation of these capacitances is an important issue for current-mode circuits. As an example for calculation of the total parasitic capacitances at the input node of the circuit, the CMOS Core Circuit which was developed as a classifier integrated circuit and manufactured as DU-TCC1209 in 2009 [9], has been used. The CMOS implementation of the classifier core circuit is shown in Fig. 4. To calculate the total parasitic capacitances, the input section of the classifier core circuit with parasitic capacitances of each transistor is shown in Fig. 5.

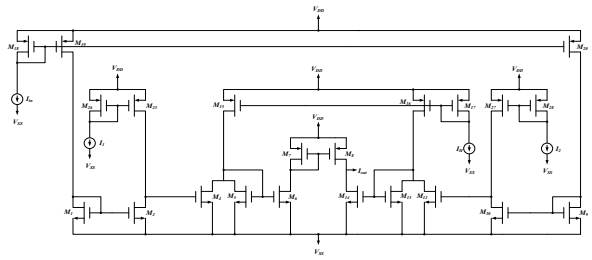

Fig. 4. CMOS Implementation of the Core Circuit [9]

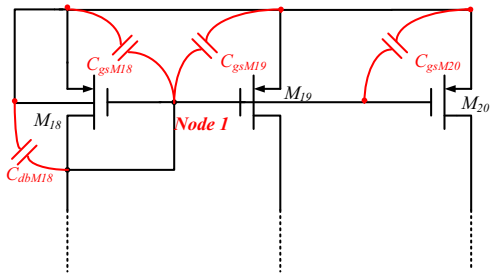

Fig. 5. Input section of the core cell with parasitic capacitances

The parasitic capacitances C_{dbM18}, C_{gsM18}, C_{gsM19}, C_{gsM20} affecting Node 1 are all connected in parallel to each other hence the equivalent overall input capacitance is calculated approximately as shown in Eq. (17).

$$C_{eq} = C_{dbM18} + C_{gsM18} + C_{gsM19} + C_{gsM20} + 7C_{ov} \quad (17)$$

The formula of the gate to source capacitance C_{gs} is given by:

$$C_{gs} = \frac{2}{3} \times C_{ox} \times W \times L \quad (18)$$

where C_{ox} is the capacitance per unit area of the gate dielectric, W and L are width and length of the transistor respectively. The drain-bulk junction capacitance (C_{db}) is found from the following equality [10]:

$$C_{db} = \left(\frac{CJ}{\left(1+\frac{VDB}{PB}\right)^{MJ}} \times AD\right) + \left(\frac{CJSW}{\left(1+\frac{VDB}{PB}\right)^{MJSW}} \times PD\right) \quad (19)$$

where CJ is is the zero-bias body-junction capacitance per unit area over the drain/source region and $CJSW$ is the zero-bias body-junction capacitance per unit length along the sidewall (periphery) of the drain/source region. MJ is the grading coefficient, for area component and $MJSW$ is the grading coefficient, for sidewall component; PB is the body-junction built in potential, AD is the area while PD is the perimeter of the drain region of MOSFET [10].

In addition C_{ov} in Eq. (17) is the overlap capacitance of each transistor effecting Node 1. The overlap capacitance, which appears due to the fact that source and drain diffusions extend under the gate oxide, is computed as:

$$C_{ov} = W \times L_{ov} \times C_{ox} \quad (20)$$

where L_{ov} is overlap length. The value C_{ov} must be added to the C_{gs} and C_{gd} for each transistor. With a routine analysis and applying Miller effect it can be seen that a total number of $7C_{ov}$ appears in Eq. (17).

The parasitic capacitances of the transistors shown in Fig. 5 for the CMOS technology ($0.35\mu m$) are given as follows: $C_{gsM18} = C_{gsM19} = C_{gsM20} = 64.22\ fF$, $C_{dbM18} = 14.11\ fF$, $C_{ov} = 9.6\ fF$. So the equivalent capacitance is $C_{eq} = 274.223\ fF$. In addition, $\beta = \frac{1}{2}\ \mu C_{ox}$, $W/L = 737.389\ (\mu A/V^2)$, $I_{OH} = 50\mu A$ and $V_T = 0.714\ V$. Using these specified values in Eq. (12) the time delay is found to be $\boldsymbol{\tau_{PLH}} = 1.26\ ns$.

Taking into account the output resistance of the MOS transistors ($r_o = 100\ k\Omega$) and using Eqs. (15) and (16) the time delay value is found to be $\tau_{PLH} = 1.4\ ns$ which shows an increase of 10% in the time delay when r_o is considered.

4. Simulation Results

The core circuit in Fig. 4 has been simulated with $0.35\mu m$ TSMC CMOS technology parameters using SPICE simulation software. The supply voltages V_{DD} and V_{SS} were selected as $\pm 1.65V$. The transistors' dimensions are given in Table 1.

Table 1. Dimensions of the CMOS Transistors in Core Circuit

MOSFET	W[μm]	L[μm]
M_1, M_2, M_9, M_{10}	42	1.05
M_7, M_8, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}, M_{25}, M_{26}, M_{27}, M_{28}	21	1.05
M_4, M_5, M_6, M_{12}, M_{13}, M_{14}, M_{21}, M_{22}	10.5	1.05

Simulated input waveform and output waveform obtained from the drain of transistor M_{19} of the CMOS core circuit is shown in Fig. 6. The resulting time delay $\boldsymbol{\tau_{PLH}}$ is equal to 1.5

ns. From calculations, time delay without r_o effect is *1.26 ns*, and with r_o *1.4 ns*, which are very close to the value obtained from the simulation; thus the simulation results verify well the proposed circuit model and the calculations.

5. Conclusions

In this paper, the calculation of time delay in current-mode circuits has been investigated and analytical expressions are obtained for calculating the time delay in MOS current mirrors. Accuracy of the expressions has been confirmed with SPICE simulations on the CMOS Core Circuit in DU-TCC1209 IC [9].

One of the main uses of time delay calculations is concerned with the operation speed of the circuit under consideration. Building ring oscillators, pulse width modulators, level crossing detectors using the Core Circuit in DU-TCC1209 IC has been presented as an application in [12]. As a future work under consideration, the delay calculations introduced here will constitute a basis for the computation of the operation frequency of such applications.

6. References

[1] G. Ferri, N.C. Guerrini, "Low-Voltage Low-Power CMOS Current Conveyors", Kluwer Academic Publishers, Boston, London, 2003.

[2] C. Toumazou, F.J. Lidgey, D.G. Haigh, "Analogue IC Design: the Current-Mode Approach", IEE Circuits and Systems Series 2, London, United Kingdom, 1990.

[3] J.R. Burns, "Switching response of complementary-symmetry MOS transistor logic circuits," RCA Rev., vol. 25, pp. 627-661, Dec. 1964.

[4] T. Sakurai, A. R. Newton, "Delay Analysis of Series-Connected MOSFET Circuits", IEEE Journal of Solid-State Circuits, vol. 26, no.2, pp. 122-131, February 1991.

[5] T. Sakurai, A. R. Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas.", IEEE Journal of Solid-State Circuits, vol. 25, no.2, pp. 584-594, April 1990.

[6] C.M. Montero, A.D Sanchez, "A Current-Mode Delay-Line with Continuous-Time Offset Compensation", 1st International Conference on Electrical and Electronics Engineering (ICEEE), pp. 614-617, Sept. 2004.

[7] Z. Xu, W. Xu, Y. Yu, Q. Wu, "A Study on the Stability of Current-Mode Control Using Time delay Model of Pulse-Width-Modulator." 7th International Conference on System Simulation and Scientific Computing, pp. 1432-1435, Oct. 2008.

[8] D. G. Narin "Analytic step response of MOS current mirrors", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, vol. 40, no. 2, pp. 133-135, 1993.

[9] M. Yıldız, S. Minaei, C. Göknar, "A flexible current-mode classifier circuit and its applications", International Journal of Circuit Theory and Applications, vol. 39, no.9, pp. 933-945, April 2010.

[10] A.S. Sedra, K.C. Smith, "Microelectronic Circuits", Fifth Edition, Oxford University Press, New York, 2004.

[11] http://www.cs.uoi.gr/~tsiatouhas/DigElecIntro/CD4007.lib

[12] İ.C. Göknar, S. Minaei, M. Yildiz and E. Akçakaya "Pulse Width Modulation Using a Recently Developed CMOS Core Circuit," accepted for presentation at the European Conference on Circuit Theory and Design (ECCTD 2013) Dresden, Germany, Sept. 2013.

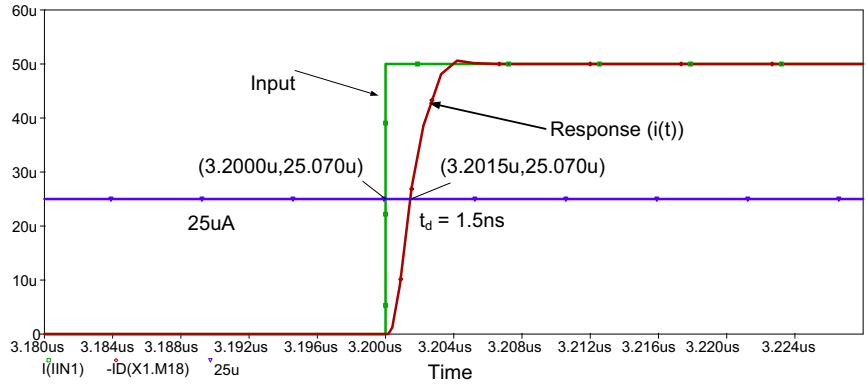

Fig. 6. Step response for the input stage of the core circuit of Fig. 5.