1–8 GHz High Efficiency Single Stage Travelling Wave Power Amplifier

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Abstract

In this paper a Class-A/AB operated wideband power amplifier is presented that comprises of only a single transistor travelling wave stage where capacitive coupling and frequency dependent lossy artificial transmission-line are employed at the input of the active device. These technique are shown to significantly enhance the amplifier frequency-bandwidth product, input match and gain flatness performance over 1-to-8 GHz operating bandwidth. Furthermore, a non-terminated output artificial transmission line inductance is determined using load-pull data to achieve an optimum power-bandwidth performance. Overall 1.31×2.93mm^2 power amplifier design is fabricated by using 0.25µm GaAs PHEMT MMIC process and the amplifier delivers 1W and 0.5W peak P_{sat} and $P_{out,1dB}$ levels respectively where the PAE levels are over 50% and 27% for P_{sat}, and $P_{out,1dB}$ almost the entire 2-to-8 GHz frequency band.

1. Introduction

The basic idea underpinning the travelling wave amplifiers (TWA) is the use of inherent parasitic capacitances at the transistor's input and output terminals together with external inductive elements to form artificial transmission-lines [1-4]. The cut-off frequency of the amplifier circuit is therefore determined by the cut-off frequency of the artificial-lines. The resulting amplifier structure readily provides broadband performance, usually above one decade. There are basically two classes of TWA structures in the literature: Conventional TWA (CTWA) [1, 2] and Cascaded Single-Stage TWA (CSSTWA) [3-5]. In a single transistor case both classes reduce to the same structure and the power amplifier could be denoted as Single-stage travelling wave power amplifier (SSTWPA) [6].

The SSTWPA has some disadvantageous namely poor broadband gain flatness and matching. However, these drawbacks can be eradicated by properly designing the amplifier circuit using techniques such as capacitive coupling [2] and frequency dependent lossy artificial-line [5].

In this paper, the proposed SSTWPA structure employs both technique of capacitive coupling and frequency dependent lossy artificial transmission-line at the FET input terminal. The FET output artificial transmission-line inductive element is determined by using load-pull data of the transistor and the termination impedance is removed to improve output power performance.

The design procedure presented here provides wideband operation using a single device with the high efficiency performance. SSTWPA circuit is designed and fabricated by using 0.25µm GaAs PHEMT process from United Monolithic Semiconductor.

2. Analysis of SSTWPA

A general and simplified topology of the SSTWPA circuit is depicted in Fig. 1 [6]. The input signal propagates along the input artificial transmission-line and stimulates the active device gate terminal. Z_T is the termination impedance of the input-line. The amplified signal at the output goes through the output line formed by the output capacitance of the FET device and the series inductance L_o.

The simplified small-signal equivalent circuit model representing the transistor shown in Fig. 2 is preferred for basic ac-analysis of TWA [7]. This model includes input (C_{in}) and output (C_{out}) parasitic capacitances, input serial resistance (r_{in}) and output parallel resistance (r_{out}). The capacitances form artificial transmission-lines with the external inductive components.

The magnitudes of the device resistive elements have the most effect on the performance of the input artificial-line. This simple model however cannot predict the device behavior completely but by investigating variations of the parameters in the model versus frequency, it is possible to predict the gain-frequency performance.

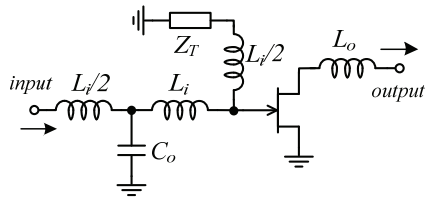


Fig. 1. Simplified schematic of the SSTWPA.

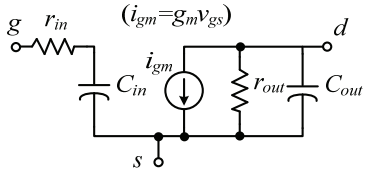


Fig. 2. Simplified active device model.

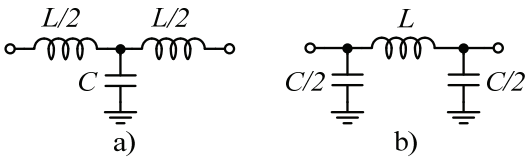


Fig. 3. Artificial transmission-line sections:
(a) T- type (b) π-type sections

Two types of artificial transmission-line sections can be defined as T-type and π-type shown in Fig. 3. Typically artificial-lines in a TWA are designed using T-type sections. However, for the circuit analysis purpose, the π-type approach at the input and output of the transistor is necessary due to the capacitive behavior of the input and output ports of the active device.

Artificial transmission-lines in a TWA behave like low-pass filter characteristics which have characteristic impedance and for the lossless case the cut-off frequency given by

$$Z_o = \sqrt{L/C} \tag{1}$$

$$f_C \cong 1/\pi\sqrt{LC} \tag{2}$$

As will be shown later the frequency dependent lossy artificial transmission-line section at the input can improve gain-frequency performance of the SSTWPA. In Fig. 4, an SSTWPA input line is shown to employ one lossy T-section comprising of a resistor (R_i). This lossy section has not only an effect of improving the input matching and gain flatness but also it helps to ensure stability of the amplifier. Furthermore, the SSTWPA in Fig. 4 also employs a capacitance (C_c) in serial to the transistor input to increase the frequency-bandwidth [2]. This technique of capacitive coupling however reduces the amplifier gain as a drawback.

The other important design step for the SSTWPA is the load-pull characterization in order to determine an appropriate output-line inductance. Limiting the magnitude of the inductance at the output of a SSTWPA is also important since the high frequency loss increases when the inductance value is high and therefore it can affect the amplifier's overall output power performance.

Moreover, a single inductance simplifies the amplifier's construction. As will be shown later this artificial transmission-line technique is advantageous for broadband applications. Hence, it can be deduced that the circuit given in Fig. 4 is a convenient structure for broadband power applications.

In Fig. 4, values of capacitance and resistance of the lossy section simply could be given by

$$C_i \cong \frac{C_{in}C_c}{C_{in}+C_c} \tag{3a}$$

$$R_i \cong r_{in} \tag{3b}$$

The value of the inductance at the input line is calculated to provide characteristic impedance of Z_o, equal to

$$L_i = Z_o^2 C_i \tag{4}$$

As mentioned above, the output inductance value is determined by load-pull analysis and the output line characteristic impedance (Z_{opt}) is obtained by using

$$Z_{opt} = \sqrt{L_o/C_{out}} \tag{5}$$

If Z_{opt} is not equal to 50Ω then by using an impedance matching network or a transformer at the output may help to enhance the amplifier power performance. The small-signal gain of the modified SSTWPA could be given by

$$|A_o| \cong \left(\frac{C_c}{C_{in}+C_c}\right) g_m Z_{opt} \tag{6}$$

The expressions given above were used in the first step of designing the SSTWPA. It should be noted that the obtained circuit may not provide the optimum performance because of the unaccounted inherent parasitic effects. In this case it is necessary to instigate optimization steps in order to improve the gain flatness performance of the SSTWPA in the desired frequency band of operation.

3. Design of the SSTWPA Circuit

The SSTWPA circuit is designed according to the previous discussion. The design aim is to maximize power performance over the widest possible frequency band of the amplifier.

The first step of the design process involves determining suitable transistor dimensions and choosing the bias point. Thus, a single transistor having maximum channel width of 125μm and 12 fingers geometry is selected. For this device I_D=140mA and V_{DS}=8V were found to be the optimum bias where the device are operating in class-A/AB.

In the second step, the chosen transistor is investigated for its suitability for the SSTWPA application. That is to say, input and output parasitic capacitances, input resistance, output resistance and gain variations as a function of frequency are studied. It is observed that for a given 50Ω characteristic impedance, the bandwidth performance of the chosen transistor is limited to 2GHz due to its relatively high 3pF input capacitance. To increase the bandwidth performance, the capacitive coupling technique is employed by sacrificing the overall gain level. In this way the equivalent input capacitance of the transistor reduced to around 1pF where C_c=2.1pF is taken as an optimized value. Furthermore, the input line is designed for Z_o≈40Ω where it is sufficient for a good match to 50Ω.

Although these modifications resulted by sacrificing the amplifier gain performance, it enabled the realization of a much wider bandwidth within the operation band of 1-to-8GHz.

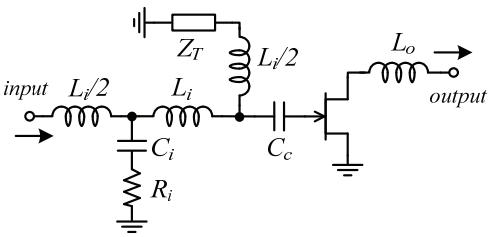


Fig. 4. Modified SSTWPA to improve power performance.

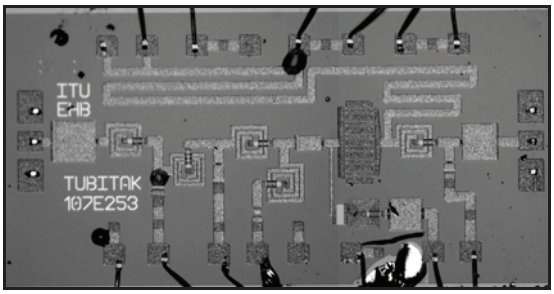


Fig. 5. Chip photograph of the fabricated SSTWPA.

The output capacitance of the transistor is approximately equal to 0.5pF. For a maximum voltage swing, optimum-load impedance is obtained to be approximately 34Ω according to the load-pull simulations. As a result, by using the Eq. 5, optimum inductance L_o could be determined as 0.57nH. Input line is constructed with using two T-sections, one of which is lossy. Finally, for the biasing purposes at the drain, an on chip inductive transmission-line is constructed to form a wideband RF choke. The fabricated chip photograph of the SSTWPA is shown in Fig. 5 where the die chip dimensions are $1.31\times2.93mm^2$.

4. Results

The small signal s-parameter performance of the SSTWPA is shown in Fig. 7 including both simulations and measurements. The chip is bond-wired to an external PCB board for DC supplying purpose. RF signals are left inside the chip and G-S-G type probes and probe station are used for the input and output signal measurements.

The amplifier exhibits an average gain of 10dB across the bandwidth from 1-to-8GHz. The gain can be increased by removing the capacitive coupling, but in doing this would compromise the amplifier bandwidth as mentioned before. Input match (S_{11}) of the SSTWPA is below -10dB and the output matching (S_{22}) is measured to be -5dB and below for the worst case.

The low frequency mismatch between the simulation and the measurement of the S_{22} is due to degraded performance of the on chip drain biasing inductance. It is however possible to improve S_{22} performance by using a suitable external off chip inductance. Fig. 8 shows the group delay performance where the results match quite well with the simulations. For the stability concern, Fig. 6 gives the stability factor (K) and stability measure (B) parameters for simulations. The necessary and sufficient conditions for unconditional stability are that the stability factor is greater than unity and the stability measure is positive. As can be seen from the figure that both K>1 and B>0 are derived inside the band. Also there is not any oscillation condition observed at the output when stimulating input signal when measuring the chip. Therefore, SSTWPA presented a stable operation within the operation band.

Saturated output power (P_{Sat}) and output referred 1dB compression point power ($P_{out,1dB}$) levels are measured and the related power added efficiency (PAE) performances are also calculated using the power measurements in the band of 2-to-8GHz. Results are plotted in Fig. 9. P_{Sat} and $P_{out,1dB}$ power levels have their peak values at 1W (30dBm) and 0.5W (27dBm) and PAE levels are above 50% and 27% respectively inside the band.

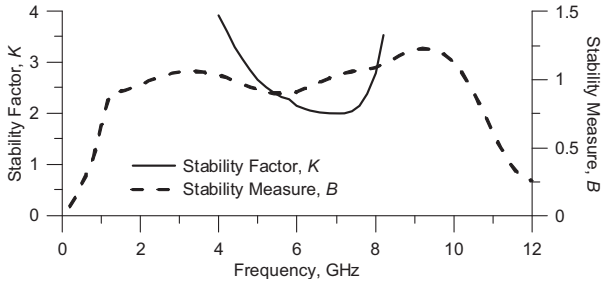


Fig. 6. Stability performance of the SSTWPA (K>1 and B>0).

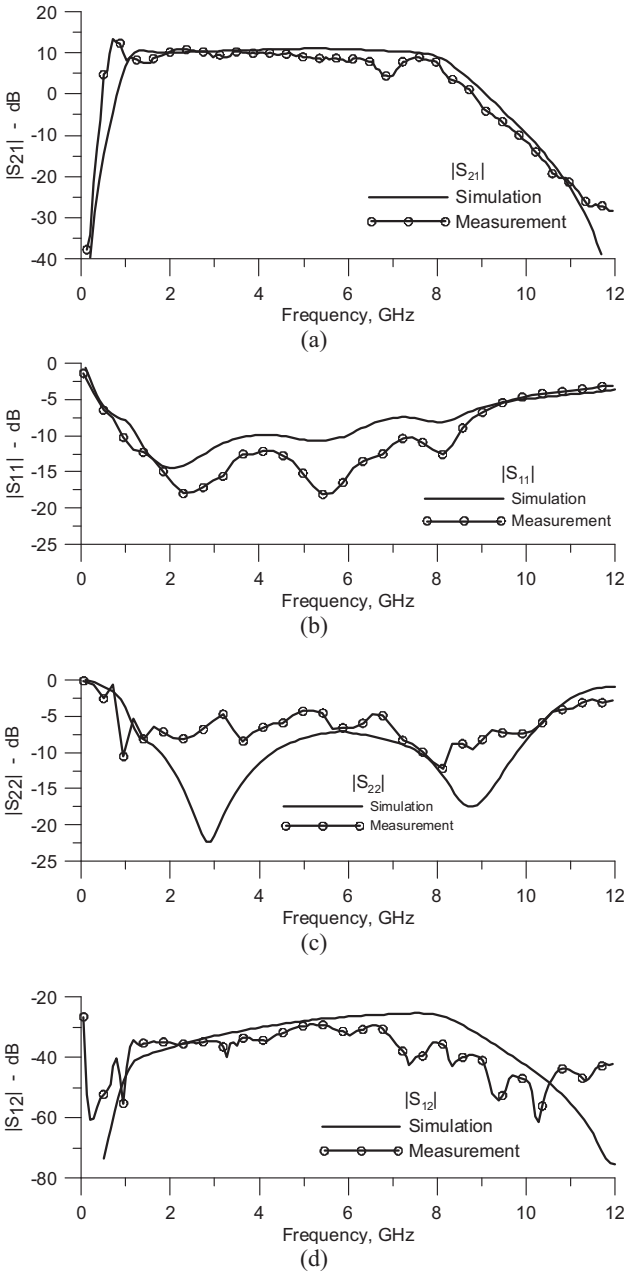


Fig. 7. Simulated and measured small-signal s-parameters of the SSTWPA.
(a) Gain, $|S_{21}|$ (b)$|S_{11}|$ (c)$|S_{22}|$ (d) $|S_{12}|$

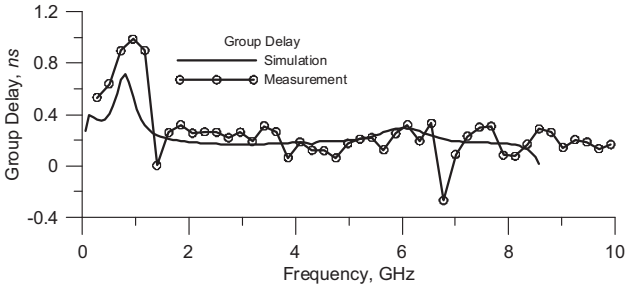
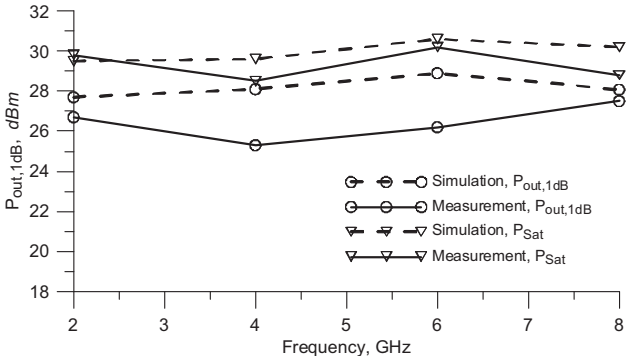
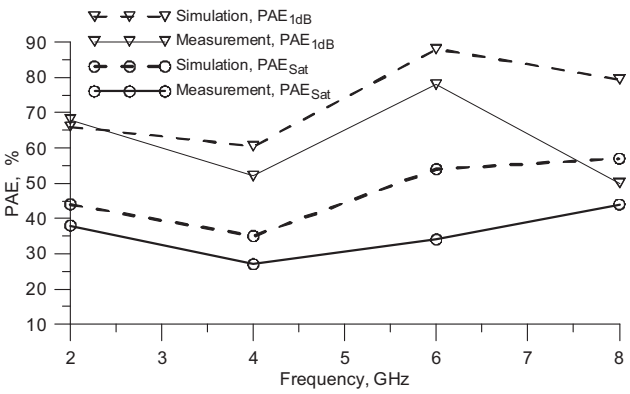


Fig. 8. Group delay performance of the SSTWPA.



(a)



(b)

Fig. 9. (a) Saturated and 1dB compression point power performance of the simulated and measured SSTWPA. (b) PAE performances for the SSTWPA.

6. Conclusions

This paper demonstrated a special case of a wideband travelling wave power amplifier which uses a single transistor operating in Class-A/AB. Realized single stage travelling wave power amplifier comprised of capacitive coupling and frequency dependent lossy artificial transmission-line to enhance the amplifier frequency-bandwidth product, input match and gain flatness response. Output termination impedance of the amplifier is cancelled and the output-line is comprised of an inductive element to achieve an optimum power-bandwidth performance. The SSTWPA was designed using a 0.25μm GaAs PHEMT process. The fabricated amplifier is shown to provide 10dB gain in the 1-to-8GHz band. P_{Sat} and $P_{out,1dB}$ power levels have their peak values at 1W (30dBm) and 0.5W (27dBm) and PAE levels are above 50% and 27% respectively.

Acknowledgment

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7. References

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