VDDDA – New 'Voltage Differencing' Device for Analog Signal Processing

Norbert Herencsar[1], Roman Sotner[2], Bilgin Metin[3], Jaroslav Koton[1], Kamil Vrba[1]

[1] Department of Telecommunications, Brno University of Technology
Technicka 3082/12, 616 00 Brno, Czech Republic
[2] Department of Radio Electronics, Brno University of Technology
Technicka 3082/12, 616 00 Brno, Czech Republic
{herencsn; sotner; koton; vrbak}@feec.vutbr.cz
[3] Department of Management Information Systems, Bogazici University
Hisar Campus, 34342 Bebek-Istanbul, Turkey
bilgin.metin@boun.edu.tr

Abstract

This paper presents a new 'voltage differencing' active building block called voltage differencing differential difference amplifier (VDDDA). The usefulness of the introduced device is demonstrated on novel resistorless voltage-mode first-order all-pass filter and voltage-mode quadrature oscillator design. The pole frequency of the filter can be easily controlled by means of internal transconductance and it provides both high-input and low-output impedances, which is important for cascading. In the oscillator the condition of oscillation and frequency of oscillation can be tuned independently. The theoretical results are verified by SPICE simulations using TSMC 0.18 μm level-7 SCN018 CMOS process parameters with ± 0.9 V supply voltages.

1. Introduction

Since 1970s the current differencing amplifier (or Norton amplifier) is known as the first active building block (ABB) with 'current differencing' capability in the literature [1]. Later on the operational transresistance amplifier (OTRA) [2], differential current conveyor (DCCII) [3], current differencing buffered amplifier (CDBA) [4], and the current differencing transconductance amplifier (CDTA) [5] have also received considerable attention in the literature. The input circuitry of these ABBs contains the so-called current differencing unit (CDU), which has two low-impedance terminals while the DCCII has additional voltage input terminal. In 2008, a set of new ABBs were introduced as counterparts of above mentioned 'current differencing' ABBs [6]. In these ABBs the CDU is replaced by voltage differencing unit (VDU), which is formed by differential-input operational transconductance amplifier (OTA) [7]. In this way, the CDBA is transformed to voltage differencing buffered amplifier (VDBA) [6], [8] and its generalization leads to voltage differencing-differential input buffered amplifier (VD-DIBA) [9], which along with the voltage differencing transconductance amplifier (VDTA) and voltage differencing inverting buffered amplifier (VDIBA), is the most popular nowadays [10]–[14]. As continuation of these works, this paper introduces new versatile 'voltage differencing' ABB so-called voltage differencing differential difference amplifier (VDDDA). The VDDDA can be considered as universal ABB, since it also allows realization of both VDBA and VD-DIBA. As its application grounded capacitor-based novel voltage-mode (VM) first-order all-pass filter (APF) and quadrature oscillator are given. SPICE simulation results are included to support the theory.

Ing. Norbert Herencsar, Ph.D. was supported by the project CZ.1.07/2.3.00/30.0039 of Brno University of Technology. Research described in this letter was also in part supported by the project SIX CZ.1.05/2.1.00/03.0072 from the operational program Research and Development for Innovation, FEKT–S–11–15, and Czech Science Foundation projects under No. P102/11/P489 and P102/09/1681.

2. Circuit Description

The VDDDA is a new six-terminal active device with electronic tuning, which circuit symbol and behavioral model are shown in Figs. 1(a) and (b), respectively. From the model it can be seen that the advantage of the differential-input OTA [7] and differential difference amplifier (DDA) [15], [16] is extended in this new ABB. It has a pair of high-impedance voltage inputs $v+$ and $v-$, a high-impedance auxiliary current output z, a high-impedance voltage inputs v_n and v_p, and low-impedance voltage output w, which value is given by the differential difference of voltages $V_z - V_{v_n} + V_{v_p}$. Hence, the relationship between port currents and voltages of a VDDDA can be described by the following equations:

$$I_z = g_m(V_{v+} - V_{v-}), \quad V_w = \beta_1 V_z - \beta_2 V_{v_n} + \beta_3 V_{v_p}, \quad (1)$$

and the currents of $v+$, $v-$, v_p, and v_n terminals are zero. In Eq. (1), g_m and $\beta_i = 1 - \varepsilon_{vi}$ for $i = 1, 2, 3$ represent transcon-

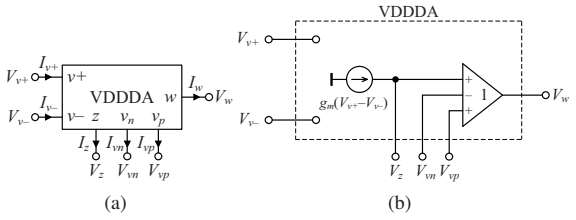

Figure 1. (a) Circuit symbol, (b) behavioral model.

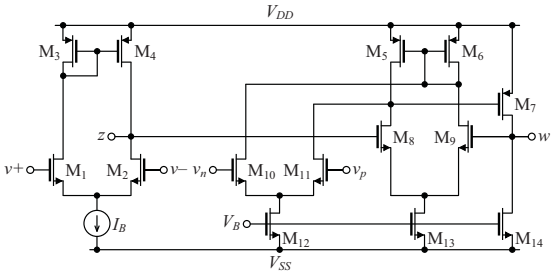

Figure 2. CMOS implementation of VDDDA.

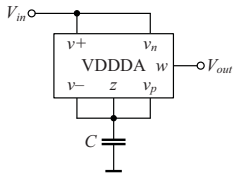

Figure 3. Proposed VM cascadable all-pass filter.

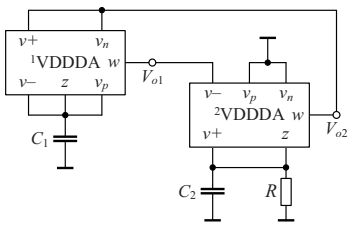

Figure 4. Proposed VM quadrature oscillator.

ductance and non-ideal voltage gains of VDDDA, respectively, and ε_{vi} ($|\varepsilon_{vi}| \ll 1$) denotes voltage tracking error of VDDDA. However, for ideal VDDDA the values of β_i are equal to unity.

Proposed CMOS implementation of the VDDDA is shown in Fig. 2, where transistors M_1–M_4 realize the OTA and M_5–M_{14} form the differential difference stage. Here it is worth noting that the proposed structure can also be effectively used for implementation of VDBA [6] and VD-DIBA [9], if v_n and v_p or only v_p terminals of VDDDA are grounded.

The newly proposed VM first-order APF using single VD-DDA and grounded capacitor is shown in Fig. 3. Considering an ideal VDDDA, i.e. $\beta_i = 1$, routine analysis yields voltage transfer function (TF) in the following form:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{sC - g_m}{sC + g_m}, \tag{2}$$

and the phase response of the filter is given as follows:

$$\varphi(\omega) = -2\tan^{-1}\left(\frac{\omega C}{g_m}\right). \tag{3}$$

As it is seen from the equation above, the phase of voltage TF alters from 0° to –180° while ω changes from $0 \to \infty$.

The pole (ω_p) and zero (ω_z) frequencies of the TF are:

$$\omega_p = \omega_z = \frac{g_m}{C}, \tag{4}$$

and their sensitivity to active parameter and passive element are as $S_{g_m}^{\omega_p,\omega_z} = -S_C^{\omega_p,\omega_z} = 1$ and are unity in relative amplitude.

For a complete analysis of the proposed VM APF it is also important to take into account the non-idealities of the active element used. Considering the aforementioned non-ideal voltage transfers of the VDDDA, the ideal TF in Eq. (2) turns to:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{\beta_2 sC - g_m(\beta_1 - \beta_2 + \beta_3)}{sC + g_m}. \tag{5}$$

Now, the phase response of the filter can be expressed as:

$$\varphi(\omega) = -\tan^{-1}\left(\frac{\beta_2 \omega C}{g_m(\beta_1 - \beta_2 + \beta_3)}\right) - \tan^{-1}\left(\frac{\omega C}{g_m}\right). \tag{6}$$

Subsequently, the zero ω_z and pole ω_p frequencies are not equal and can be given as:

$$\omega_z = \frac{g_m(\beta_1 - \beta_2 + \beta_3)}{\beta_2 C}, \quad \omega_p = \frac{g_m}{C}. \tag{7}$$

It it worth noting that the pole frequency ω_p of the filter can be easily tuned by means of the transconductance of the VD-DDA. However, the mismatch between the pole frequency ω_p and the corresponding zero frequency ω_z affects both the magnitude and phase response of the circuit. Therefore, to receive $\omega_z = \omega_p$ precise design of VDDDA with values of β_i very close to unity is needed.

Typical application area of the all-pass filter is quadrature oscillator [12], [17], which is important circuit is various communication systems [18]. Here introduced new quadrature oscillator shown in Fig. 4 was proposed by cascading the APF to a lossy integrator in a closed loop. Routine circuit analysis yields the following characteristic equation (CE):

$$\text{CE}: \quad s^2 C_1 C_2 R + s(C_1 + C_2 R g_{m1} - 2C_1 R g_{m2}) + g_{m1} = 0. \tag{8}$$

From (8) the condition of oscillation (CO) and the frequency of oscillation (FO) can be evaluated as:

$$\text{CO}: \quad g_{m2} \geq \frac{1}{2}\left(\frac{1}{R} + g_{m1}\frac{C_2}{C_1}\right), \tag{9}$$

$$\text{FO}: \quad \omega_0 = \sqrt{\frac{g_{m1}}{C_1 C_2 R}}. \tag{10}$$

From Eqs. (9) and (10) it is clear that the FO can be controlled by adjusting the value of the resistor R and/or by varying the control current I_{B1} of g_{m1}.

Assuming the matching $R = 1/g_{m2}$, the relationship between the output voltages can be given as:

$$V_{o1} = -jkV_{o2}, \quad \text{where} \quad k = \omega_0 C_2 R, \tag{11}$$

ensuring the output voltages V_{o1} and V_{o2} to be quadrature (the phase difference $\phi = 90°$) and have equal amplitudes if $k = 1$.

3. Simulation Results

To verify the theoretical study, the behavior of the proposed CMOS VDDDA structure and VM APF shown in Figs. 2 and 3, respectively, have been verified by SPICE simulations with DC power supply voltages equal to $+V_{DD} = -V_{SS} = 0.9$ V and $V_B = -0.35$ V. In the design, transistors are modeled by the TSMC 0.18 μm level-7 SCN018 CMOS process

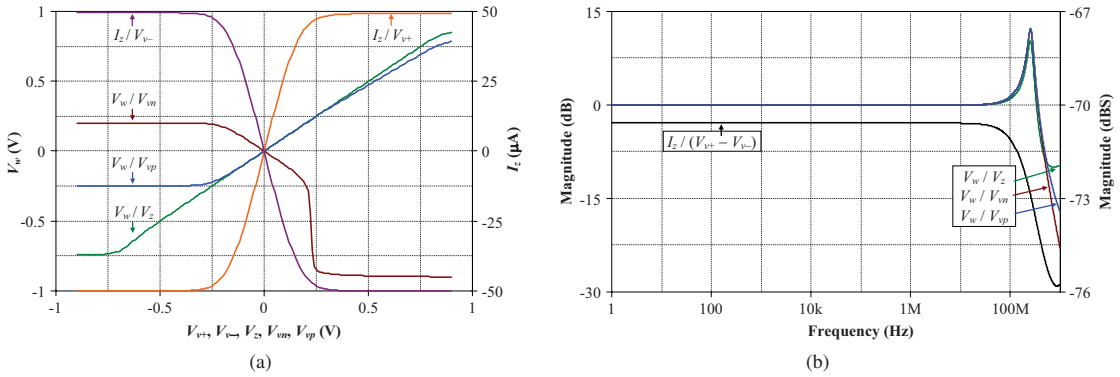

Figure 5. (a) DC and (b) AC analyses of VDDDA in Fig. 2.

Table 1. Transistor dimensions of the VDDDA.

PMOS transistors	W(μm)/L(μm)
M_3, M_4	3.96/1.08
M_5–M_7	3.6/0.18
NMOS transistors	W(μm)/L(μm)
M_1, M_2	9/1.08
M_8–M_{11}	0.72/1.08
M_{12}–M_{14}	2.16/1.08

parameters ($V_{THn} = 0.3725$ V, $\mu_n = 259.5304$ cm^2/(V·s), $V_{THp} = -0.3948$ V, $\mu_p = 109.9762$ cm^2/(V·s), $T_{ox} = 4.1$ nm) [19]. The aspect ratios of the newly designed VDDDA are given in Table 1.

First of all, the performance of the VDDDA was tested by DC and AC analyses and the results are depicted in Fig. 5. From the DC results it can be seen that the maximum values of terminal voltages without producing significant distortion are approximately computed as ±200 mV for the OTA and –0.24 to +0.2 V for the differential difference stage, respectively. The bias current was selected as $I_B = 50$ μA, which results in g_m approximately equal to 300 μA/V. Subsequently, the obtained gains β_i of voltage transfers $V_w/\{V_z, V_{v_n}, V_{v_p}\}$ are equal to 0.997. The AC results show that the maximum operating frequency of the VDDDA is 142.51 MHz. Fig. 6 shows the ideal and simulated phase and gain responses illustrating the electronic tunability of the proposed VM all-pass filter. The pole frequency of the filter is varied for $f_p \cong \{1.015; 1.565; 2.301\}$ MHz via the bias current $I_B = \{25; 50; 110\}$ μA, respectively. In all simulations the value of the capacitor C has been selected as 30 pF. The total power consumption of the APF for simulated pole frequencies from 1.015 to 2.301 MHz varies from 51.8 to 205 μW. To illustrate the time-domain performance, transient analysis is performed to evaluate the voltage swing capability of the filter as shown in Fig. 7. A sine-wave input of 100 mV amplitude and frequency of 1.565 MHz was applied to the filter. Note that the output waveform is very close to the input one. The total harmonic distortion (THD) variations with respect to amplitudes of the applied sinusoidal input voltages at 1.565 MHz are shown in Fig. 8. An input with the amplitude of 100 mV yields THD value of 0.461%.

The proposed oscillator was designed with the following active parameters and the passive element values: $I_{B1} =$ 50 μA, $R = 3.3$ kΩ, and $C_1 = C_2 = 30$ pF, respectively, to obtain the sinusoidal output waveforms with theoretical oscillation frequency of $f_0 = \omega_0/2\pi \cong 1.588$ MHz. In practice, to ensure the startup (build-up) of oscillations and subsequently to satisfy the CO in Eq. (9) the value of I_{B1} is chosen as 60 μA. The simulated oscillation frequency is 1.55 MHz. The waveforms of the quadrature voltages are shown in Fig. 9. The total harmonic distortion (THD) at outputs V_{o1} and V_{o2} were 1.49 % and 1.99 %, repectively.

From the simulation results it can be seen that both solutions are in good agreement with the theory.

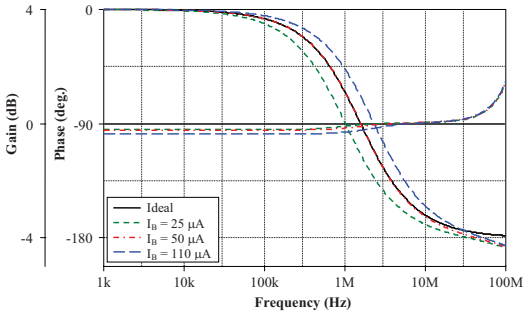

Figure 6. Electronical tunability of the pole frequency of the proposed VM first-order all-pass filter by the bias current I_B.

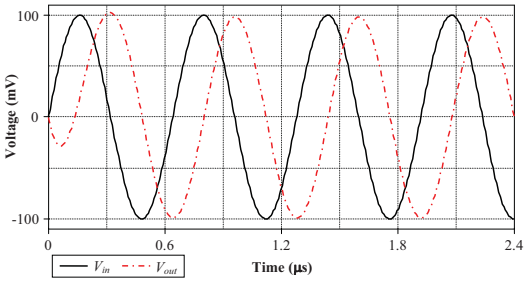

Figure 7. Time-domain responses of the proposed all-pass filter at 1.565 MHz.

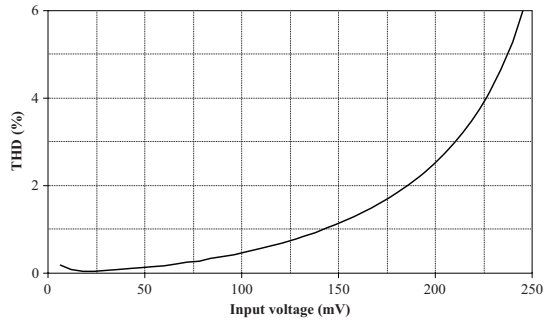

Figure 8. THD variation of the proposed all-pass filter against applied input voltage at 1.565 MHz.

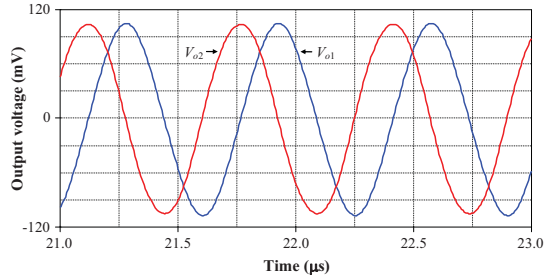

Figure 9. Steady state oscillation waveforms of the quadrature outputs.

4. Conclusion

This paper presents new active element from the group of 'voltage differencing' devices, namely voltage differencing differential difference amplifier. Since the internal structure of the introduced active element contains OTA, it is attractive for resistorless and electronically controllable circuit applications. Therefore, its usefulness is demonstrated on VM APF design, which was used for quadrature oscillator design. The VDDDA can be considered as universal 'voltage differencing' ABB, since using its CMOS implementation both VDBA and VD-DIBA can be realized simpler and more effective way than in [8] and [10] from their transistor count point of view.

5. References

[1] F. Anday, "Realization of n-th order transfer functions using current differencing amplifiers", *Int. J. Electron.*, vol. 42, no. 6, pp. 613–616, 1977.

[2] J. J. Chen, H. W. Tsao, and C. Chen, "Operational transresistance amplifier using CMOS technology", *Electron. Lett.*, vol. 28, no. 22, pp. 2087–2088, 1992.

[3] H. O. Elwan and A. M. Soliman, "A CMOS differential current conveyor and applications for analog VLSI", *Analog Integr. Circ. Sig. Process.*, vol. 11, pp. 35–45, 1996.

[4] C. Acar and S. Ozoguz, "A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filters", *Microelectron. J.*, vol. 30, pp. 157–160, 1999.

[5] D. Biolek, "CDTA - building block for current-mode analog signal processing", in *Proc. of the 16th European Conf. on Circuit Theory and Design - ECCTD 2003*, Krakow, Poland, pp. 397–400, 2003.

[6] D. Biolek, R. Senani, V. Biolkova, and Z. Kolka, "Active elements for analog signal processing: classification, review, and new proposals", *Radioengineering*, vol. 17, no. 4, pp. 15–32, 2008.

[7] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial", *IEEE Circuits Devices Mag.*, vol. 1, pp. 20–32, 1985.

[8] F. Kacar, A. Yesil, and A. Noori, "New CMOS realization of voltage differencing buffered amplifier and its biquad filter applications", *Radioengineering*, vol. 21, no. 1, pp. 333–339, 2012.

[9] D. Biolek and V. Biolkova, "First-order voltage-mode all-pass filter employing one active element and one grounded capacitor", *Analog Integr. Circ. Sig. Process.*, vol. 65, pp. 123–129, 2010.

[10] K. L. Pushkar, D. R. Bhaskar, and D. Prasad, "Single-resistance-controlled sinusoidal oscillator using single VD-DIBA", *Active and Passive Electronic Components*, vol. 2013, Article ID 971936, 5 pages, 2013.

[11] N. Herencsar, R. Sotner, J. Koton, J. Misurec, and K. Vrba, "New compact VM four-phase oscillator employing only single z-copy VDTA and all grounded passive elements", *Electronics and Electrical Engineering (Elektronika ir Elektrotechnika)*, pp. 1–4, accepted in April, 2013.

[12] N. Herencsar, S. Minaei, J. Koton, E. Yuce, and K. Vrba, "New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA", *Analog Integr. Circ. Sig. Process.*, vol. 74, no. 1, pp. 141–154, 2013.

[13] R. Sotner, J. Jerabek, and N. Herencsar, "Voltage differencing buffered/inverted amplifiers and their applications for signal generation", *Radioengineering*, vol. 22, no. 2, pp. 490–504, 2013.

[14] N. Herencsar, O. Cicekoglu, R. Sotner, J. Koton, and K. Vrba, "New resistorless tunable voltage-mode universal filter using single VDIBA", *Analog Integr. Circ. Sig. Process.*, vol. 76, no. 2, pp. 251–260, 2013.

[15] E. Sackinger and W. Guggenbiihl, "A versatile building block: the CMOS differential difference amplifier", *IEEE J. Solid-State Circuits*, vol. 22, pp. 287–294, 1987.

[16] W. Chiu, S.-I. Liu, H.-W. Tsao, and J.-J. Chen, "CMOS differential difference current conveyors and their applications", *IEE Proc. Circuits Devices Syst.*, vol. 143, pp. 91–96, 1996.

[17] S. Minaei and E. Yuce, "Novel voltage-mode all-pass filter based on using DVCCs", *Circuits Syst Signal Process*, vol. 29, pp. 391–402, 2010.

[18] N. Herencsar, A. Lahiri, K. Vrba, and J. Koton, "An electronically tunable current-mode quadrature oscillator using PCAs", *Int. J. Electron.*, vol. 99, no. 5, pp. 609–621, 2012.

[19] TSMC 0.18 μm level-7 SCN018 CMOS technology parameters [online]: ftp://ftp.isi.edu/pub/mosis/vendors/tsmc-018/t44e_lo_epi-params.txt