Novel Current-Mode Second-Order Square-Root-Domain Highpass and Allpass Filter

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Abstract

In this paper, current-mode second-order square-root-domain highpass, and allpass filters are proposed by using only a circuit. Literature survey showed that, current-mode second-order highpass and allpass filters are not proposed. The proposed circuit is derived from first-order blocks. The presented of the first-order blocks are based on the state-space synthesis method with two subcircuit; square-root and squarer/divider circuits. The proposed circuit has one input and one output and can realize highpass (HP), and allpass (AP) responses without any changes in the circuit topology. Only MOS transistors and grounded capacitors are required to realize the filter circuit. The center frequency of the filters can be electronically tuned by changing external currents. Time and frequency domain simulations are performed using PSPICE program for the filters to verify the theory and to show the performance of them. For this purpose, the filter is simulated by using *TSMC 0.35 µm Level 3 CMOS* process parameters.

1. Introduction

Companding filters are studied by many researchers, because these filters have the advantages of high-frequency operation, electronically tunable, and large dynamic range under low power supply voltages [1-5]. The companding filters, in which the input signals are first compressed, then properly processed and finally expanded at the output such as log-domain and square-root-domain filters [1-5].

Companding filters are translinear circuits, whose principle based on the exponential I–V characteristics of BJTs and MOS transistors in weak inversion region [6-7]. The quadratic law of MOS is the linear transconductor that was proposed by Bult [8]. The MOS translinear (MTL) principle is derived by Seevinck [9] from the bipolar translinear (BTL) principle [6]. The quadratic law of MOS in strong inversion region and saturation region were used [3], [10-11]. MOS translinear approach is used to implementation of several analog building blocks such as square-root domain integrators [10], [12], differentiators [13], oscillators [14-15], filters [16-20]. Also, there are a lot of papers in literature about the current-mode geometric-mean and multiplier-divider circuits that are the basic building blocks for square-root-domain circuits [17-18]. The current-mode multiplier-divider has been realized using both geometric mean [21] and squarer-divider blocks [22-23].

A number of square-root-domain filters, including both voltage-mode and current-mode approach were presented by the authors in the literature. Second-order current-mode lowpass and bandpass biquads are given in [3], second-order voltage-mode lowpass and bandpass biquads are presented in [18], second order current-mode lowpass was given in [17] and is second order voltage-mode lowpass is presented in [20] and the fifth-order Chebyshev lowpass was given in [24]. Literature survey shows us, second-order highpass and allpass are not proposed. In this paper, by using the first order current-mode lowpass and via square-root-domain techniques and then the second order current-mode highpass and allpass filters were proposed by using this first order filter blocks. The proposed circuit has one input and one output and can realize highpass (HP), and allpass (AP) responses without any changes in the circuit topology.

2. The proposed current-mode second-order square-root-domain HP and AP Filters

2.1. The realizations of first-order square-root-domain LP filter circuit

Up to now, current-mode square-root domain first-order lowpass filters have been presented in the literature [4], [25-27]. First order lowpass filter transfer function can be written as follows ,

$$T_{LP}(s)=\frac{Y(s)}{U(s)}=\frac{I_{out}(s)}{I_{in}(s)}=\frac{a_2\omega_0}{s+a_1\omega_0} \tag{1}$$

where ω_0 is the cut-off frequency of filter and, a_1 and a_2 are constant. Transfer function was transformed to the following state-space equation [27]:

$$\dot{x}_1=-a_1\omega_0 x_1+a_2\omega_0 u \tag{2}$$

The output equation is [15]

$$y_{LP}=x_1 \tag{3}$$

where u is the input, y is the output and, x_1 is the state variable. The Eq.(2) can be transformed into a set of nodal equations by using square mappings on the input and state variables. The following mappings can therefore be applied to quantities in equation:

$$x_1=\frac{\beta}{2}(V_1-V_{th})^2 \tag{4}$$

where $\beta = \mu_0 C_{ox}(W/L)$, V_1, and V_{th} are the device transconductance parameter, the gate-to-source voltage and the threshold voltage, respectively.

The derivative of x_1 is given by

$$\dot{x}_1 = \beta \dot{V}_1 (V_1 - V_{th}) \tag{5}$$

The above relationship was applied to Eq.(2) then they are arranged to form the following nodal equations [27]:

$$C\dot{V}_1 = -a_1\sqrt{I_1}\,\frac{\omega_0 C}{\sqrt{2}\sqrt{\beta}} + a_2\,\frac{\omega_0 C}{\sqrt{2}\sqrt{\beta}}\,\frac{I_{in}}{\sqrt{I_1}} \tag{6}$$

I_0 are positive constants which are given by,

$$I_0 = \frac{\omega_0^{\,2} C^2}{\beta} \tag{7}$$

$$I_{0i} = a_i^2 I_0 \quad i = 1,2 \tag{8}$$

Eq. (3), Eq. (6) and Eq. (7) can be arranged as,

$$C\dot{V}_1 = -\sqrt{\frac{I_{01} I_1}{2}} + \sqrt{\frac{I_{02} I_{in}^2}{2I_1}} \tag{9}$$

$$y_{LP} = x_1 = \frac{\beta}{2}(V_1 - V_{th})^2 \tag{10}$$

The realizations of first-order square-root domain LP filter circuits using Eq..(9) and Eq.(10) is shown in Fig.1. The cut-off frequency of LP filter is

$$\omega_0 = \frac{\sqrt{\beta}\sqrt{I_0}}{C} \tag{11}$$

It should be noted that ω_0 can electronically be tuned by changing I_0

To obtain the proposed filter circuit, the filter structures need to be connected two subcircuits. First subcircuit is square-root-domain structure and second subcircuit consists of square-root-domain structure and squarer/divider structures. Current-mode square-root and current-mode squarer/divider circuits are the MOS translinear MTL circuits [22-23]. Fig.2 and Fig. 3 show the square-root and squarer/divider circuits [22-23]. Second subcircuit block diagram is shown in Fig. 4. Current-mode squarer/divider circuit is derived from [20].

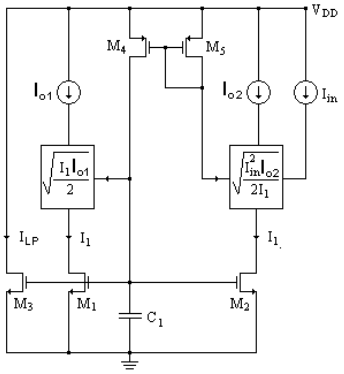

Fig. 1. The first-order square-root-domain lowpass filter.

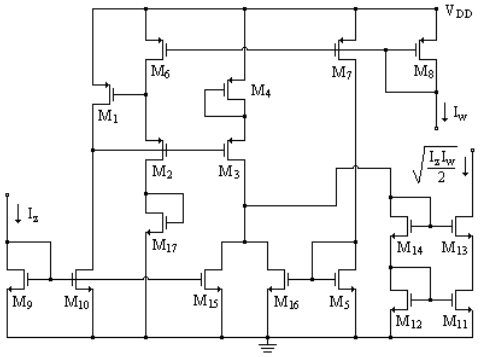

Fig. 2. Current-mode square-root circuit

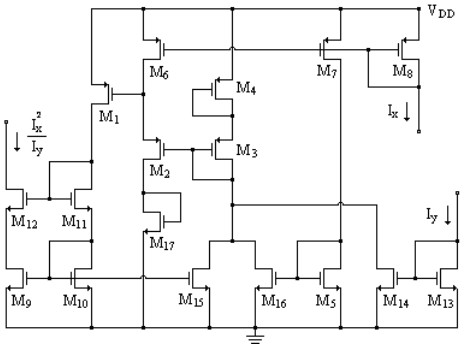

Fig. 3. Current-mode squarer/divider circuit

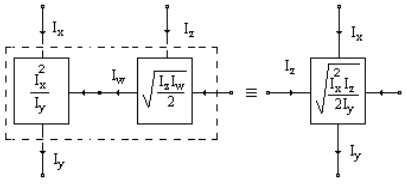

Fig. 4. Second subcircuit: Current-mode square-root circuit connected to current-mode squarer/divider circuit.

The transistor dimensions are chosen as W/L=7μm/0.7μm for M_1, M_{15}, and M_{17}, W/L=14μm/0.7μm for M_2-M_{14}, and W/L=3.5μm/0.7μm for M_{16} for square–root and W/L=7μm/0.7μm for M_1, M_2 and M_{15}-M_{17}, and W/L=14μm/0.7μm for M_3-M_{14}, for squarer–divider sub circuits and W/L=3.5μm/0.7μm for M_1, M_2 and M_3, W/L=14μm/0.7μm for M_4–M_5 for LP

2.2The realizations of second-order square-root domain HP and AP filter circuit

The second order HP and AP filter block diagram can be realized by using two first order low-pass filter blocks as shown in Fig. 5. The second order HP and AP filter circuits can be achieved as shown in Fig. 6.

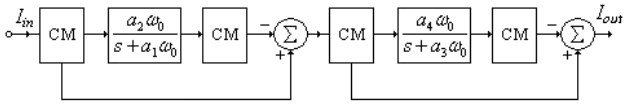

Fig. 5. The second order multi-output filter block diagram

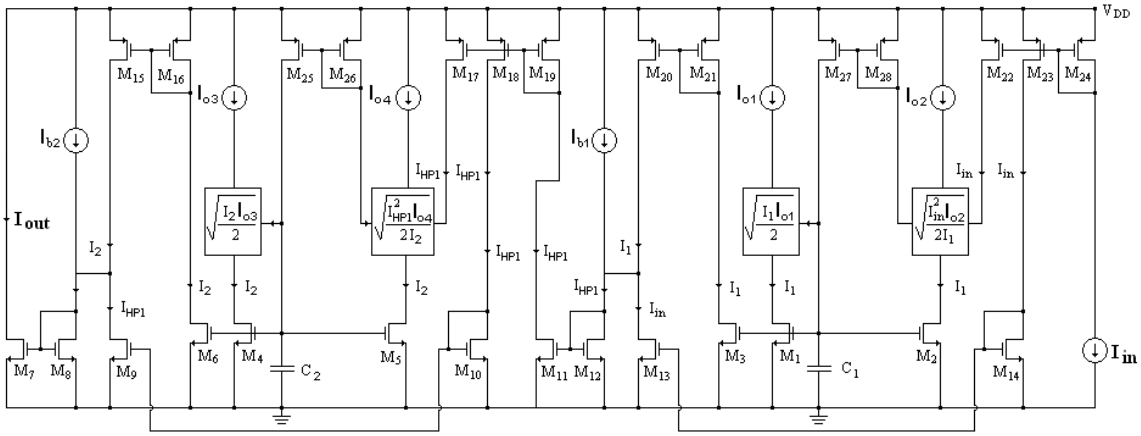

Fig. 6. The second order current-mode multi-output filter

The aspect ratio of MOS transistors in second-order highpass filter circuit are chosen as W/L=3.5μm/0.7μm for the transistors M_1~M_6 and W/L=14μm/0.7μm for the transistors M_7~M_{28}.

The transfer function of output filter in Fig. 6 can be extracted routine analysis. Then, the current equations at nodes that are capacitances are connected and the output variable can be written as follows,

$$C\dot{V}_1 = -\sqrt{\frac{I_{01}I_1}{2}} + \sqrt{\frac{I_{02}I_{in}^2}{2I_1}} \tag{12}$$

$$C\dot{V}_2 = -\sqrt{\frac{I_{03}I_2}{2}} + \sqrt{\frac{I_{04}I_{HP1}^2}{2I_2}} \tag{13}$$

$$I_{LP1} = I_1 \tag{14a}$$

$$I_{HP1} = I_1 - I_{in} \tag{14b}$$

$$I_{OUT} = I_2 - I_{HP1} \tag{14c}$$

The transfer function of output filter is given as written in Eq. (15)

$$I_{OUT} = I_2 - I_{HP1} = \frac{s^2 + (a_1 - a_2 + a_3 - a_4)\omega_0 s + (a_2 - a_1)(a_4 - a_3)\omega_0^2}{s^2 + (a_1 + a_3)\omega_0 s + a_1 a_3 \omega_0^2} I_{in} \tag{15}$$

If the constants are chosen as a_1=a_2=a_3=a_4=1 the transfer function in Eq. (15) is reduced as

$$\frac{I_{out}}{I_{in}} = \frac{s^2}{s^2 + 2\omega_0 s + \omega_0^2} \tag{16}$$

If the constants are chosen as a_1=a_3=*1* and a_2=a_4=*2* the transfer function in Eq. (15) is reduced as

$$\frac{I_{out}}{I_{in}} = \frac{s^2 - 2\omega_0 s + \omega_0^2}{s^2 + 2\omega_0 s + \omega_0^2} \tag{17}$$

The filter quality factor can be increased by adding feedback subcircuit. The Eq.(16) is HP filter and Eq.(17) is AP filter transfer function. The natural frequency of HP and AP filters are

$$\omega_0 = \frac{\sqrt{\beta I_0}}{C} \tag{18}$$

It should be noted that ω_0 can electronically be tuned by changing I_0

3. Simulation Results

The proposed second-order square-root domain filters were simulated by *TSMC 0.35μm Level 3 CMOS* process parameters. The circuits parameters are chosen as, V_{DD}=*3V,* I_o=*40μA* and *C=20pF*. The natural frequency of filters is about f_o=*1MHz*. The gain and phase response of second-order current-mode square-root-domain HP and AP filters are shown in Fig. 7 and Fig. 8, respectively.

The gain responses of second-order HP and AP filters for different natural frequency could be obtained by varying external dc currents value I_0. The center frequency of the second order band-pass filter changes from about *350 kHz* to *1000 kHz*, when I_0 dc bias current is changed from *4μA* to *40μA*. Thus the natural frequency of the filters can be adjusted in a frequency range of *650 kHz*. The cut-off frequency tuning range for gain

responses of the second order HP and AP filters are shown in Fig. 9 and Fig. 10 respectively and tuning range for phase responses of the second order AP filter is shown in Fig. 11.

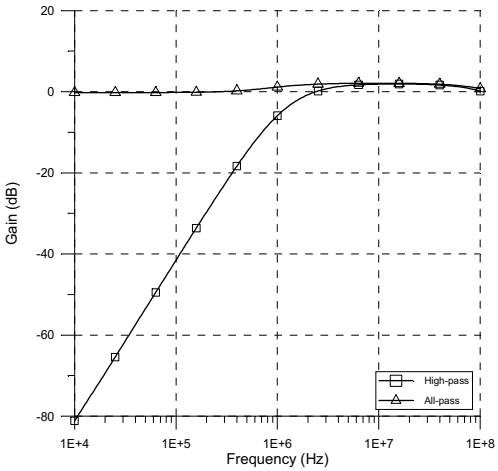

Fig. 7. Gain responses of second-order HP and AP filters

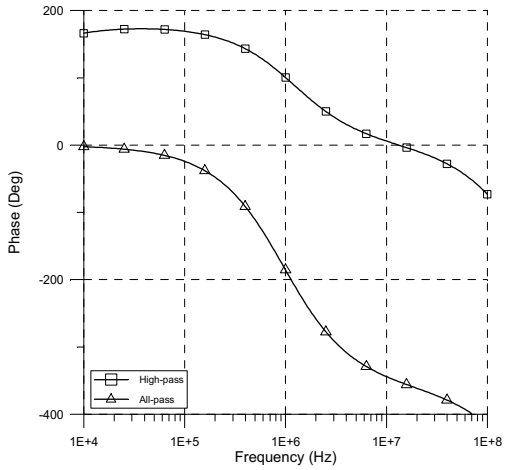

Fig. 8. Phase response of second-order current-mode square-root-domain filters

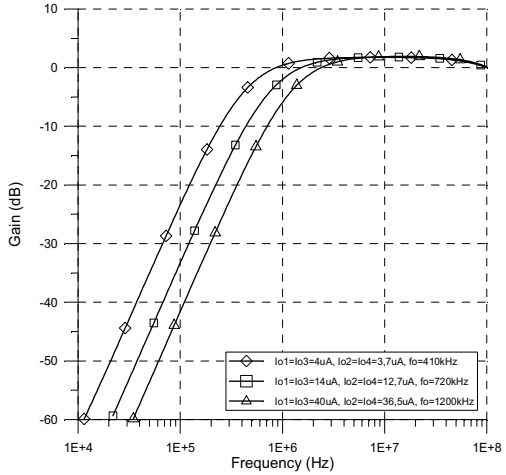

Fig. 9. Gain responses of second-order HP filter for different natural frequency

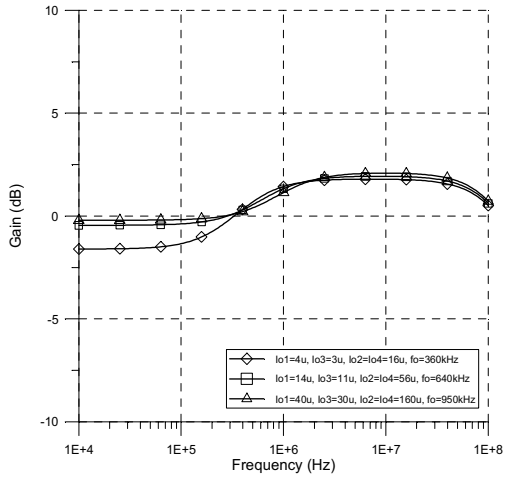

Fig. 10. Gain responses of second-order AP filter for different natural frequency

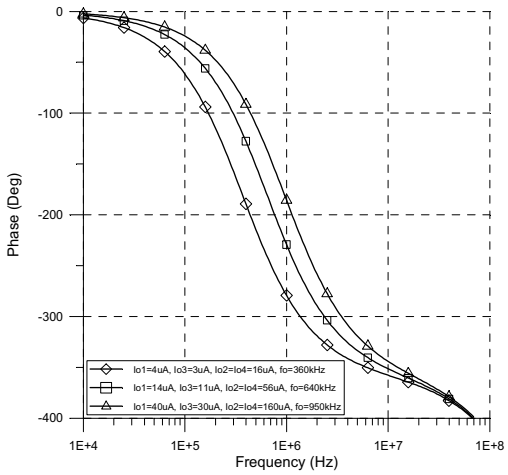

Fig. 11. Phase responses of second-order AP filter for different natural frequency

Fig.12 shows the time-domain response of the second order AP filter. A sine-wave input at a frequency of *950 kHz* was applied to the filter.

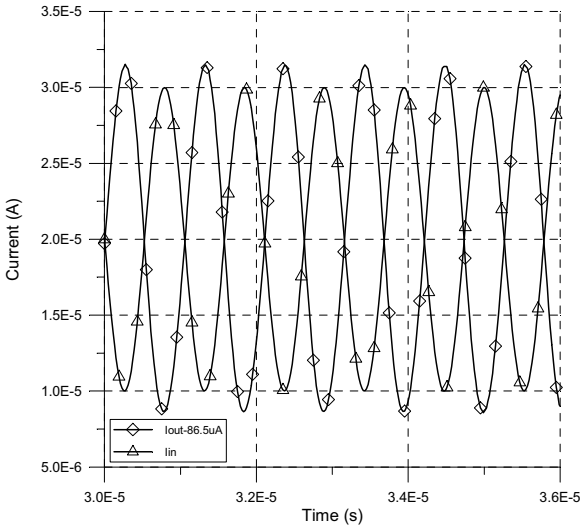

Fig. 12. Time-domain response of second-order AP filter

The HP and AP output signal's THD (Total harmonic distortion (%)) were measured as *1.27%* and *2.65%* respectively. The filter was set to *1.0MHz* cut-off frequency with $I_0=40\mu A$, and the input frequency was also set to this value. Then, a sinusoidal signal with $10\mu A$ peak-to-peak amplitude was applied to the filter. Total power dissipation of the filter is less than *5mW*.

4. Conclusion

Second-order current-mode square-root-domain highpass, and allpass filters structures are presented. A systematic synthesis procedure to derive the filter circuit is also given. PSPICE simulations are provided to confirm the theoretical analysis. The presented filters have the following advantages:

i) realizing linear system with inherently nonlinear circuit building blocks.
ii) can be electronically tuned,
iii) employs only MOSFETs and grounded capacitor,
iv) suitable for VLSI (very large-scale integration) technologies.
v) suitable for low voltage/power applications.

It is expected that the proposed current-mode square-root-domain first-order filters will be useful in the design of analog signal processing applications.

5. References

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