An X-Band SiGe Driver Amplifier

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Abstract

In this paper, an integrated driver amplifier operating at X-Band (7-10 GHz) frequencies is presented. This driver amplifier is implemented in a 0.25-µm SiGe BiCMOS process. The two-stage push-pull amplifier uses on-chip transformers for the purpose of single-ended to differential signal conversion as well as input and output impedance matching. Operating with a 3.3 V supply voltage, the amplifier exhibits a measured output power of 13 dBm at 1-dB compression point with power-added efficiency of 12% and small signal gain of 21 dB.

1. Introduction

SiGe BiCMOS processes continue to achieve higher performance with increasing transition frequency, better noise performance than their CMOS counterparts. SiGe heterojunction bipolar transistor technology delivers good RF performance and higher integration level with basic CMOS process. It is possible to implement SiGe high frequency transceivers and CMOS digital functions, power management circuits on the same die with SiGe BiCMOS process [1].

This paper presents a SiGe driver amplifier to be used as a building block for an X-Band transceiver module. The amplifier utilizes push-pull architecture with input/output transformers providing single-ended to differential signal conversion and input/output impedance matching. Push-pull architecture is known for its good second harmonic suppression and robustness against parasitics [2], [3].

2. Amplifier Design

Push-pull configuration requires differential input signals to operate properly. Integrated transformers have been used as baluns at X-Band amplifiers [4]-[6]. Similarly, the driver amplifier uses two integrated transformers which are utilized as input and output baluns. The simplified circuit diagram of the driver amplifier is given in Fig. 1.

2.1. Technology

In this work, a commercial 0.25-µm SiGe BiCMOS process is used. This process offers three different types of SiGe HBTs. The first stage employs the high performance transistors with peak transition frequency, f_T=110 GHz and maximum oscillation frequency, f_{max}=180 GHz. The collector-emitter breakdown voltage of the high performance transistor is above

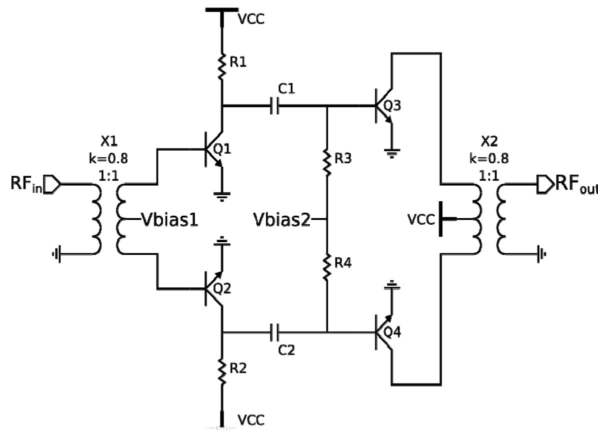

Fig. 1. Simplified circuit diagram of the driver amplifier

2 V. Second stage is designed using the medium voltage transistors with peak f_T=45 GHz and f_{max}=140 GHz. The collector-emitter breakdown voltage of the medium voltage transistor is higher than that of the high performance transistors. Passive devices such as poly resistors and metal-insulator-metal capacitors are available in the process. This technology also offers five metal layers, top two metal layers being thick metal layers to build passive elements such as inductors, transmission lines, transformers, etc.

2.2. Input and Output Transformers

The two uppermost thick metal layers are used to build X1 and X2 transformers. Input transformer X1 provides single-ended to differential conversion of the input signal and the impedance matching. Similarly, output transformer X2 provides differential to single-ended conversion of the output signal and the impedance matching. X1 and X2 transformers are identical in terms of structure, size and specifications. The inductance of primary and secondary windings are L_p=L_s=1.4 nH, corresponding to 1:1 turn ratio. The input capacitance of the first stage, the output capacitance of the second stage and the coupling between transformers are used to generate necessary resonances for input and output impedance matching. Bondwire inductances and pad capacitances are also taken into account. Simulated insertion loss of both transformers is below 1.1 dB and it is affected by the insulator thickness between the two uppermost metal layers. Symmetrical windings of the transformer ensure differential signaling with below 0.1 dB simulated amplitude imbalance.

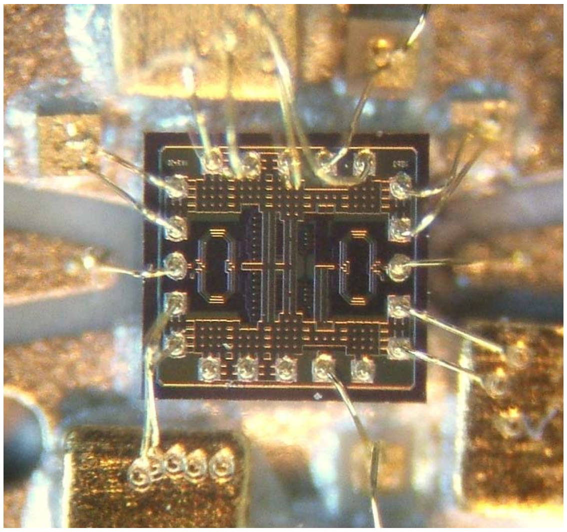

Fig. 2. Die photo of the driver amplifier

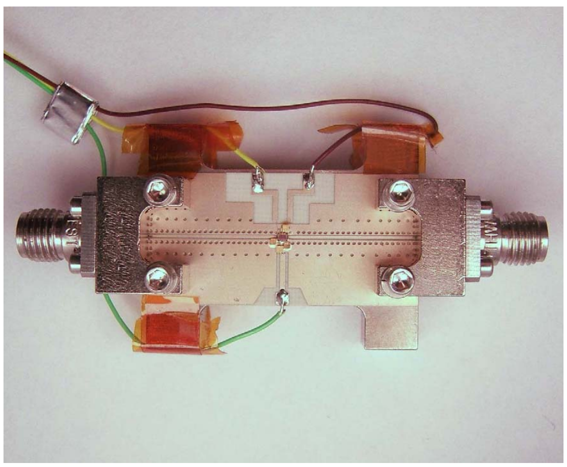

Fig. 3. Test module

2.3. Circuit Design

The circuit diagram in Fig. 1 shows that the driver amplifier consists of two stages. Both stages utilize common emitter configuration. First stage is designed using high performance transistors, Q1 and Q2, with load resistors, R1 and R2. Differential output of the first stage is connected to the second stage via ac-coupling capacitors, C1 and C2. Second stage employs medium voltage transistors, Q3 and Q4, with inductive load from primary winding of X2. Although it is not shown in the circuit diagram for simplicity, both stages of the amplifier have emitter degeneration to improve linearity and to prevent thermal runaway. Biasing circuits of both stages are simple current mirrors with their corresponding transistors. Biasing circuits are also not shown in the circuit diagram. First stage is biased in class-A mode of operation with bias voltage applied to center tap of X1. Second stage is biased in class-AB mode of operation with bias voltage applied through resistors, R3 and R4. The bias voltages of both stages can be adjusted externally.

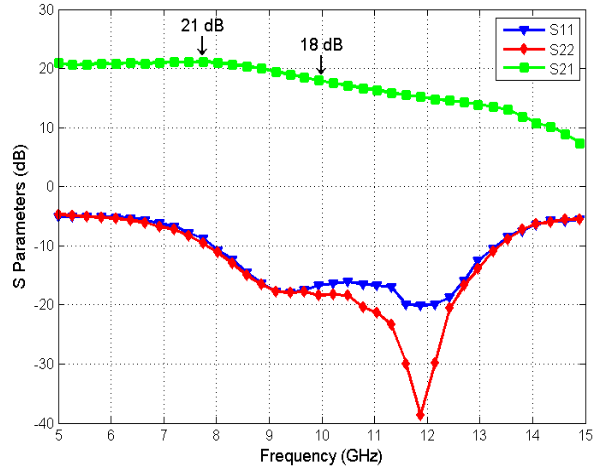

Fig. 4. Measured S-parameters of the amplifier

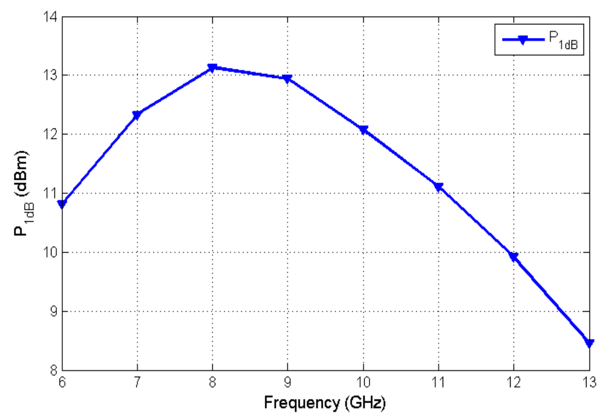

Fig. 5. Measured output power at 1-dB compression point

3. Measurements

Fig. 2 shows the die photo of the manufactured driver amplifier. The die area is 1×1 mm^2 and the size of the amplifier core without pads is 0.8×0.8 mm^2.

The test module size is 58×25 mm^2 including RF connectors. Input and output of the test module are connected to the amplifier via 50-Ω conductor-backed coplanar waveguides. No external components are used for the input and the output impedance matching. Thin-film capacitors are placed near the amplifier die for decoupling purposes. The test module is shown in Fig. 3.

S-parameter measurement results of the driver amplifier are given in Fig. 4. The maximum small signal gain of the amplifier is 21 dB at 7.8 GHz with 3-dB drop point at 10 GHz. The plot also shows better than 8 dB return loss for the 7-10 GHz band and better than 10 dB for the 8-10 GHz band.

Measured output power of the amplifier at 1-dB compression point over the 6-13 GHz band can be seen in Fig. 5. The amplifier achieves a maximum output power of 13 dBm at 8 GHz. Saturated output power of the amplifier is over 14 dBm at the same frequency.

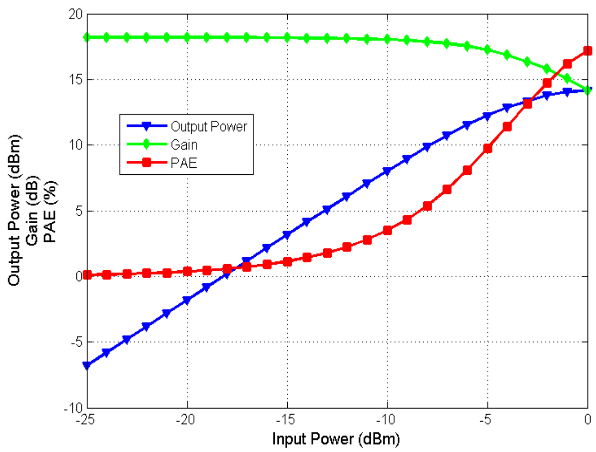

Fig. 6. Output power, gain and power-added efficiency versus input power at 10 GHz

Fig. 6 shows the power-added efficiency, gain, and output power of the amplifier versus increasing input power at 10 GHz. The driver amplifier achieves a power-added efficiency of 12% at 1-dB compression point, increasing to a maximum of 18% at saturation.

4. Conclusion

An integrated driver amplifier operating at X-Band is presented. The two-stage amplifier utilizes push-pull configuration with two integrated transformers as the input and the output baluns. The amplifier is implemented in a 0.25-µm SiGe BiCMOS technology and achieves a small-signal gain of 21 dB, an output power of 13 dBm at 1-dB compression point with 12% PAE under a supply voltage of 3.3 V. It is possible to improve small-signal gain, linearity and efficiency of the amplifier by implementing an interstage impedance matching network.

5. References

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