New Improved CMOS Implementation of Differential Difference Current Conveyor

Alper DURUK[1] Hakan KUNTMAN[2] Ali TOKER[3] Oğuzhan ÇIÇEKOĞLU[4]

[1,2,3]İstanbul Technical University, Faculty of Electrical and Electronics Engineering, Department of Electronics and Communication Eng., 80626, Maslak, İstanbul, TURKEY
Tel:+90 212 2853554, Fax:+90 212 285 3679
[1]E-mail: alper@ehb.itu.edu.tr [2] E-mail: kuntman@ehb.itu.edu.tr [3] E-mail: alitoker@ehb.itu.edu.tr
[4] Boğaziçi University, M.Y.O. Electronics Prog. 80815 Bebek-İstanbul, TURKEY
[4]E-mail: cicekogl@boun.edu.tr

Abstract

The differential difference current conveyor DDCC can be considered as an extension of the second generation current conveyor CCII and is especially suitable for applications demanding differential or floating inputs. In this paper we present an improved CMOS implementation of the noninverting differential difference current conveyor DDCC+. The performance of the proposed circuit is illustrated on DC and AC characteristics with SPICE simulations.

1. Introduction

The differential voltage current conveyor and the differential difference current conveyor can be considered as an extension of the second-generation current conveyor CCII. The CCII is a versatile building block providing the possibility of implementing a variety of high performance circuits such as wide band active filters and oscillators. However, the CCII has a disadvantage that only one of the input terminals has a high-input impedance which is especially evident if processing of differential signals is needed. To overcome this disadvantage new active elements such as DVCC and DDCC are introduced [1,2]. Furthermore it has been shown these new building blocks are especially suitable for applications demanding differential or floating inputs like impedance converter circuits, current-mode instrumentation amplifiers, analogue multipliers, squarers and square rooters [1,2].

The differential difference current conveyor DDCC+ whose circuit symbol is shown in Fig.1 is characterised by

$$\begin{bmatrix} I_{y1} \\ I_{y2} \\ I_{y3} \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

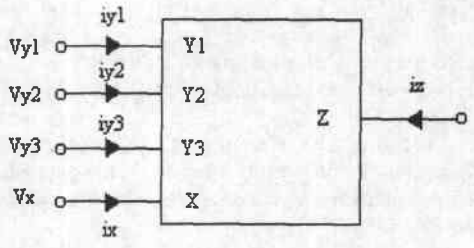

Figure 1 Circuit symbol of DDCC+

The first CMOS implementation circuit of the DDCC+ given in principle [1] is constructed with two differential stages forming a high-gain stage with a current mirror where an additional current mirror is used to build the z output.

In this paper we present an improved CMOS implementation of the DDCC+. The performance of the circuit is illustrated on DC and AC characteristics with SPICE simulations.

2. Circuit Description

The proposed improved CMOS implementation of the DDCC+ is shown in Fig.2. Starting from the same realisation concept given in [1] the building blocks are replaced with high-performance counterparts to extend the overall performance of the DDCC+. Three basic circuit blocks are used to implement the proposed DDCC+.

First: The input transconductance elements are constructed with two differential amplifiers. To obtain a large input range the differential amplifiers are formed by the high-performance topologies consisting of M1-M8, M19 and M9-M16, M20 [3]. The high-gain stage is composed of a current-mirror, M17-M18, which converts the differential current to a single-output current.

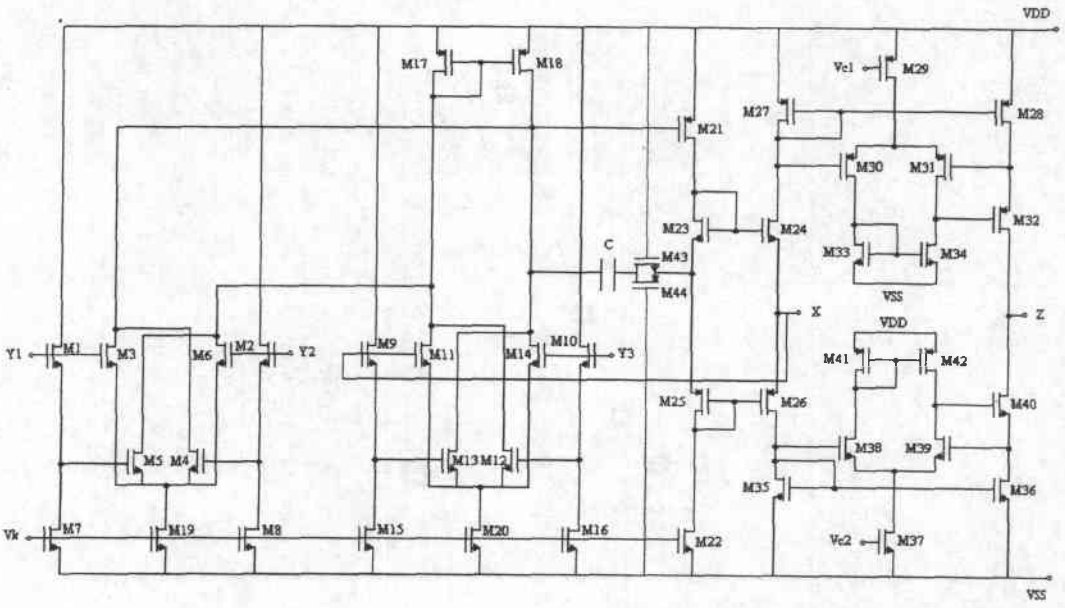

Figure 2 Improved implementation of CMOS DDCC+

Second: To provide low-output resistance at the x terminal the topology consisting of M21-M26, namely CMOS class AB current mirror, providing a good tracking is introduced to form the x terminal [4]. From the output node of the gain stage (node x) negative feedback is applied to the gates of M9 and M11, which yields the following relationship between the four input terminals:

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \qquad (2)$$

M43 and M44 are intended for frequency compensation to provide stability.

Third: In recent works it has been demonstrated that high performance current mirrors are necessary to improve the performance of the current output stages [5-8]. The output terminal z is constituted with a class AB CMOS current output stage consisting of M27-M42 to reduce the tracking error of i_z [5,6]. In this output stage two enhanced cascode current mirrors have been used to obtain very small mirroring errors and a very high output resistance. These particular mirrors are configured by including one of each differential amplifiers consisting of M29-M34 and M37-M42 which ensure minimisation of mirroring errors and at the same time maximisation of the output resistances by the use of active feedback. Note that, the very high output impedance of enhanced cascode current mirrors enables proper operation especially at low frequencies. Note also that the differential gain stages providing active feedback yield larger gain at low operating currents, which decreases the total power consumption of the circuit. As it is stated in the literature that a frequency compensation would be necessary in active feedback cascode current mirrors in case of insufficient phase-margin depending of the design conditions of the circuit [6].

3. Simulation Results

The behaviour of the newly improved CMOS DDCC+ is illustrated with SPICE simulation program. The power supply voltages were chosen as V_{DD} = 5V, V_{SS} = -5V. The biasing voltages are taken as V_k = -3.8V, V_{c1} = 4.1V and V_{c2} = -4.1V. The SPICE simulations were performed with MIETEC 1.2μm CMOS model parameters. Fig.3 illustrates the simulated DC V_X = f(V_{Y1}, V_{Y2}, V_{Y3}) characteristics of the proposed CMOS DDCC+ circuit. In Fig.3 the x terminal voltage V_x is plotted against the input voltage V_{Y1}-V_{Y2} for different V_{Y3} values taken as parameter. Furthermore, the variations of the currents i_x and i_z at the x and z terminals with the input voltage V_{Y1}-V_{Y2} are given in Fig.4. Moreover, the variation of the tracking error ΔI= (Ix-Iz) is also added to Fig.4.

The input linearity range is determined from Fig.3 as -2.4V ≤ V_{Y1}-V_{Y2} ≤ 2.26V for V_{Y3} = 0. The tracking error ΔI= (Ix-Iz) is found from Fig.4 of the order of several ten nanoampers in the range of -800μA ≤ (I_X, I_Z) ≤ 800μA. SPICE simulations yield the output resistances at X and Z terminals as r_X = 0.53Ω and r_Z = 13.65GΩ, respectively.

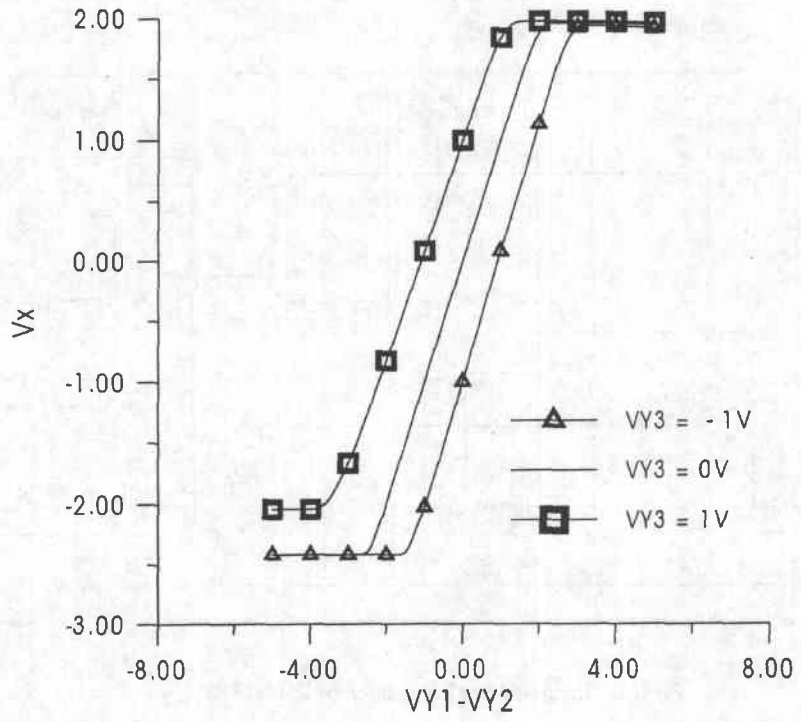

Figure 3 Simulated DC $V_X = f(V_{Y1}, V_{Y2}, V_{Y3})$ characteristics of proposed CMOS DDCC+ circuit.

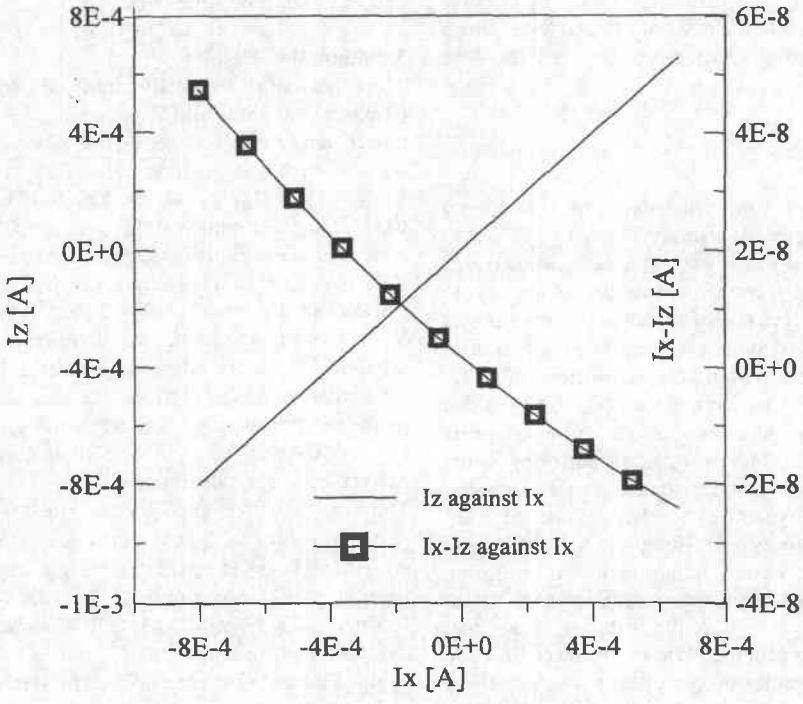

Figure 4 Variation of I_Z against I_X and variation of tracking error $\Delta I = (Ix-Iz)$ against I_X.

The 3dB bandwidth of the voltage gain $v_x/(v_{y1}-v_{y2})$ and and the current-gain i_z/i_x were determined for R_x =1kΩ and R_z = 1kΩ as f_{3dBv} = 24.6MHz and f_{3dBi} = 35.4MHz, respectively. From the simulation results it can be easily observed that the proposed circuit provides a large linearity range and a wide bandwidth.

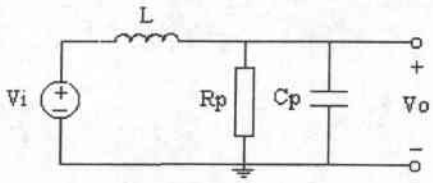

Figure 5. RLC low-pass filter

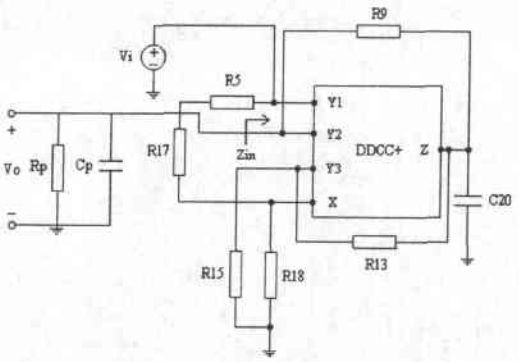

Figure 6. RLC filter constructed with an inductance simulator employing DDCC+.

Furthermore an application example is given to demonstrate the performance of the proposed CMOS DDCC+ circuit. The aim is to simulate a non-grounded inductance and construct a second-order lowpass LC filter illustrated in Fig. 5 by the use of the derived circuit. The transfer function of the low-pass LC circuit is given by

$$F(s)=\frac{V_o(s)}{V_i(s)}=\frac{\frac{1}{LC_p}}{s^2+\frac{s}{R_pC_p}+\frac{1}{LC_p}} \qquad (3)$$

where the pole angular frequency and the quality factor are written by

$$\omega_o=\left(\frac{1}{LC_p}\right)^{\frac{1}{2}} \qquad (4)$$

$$Q=\sqrt{\frac{C_p}{L}}R_p \qquad (5)$$

Choosing R_p = 10k, C_p = 0.23nF and L = 27mH a pole frequency of f_o=63.867kHz and a quality factor of Q=0.923 are obtained. Replacing the inductor in Fig. 5 with an inductance simulator constructed with DDCC+ the circuit in Fig.6 is obtained.

The subcircuit consisting of the DDCC+, C20, R5 - R18 acts a lossless inductance simulator where the impedance seen between Y1 and Y2 terminals is given by

$$Z_{in}=sC_{20}\frac{R_{18}}{R_{13}}(R_{13}+R_{15})(R_5+R_9+R_{17}) \qquad (6)$$

which yields an equivalent inductance

$$L=C_{20}\frac{R_{18}}{R_{13}}(R_{13}+R_{15})(R_5+R_9+R_{17}) \qquad (7)$$

under assumption of

$$R_{15}(R_5+R_9+R_{17})=R_{18}(R_5+R_9+R_{17}+2R_{13}) \qquad (8)$$

Choosing R_{18}=1.5kΩ, R_{13}=R_{15}=3kΩ, R_5=R_9= R_{17}=2kΩ, C_{20}=1.5nF we obtain an equivalent inductance of L = 27mH. Resulting magnitude-frequency characteristic obtained from SPICE simulations performed for the circuits given in Fig.5 and 6 is illustrated in Fig.7. From Fig.7 it can be easily seen that the inductance simulator constructed with the proposed DDCC+ circuit exhibits a good performance. The tracking error between two curves is determined as %0.017. Furthermore, the large signal behaviour of the filter designed is also investigated by SPICE simulation program applying a 2.8V and 10 kHz sinusoidal voltage to the input. The resulting waveform is given in Fig.8. It is obvious from Fig.8 that the circuit exhibits a good large signal behaviour.

4. Conclusion

This paper introduces an improved CMOS implementation of the DDCC+. It is believed that the proposed CMOS implementation can be useful in the design of current-mode circuits and can be used as a high-performance active element to realise signal processing circuits where differential signals are to be handled.

The proposed circuit has the following advantages:

i) small voltage-tracking errors are obtained using input stages constructed with cross-coupled pairs,

ii) very low x-input resistance is obtained with a negative series -feedback via a class-AB current mirror,

iii) very high z-output impedance and very low current tracking error are achieved by the use of enhanced cascode current mirrors.

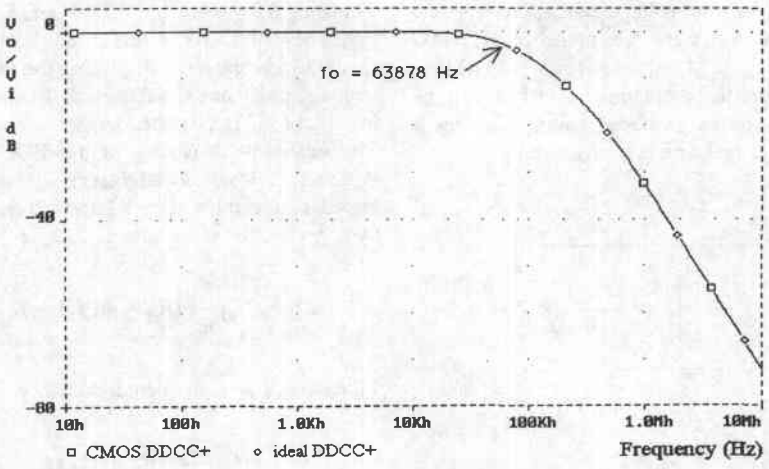

Fig.7. Simulated frequency responses of the passive and active filters

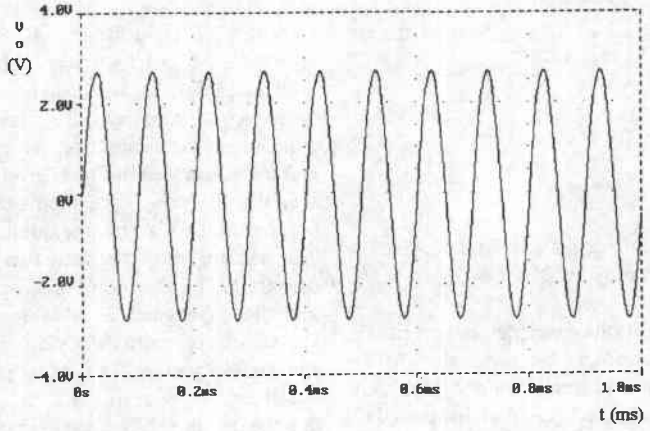

Fig.8. Large signal behaviour of the designed active filter.

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