THREE-PHASE SINUSOIDAL CURRENT AC-DC CONVERTER

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Abstracts

This paper presents the design and evaluation of a three-phase sinusoidal AC to DC buck power converter that draws sinusoidal current waveforms. The implementation of the synchronous PWM makes it possible to obtain sinusoidal line current and regulated with unity; leading and lagging power factor can be achieved by controlling the displacement factor control with low EMI. This complies with the IEC1000-3-2 requirements on harmonic currents. Simulation and experimental results are provided to demonstrate the effectiveness of the converter system.

1.0 Introduction

Three phase diode rectifier have traditionally been the most common tool for AC to DC conversion, primarily because they are cheap, robust and generate a reasonably steady DC output. These power converters when operated from the AC mains may generate current harmonics, which are injected back into the AC system. The problem of the harmonics in low voltage distribution systems is considered very important.

Limits on, EMI are being tightened by standards organizations as they strive for a largely noise-free electrical environment. EN61000-3-2 regulation [1], which is based on IEC61000 part 2, which requires, power converter system should draw a near sinusoidal line current and comply with the limits proposed by the regulation. EN 61000 is an emission standard concerned with low frequency conducted emissions from household goods and similar equipment. Limits are placed on the amplitude of mains harmonic currents up to 40th, e.g., the 3rd harmonic is limited to 2.30A and the 39th. harmonic is limited 0.058A. Even harmonics have generally lower limits.

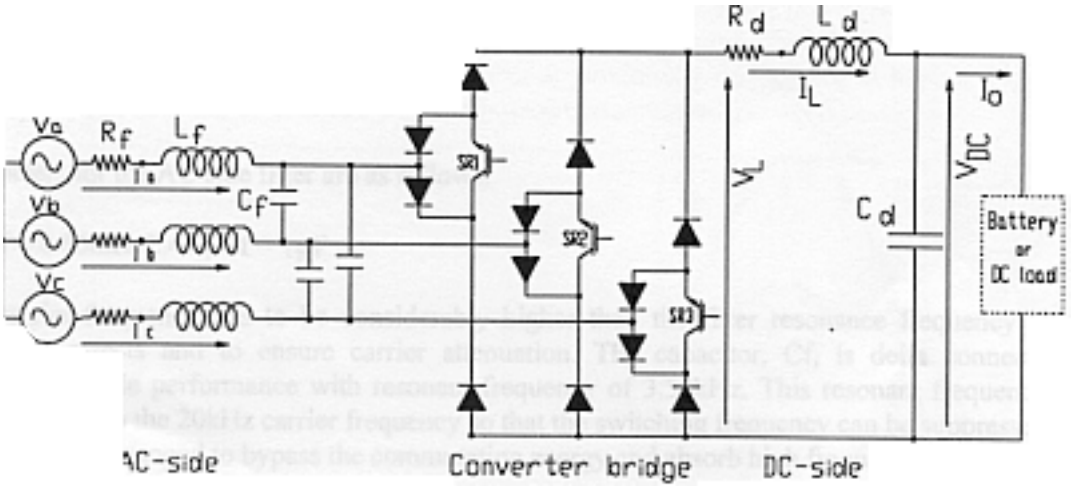
The three-phase AC to DC conversion using diode bridge is one of the circuits most commonly used in industrial application that require an AC to DC conversion. This circuit is simple, robust and cost effective. However, diode bridge rectifiers cause current distortion and conducted EMI and a DC output voltage dependent solely on the amplitude of the input waveform. The large inductance and capacitance can be used to improve the spectrum but it must

pass 50Hz or 60Hz and reject the third, fifth, and seventh and higher harmonics. However this costly and bulky and dissipate resistance to add damping [2].

In this paper, the design and evaluation of a three-phase AC to DC converter which produces an DC output voltage of 0 to 1.5 $\hat{V}_{ph}$ using synchronous PWM. Low EMI can be achieved and comply with IEC regulation with different displacement factor are shown. The application area is for high power and low distortion equipment's.

2.0 Step-down converter

Figure 1 shows the circuit diagram of the power circuit comprising the switched bridge together with the AC and DC side filters [3]. The AC side is connected to the AC mains supply and the DC-side to the DC load.



The voltage produced by the bridge, V_L is low-pass filtered by an L_dC_d combination to provide an output voltage V_{DC}. The converter is operated as a step-down converter where the output voltage can be controlled in the range of 0 to 1.5 $\hat{V}_{ph}$

V_L, averaged over one switching cycle, was given as;

$$V_L = \frac{3}{2} M V_{ph} . \cos\theta$$

Where, M -depth of modulation

$\hat{V}_{ph}$ - peak phase voltage

θ -the phase angle between the phase voltage set and the reference set

V_L is dependent on the phase angle θ and can be controlled within the range of 0 to 1.5 V_{ph} modulation depth, $M\ (0 \leq M \leq 1)$. VDC differs from the average value Of W by the drop across the resistance, Rd, of the link inductor, L_d.

The DC voltage, V_{DC} is less than the bridge voltage by the drop across the resistor, Rd, of the link inductor, L_d. Usually V_{DC} can be approximated by $V_{L(average)}$.

In steady-state, the voltage across the link inductor Ld, averaged over one switching cycle is zero. A constant inductor current IL is set up that equals the output current I, This current is chopped by the switching action into the three phase-currents.

The carrier frequency has to be considerably higher than the filter resonance frequency in order to avoid resonance effects and to ensure carrier attenuation. The capacitor, Cf, is delta connected to give good differential mode performance with resonant frequency of 3.58kHz. This resonant frequency of the AC side filter is less than the 20kHz carrier frequency so that the switching frequency can be suppressed effectively. The capacitors are arranged to bypass the commutating energy and absorb high frequency switching harmonics.

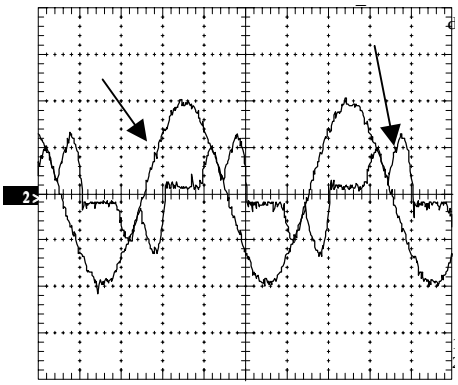
At the DC filter, Ld is used to maintain a near constant current. Filter capacitor Cd acts as voltage source. The link inductor Ld has a gapped-core construction to avoid saturation. The inductor value is chosen with regard to ripple current requirement. The inductor can be relatively small since the ripple frequency will be related to the switching frequency and not the line 50Hz frequency. A large inductance facilitates smooth current but detracts from the transient response of the circuit.

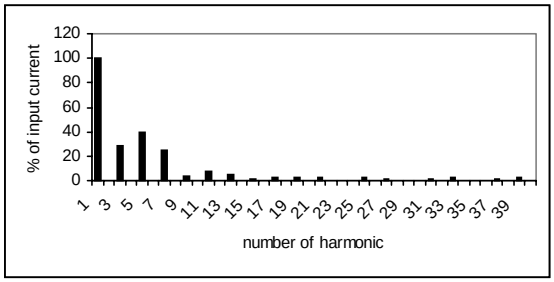
3.0 Synchoronous PWM

The mode of operation of the circuit is similar in that a near constant current in the DC-side inductor is chopped between the phases of the AC connection. The switching of the power controllable devices is modulated by synchronous PWM implemented in an XC-3042 field programmable gate array (FPGA), which offers flexibility in developing designs. Displacement factor control is achieved to give controllable displacement factor of leading or lagging phase angle respectively. The main clock frequency is locked to the mains frequency using a phase locked loop. Both the reference waveform and the switching frequency of 20kHz are locked to the mains frequency and therefore the PWM is synchronous.

4.0 Simulation and Experimental Results

Figure 2 shows the experimental results for a line current of the three-phase diode bridge rectifiers. The ac mains current is harmonically rich. This current waveform is made up of odd-order harmonics which are integer multiples of the fundamental frequency. Figure 3 shows the harmonic spectrum of the three-phase diode bridge input current. The total harmonic distortion for the line current is 56.94%.





A prototype was constructed and tested for the purpose of verifying both simulation and theory. Pspice is used to perform time domain simulation of the rectifier circuit in steady state. The prototype three-phase power converter was tested at powers greater than 1kW. The prototype was tested with different values of modulation index, M, and also with different phase displacements between the input voltages and currents. Circuit performance proved to be satisfactory in all conditions and well in accordance with the simulation results

Figure 4a and b show simulation and experimental results for a line current and voltage unity power factor and M = 0.8. There is a small leading angle due to the AC-side filter. The AC-side current is continuous and contains a low proportion of the switching frequency components. Figure 5a and b illustrate the capability of varying the displacement factor, approximately 30^0 leading at M=0.8. The leading power factor feature can be utilised to compensate other equipment operating with a lagging power factor. Figure 6a and b show the simulated and experimental results with a displacement factor of approximately 40^0 lagging at M=0.8. The converter leading and lagging power factor capabilities with minimised current distortion can be achieved.

4.2 Total Harmonics Distortion

The output of the practical power converter contains certain harmonics and the quality of the converter can be normally evaluated in terms of harmonic factor and total harmonic distortion. The percentage of the n^{th} harmonic factor is a measure of an individual harmonics contribution, and is defined as,

$$\textit{Harmonic factor}_n = \frac{V_n}{V_1} * 100\%$$

Total harmonic distortion is a measure of the distortion caused by the undesirable frequency components in a waveform. It is a measure of closeness in shape between a waveform and its fundamental component, and is defined as,

$$\textit{Total harmonic distortion} = \frac{1}{V_1}\left(\sum_{n=2,3,\ldots}^{\infty} V_n^2\right)^{\frac{1}{2}}$$

Figure 7, 8 and 9 shows the current spectrum for unity, leading and lagging power factor respectively. The total harmonic distortion for the current (THD_i) for unity, leading and lagging power factor are 7.29%, 6.28% and 5.78% respectively compared to main supply voltage total harmonic distortion (THD_v) of 2.29%. The total harmonic distortion due to the power converter for unity, leading and lagging are 6.29%, 5.85% and 5.31% respectively, based on equation below as,

$$THD = \sqrt{THD_i^2 - THD_v^2}$$

5.0 Conclusions

The circuit topology presented enables step-down rectification resulting in a controllable DC output voltage, with predominantly sinusoidal supply currents. Low distortion supply currents were achieved using synchronous PWM to control the switching elements of the bridge. The line current can be sinusoidal regulated with unity, leading and lagging power factor can be achieved by controlling the displacement factor control with low EMI.

6.0 References

[1] BS 5406: Part 2: 1988, EN 60 555-2: 1987; "Disturbances in supply systems caused by household appliances and similar electrical equipment", Part 2, Specification of harmonics.

[2] M. J. Nave, "Power line filter design for switched-mode power supplies", chapter seven, Van Nostrand Reinhold, 1991.

[3] R. ltoh, "Steady-state and transient characteristics of a single-way, step-down PWM GTO voltage source converter with sinusoidal supply currents", IEE Proceedings, Vol. 136, Pt. B, No. 4, pp 168 - 175, 1989

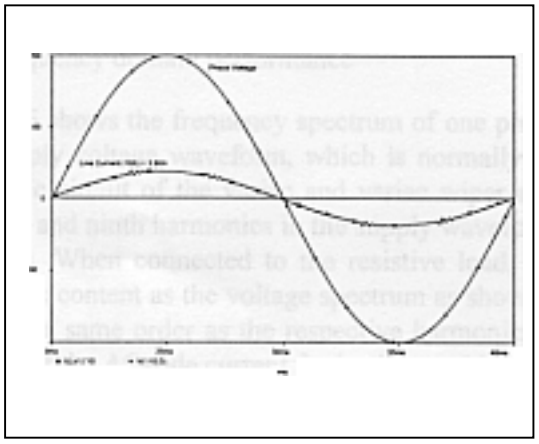


Figure 4a: Sinusoidal i/p voltage & current at unity p.f (AC-DC), M=0.8, (Simulated)

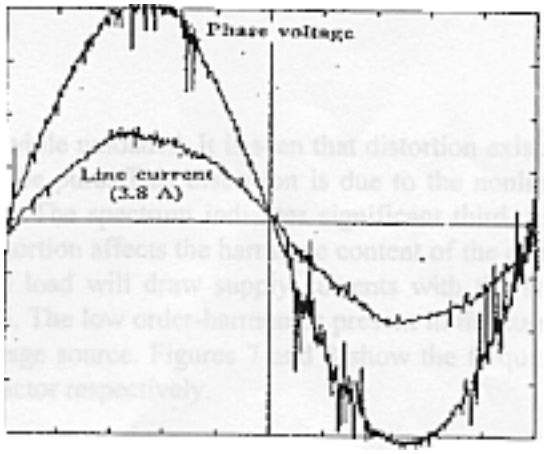


Figure 4b: Sinusoidal i/p voltage unity power factor, M =0.8 (experimental)

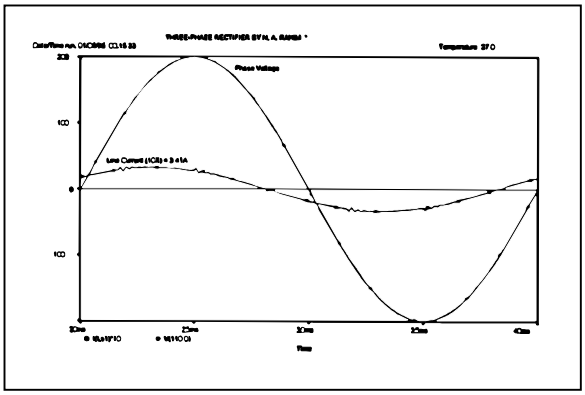


Figure 5a: Sinusoidal input voltage & current at leading p.f (simulated)

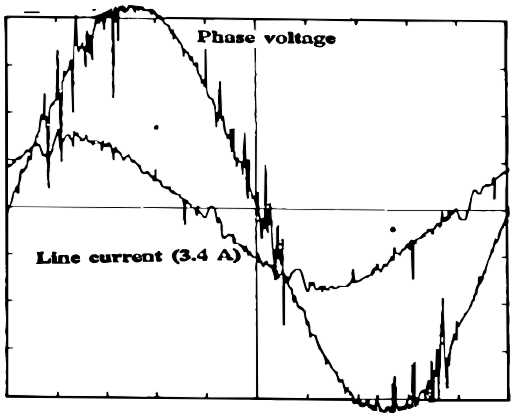


Figure 5b: Sinusoidal i/p voltage and line current at leading power factor, M =0.8 (experimental) SW/div,2Aldiv & 2ms/div

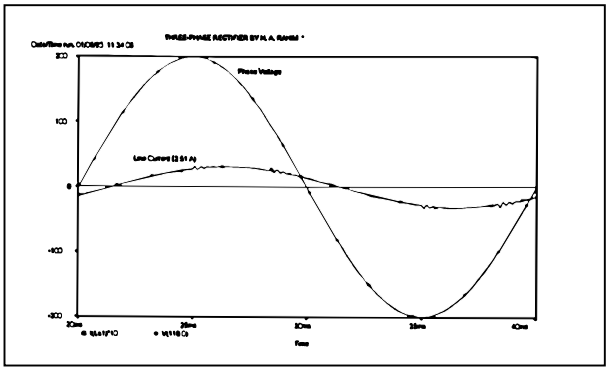


Figure 6a: Sinusoidal input voltage & current at lagging p.f (simulated)

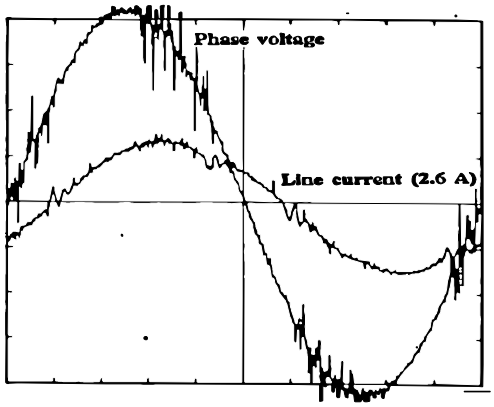


Figure 6b: Sinusoidal i/p voltage and line current at lagging power factor, M =0.8 (experimental)

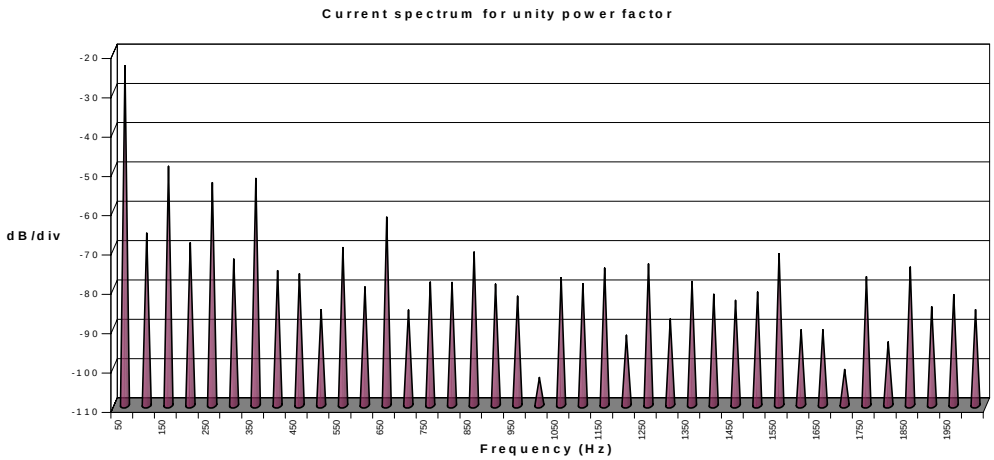


Figure 7: Line current spectrum at unity power factor

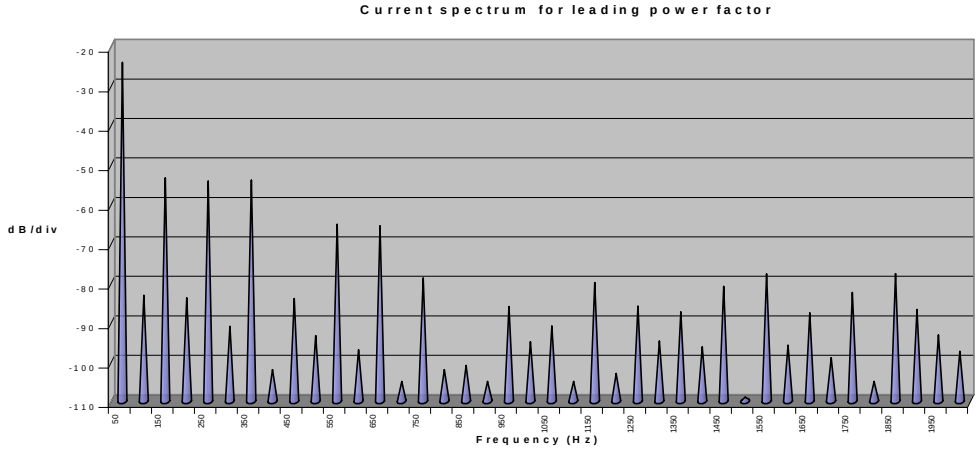


Figure 8: Line current spectrum at leading power factor

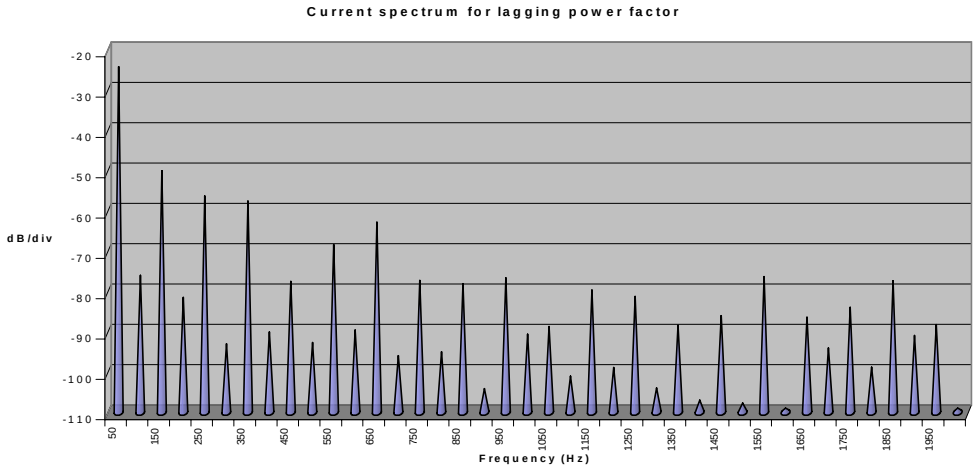


Figure 9: Line current spectrum at lagging power factor