A two-input 8-transistor SRAM cell with enhanced noise immunity

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Abstract

The paper presents 8-transistor SRAM cell with improved noise immunity. The effect is reached by use an additional supply bus. Simulation and experiment have been demonstrated following characteristics SNM = 222 mV, WRM = 1017 mV, Icell = 114 uA. The test chip has been fabricated using UMC 180 nm CMOS technology.

1. Introduction

With a decrease in resolution of CMOS technology a process spread of threshold voltage and carrier mobility grows [1]. So, in digital circuits, including SRAM's, ranges of logic level values are expanded and the guard interval between them diminishes, which deteriorates noise immunity. A SRAM is characterized by the minimal amplitude and duration of control pulses on word lines (WL) and bit lines (BL), where writing and reading are ensured with specified probability of occurrence of non-operative cells from the array. These characteristics are determined by both parameters of the bus and those of the SRAM core. Bus parameters depend mostly on CMOS technology. Core parameters as applied to SRAM are determined by the circuit structure of the cell and include static noise margin (SNM), write margin (WRM), and cell discharge current. SNM is an additional voltage supplied to master nodes of a SRAM trigger in the opposite phases, at which the trigger changes its state to the opposite one. The parameter corresponds to inverter margin offset due to a process spread and noise occurring due to a parasitic connection with the buses. WRM is the voltage in the node of connection to BL, at which the trigger changes its state. The cell discharge current (I_{cell}) is the current flowing to SRAM from BL in the read mode.

In general a SRAM trigger is a negatron built on the basis of a non-linear voltage controlled voltage source (VCVS), with nonzero output impedance loaded on a retrieval switch. The node to which the VCVS switch and the output are connected is a master node for the VCVS. The potential of the master node should be securely in the stable zone in the read mode and in the unstable zone in the write mode. Consider known methods for enhancing noise immunity. Existing circuit designs are divided into groups by the number of transistors. Those are 6, 8, and 10-transistor SRAMs [1]. Logic states of the basic 6-transistor circuit are changed by the potential of the input node to which the master node is connected through the retrieval switch impedance. In the read mode the potential increases in the master node corresponding to the inverter low-level output, which may lead to the unstable zone. In order to increase SNM, the width ratio of n-channel inverter transistors in the trigger to the retrieval switch transistors should be increased. In order to increase WRM, the width ratio of the load p-channel transistor to the retrieval switch transistor should be decreased. As a result, to achieve required SNM and WRM values, the circuit area grows. In [2] the method of changing the control voltage for retrieval switches to increase noise immunity is presented. This method is based on reducing voltage on an active WL in the read mode and supplying the nominal voltage in the write mode. As a result, in the read mode the conductivity of retrieval switch transistors in reduced and SNM increased, and in the write mode WRM is increased. The drawback is sensitivity of the enumerated parameters to the spread of the transistor threshold voltages. Another way to increase noise immunity is based on controlling supply voltage of the trigger [2]. The width of the retrieval transistor is specified similarly to the previous case. In the write mode the trigger supply voltage is understated, which reduces conductivity of the open p-channel transistor in the trigger and increases WRM. The drawback is two power sources. To increase noise immunity, also negative voltage on BL in the write mode [2] is used, the width of retrieval transistors being specified lower than in the previous case, which increases SNM. To compensate for reduction in WRM, the zero logic level on BL is selected as a negative voltage. However, cross noise and power consumption (P_{cons}) increases.

The use of an external discharge circuit maximizes SNM due to a reduced load of the trigger inverters [3]. A discharge transistor connected in series to an additional retrieval transistor which has been connected to an additional reading BL. The gate of the discharge transistor is linked to the trigger output. Such solution allows the required read current to be secured without reducing SNM, but requires an additional pair of transistors and buses. The methodology of controlling the access duration is given in [4]. In the read mode retrieval switches are opened during a shorter time than in the write mode. As a result the varied voltage on the VCVS master node in the read mode becomes lower than in the write mode therefore SNM increases. The drawback of this approach is necessity of a controlled pulse generator.

So, the existing solutions complicate circuitry of SRAMs that, consequently, increase the area of the die of the memory cell [3] and, in a number of cases, power consumption [2]. The purpose of this work is to develop a SRAM circuit with enhanced noise immunity and decreased power consumption. The SRAM does not require the die area to be increased and the peripheral circuits complicated. The paper is prepared as follows. The second section presents the developed memory cell, the third section gives the methodology of computer modeling, and the last section reviews the experiment methodology and compares the design and experimental data.

2. A memory cell with enhanced noise immunity

To enhance noise immunity an additional supply bus is connected to the cell trigger. The bus potential is higher than the potential of the core common bus. It was demonstrated in [5] that the additional supply bus can decries the "read-write" time of the memory cell. Our proposal is to use the additional supply bus to optimize SNM and WRM of the cell. The suggested solution reduces conductivity of retrieval switches therefore SNM increases. Besides write margin of trigger inverters increases also. It causes WRM of the cell to grow. The area and P_{cons} of the cell with the additional bus is unchanged. To reduce P_{cons}, the method of two-coordinate retrieval [6] is used. The SRAM is activated both by lines and columns, unlike a one-coordinate retrieval where the potential in all BL pairs is changed by a WL signal. It allows the potential to be changed only in BL pairs transmitting information to a data bus.

The suggested circuit is given in Fig. 1. The trigger is built on two CMOS inverters formed by transistors T4-T7. To master nodes of inverters retrieval switches realized on transistors T3 and T8 are connected. The logic element «AND» consists of transistors T1 and T2, gates of them are connected to column select lines CL+ and CL–. Pairwise inverse control signals are supplied to the lines. The drain of the transistor T1 is connected to the address bus WL. The proposed cell was calculated and optimized using parameters of UMC 180 nm CMOS technology. As a result, following transistor sizes are obtained. The length of transistor channels is 180 nm; widths of n-channel transistors in the trigger are 450 nm, p-channel ones are 250 nm. Widths of n-channel transistors in the logic element are 350 nm.

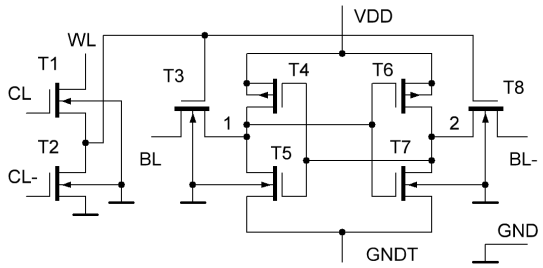

Fig. 1. Circuit of the proposed memory cell

3. Memory cell simulation

The method of a SRAM circuit quasi-static modeling based on linearly varying voltage sources with slew rate much slower than slew rate of the node potentials upon switching the circuit is used [7]. The source voltage upon changing the state corresponds to the parameter being measured. A circuit for SNM simulation is given in Fig. 2. BSIM3 models are used for transistor modeling. Linearly varied voltage sources V3 and V4 serve to imitate noise signals and have following parameters. The minimal and maximal voltages are 0.0 V and 1.0 V, and rise time is 30 ns. Sources V1 and V5 serve to generate the supply voltage 1.8 V and the voltage of the additional supply bus of the trigger. Source V2 serves for initial setup. When node potentials CL– and CL+ are equal the noise signal voltage is determined as SNM. WRM measuring differs from the discussed SNM one in that the noise signal is missing, but the BL potential changes using source V2 (Fig. 3). The drain voltage of transistor T3 on switching the trigger corresponds to WRM value. Simulation of I_{cell} in the read mode is effected by a direct current using a circuit with disconnected feedback (Fig. 4). The test source current at the BL voltage pre-charge corresponds to I_{cell} parameter. The temperature corresponds to 27°C. Simulation was performed under the potential of the trigger additional supply bus GNDT (Fig. 1) varying from 0.0 V to 0.7 V.

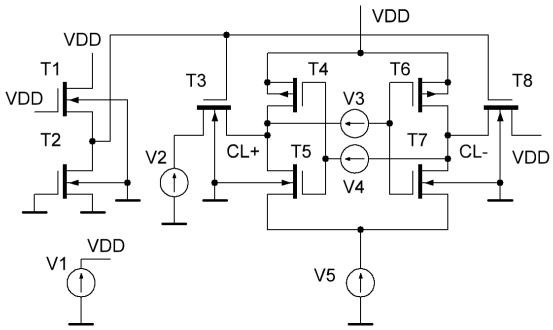

Fig. 2. Circuit for SNM simulation and measuring

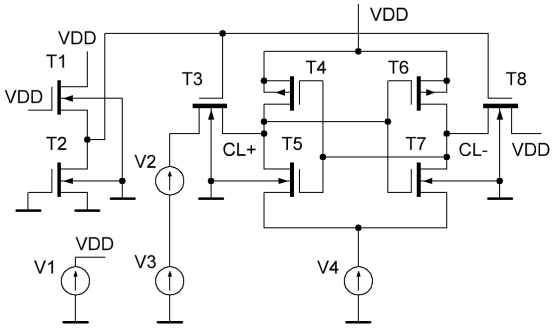

Fig. 3. Circuit for WRM simulation and measuring

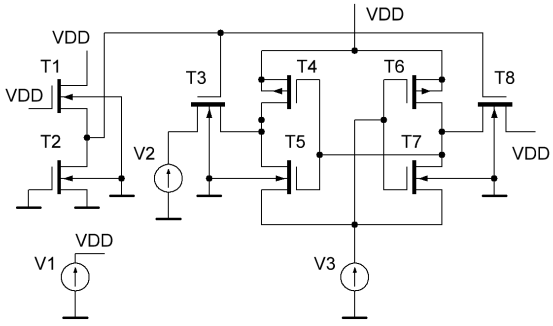

Fig. 4. Circuit for discharge current simulation and measuring

4. Experiment and measurement of the circuit parameters

A test SRAM chip with a disrupted feedback loop has been designed. The test circuit is given in Fig. 5. The inputs of the inverters IPC and PC are disconnected from the master nodes and led to separate pads to pass an additive noise signal. The master nodes of the trigger are OUT1 and OUT2. Dies were fabricated by Europractice using UMC 180 nm CMOS technology. The die is 8.0 um per 5.2 um and includes a 33*33 test core, bus drivers, and a source buffer. The die microphotography is shown in Fig. 6.

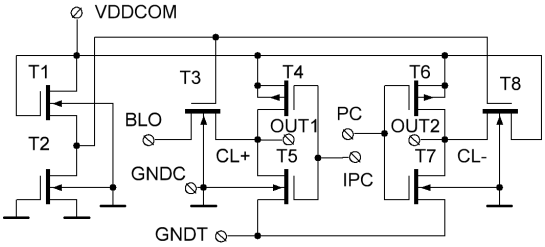

Fig. 5. Circuit for quasi-static measurements

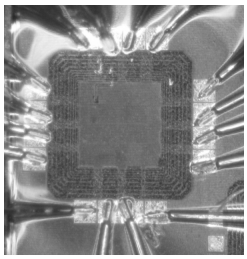

Fig. 6. Die microphotography

For measuring the sources of linearly varied voltage are substituted by voltage summators with high input and low output impedances. The output voltage is the sum of the input voltage and the offset voltage specified manually. Noise signal summators and controlled constant voltage sources are implemented on operational amplifiers (OpA) on a test board (Fig. 7). On DA1 and DA2 OpAs voltage sources are implemented with low output resistance imitating BL (BLO terminal) and the supply bus of the trigger (GNDT terminal) respectively. The respective voltages are specified by potentiometers R1 and R2. Microammeter PA1 measures I_{cell}. On DA3 and DA4 OpAs the sources +1.8 V and –1.8 V are implemented. Voltage +1.8 V is supplied also to the power bus VDDCOM. On DA5 and DA8 OpAs voltage buffers with high input resistance isolating the master nodes from the noise signal summators are implemented. The noise signal summators are based on DA6 and DA9 OpAs, the noise signal being supplied with the opposite polarity from the buffer based on DA7 OpA and the voltage inverter based on DA10 OpA. The corresponding SNM is specified using R3 potentiometer. Switches S1 and S2 serve to preset the trigger. For each parameter a series of measurements is carried out with voltages on the supply bus of the trigger varying from 0.0 V to 0.7 V with the step 0.1 V. The results are shown jointly with the simulation results in Fig. 8–10 (AVE index denotes the averaged experimental values, SIM is for the simulation results).

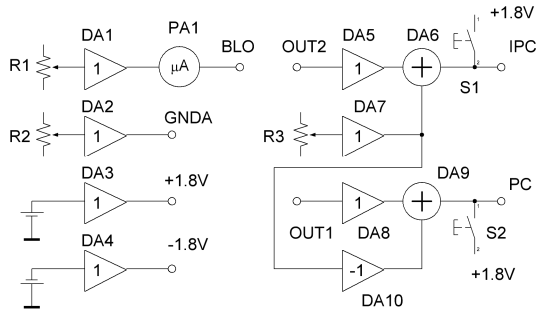

Fig. 7. Circuit of the test board

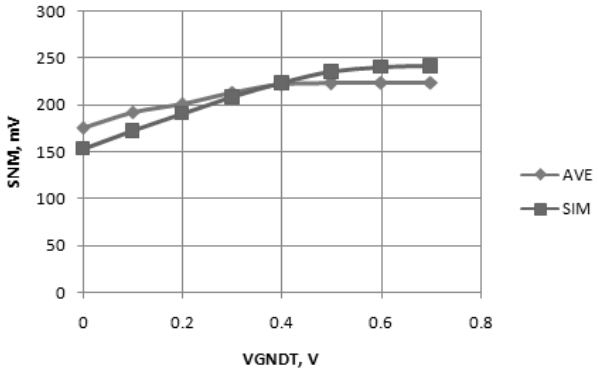

Fig. 8. Dependency of SNM on the potential of the supply bus of the trigger

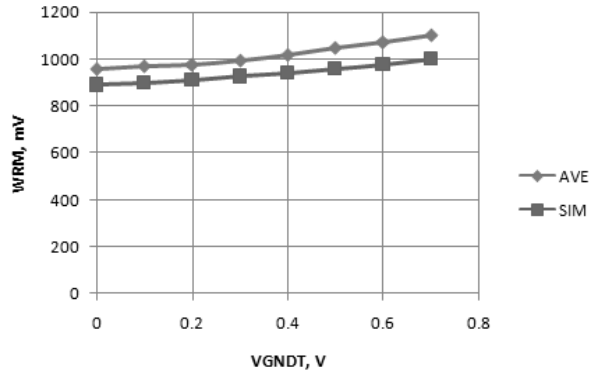

Fig. 9. Dependency of WRM on the potential of the supply bus of the trigger

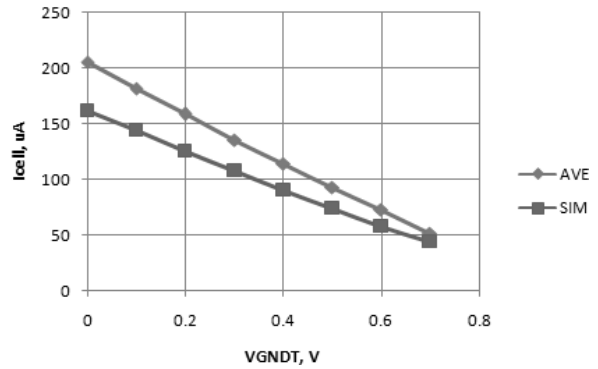

Fig. 10. Dependency of I_{cell} on the potential of the supply bus of the trigger

As it is seen from Fig. 8–10, it is appropriate to increase the potential of the trigger additional supply bus to 0.4 V, the further increase does not result in any improvement. SNM is increased by 26% to 222 mV, WRM by 6% to 1017 mV compared to the standard 6-transistor circuit. The discharge current is decreased two times from 205 uA to 114 uA, which doubles data delay through the data bus. In high-capacity memory this does not lead, however, to a considerable increase of response time due to high delays in the address bus and peripheral circuits. Divergences between the results of the experiment and the simulation did not exceed: 11% for WRM, 16% for SNM, 27% for I_{cell}.

5. Conclusions

This paper proposes the SRAM cell with two address inputs and enhanced noise immunity. The technical solution has been illustrated using 180 nm CMOS technology. Table 1 presents comparative results for memory cells with close process parameters. SNM of the suggested circuit is second to known results, but the cell is essentially simpler and, consequently, occupies less die square. The additional trigger bus does not increase P_{cons}.

Table 1. Comparison to existing solutions

Work	Process	SNM, mV	Advantages	Disadvantages
This work	180 nm	222	- reduced P_{cons} up to 3 times; - small size; - high WRM; - simple supply circuit.	- decreasing of I_{cell} in 2 times.
[8]	180 nm	220	- small size; - simple control circuit.	- decreasing of WRM; - high P_{cons}.
[9]	130 nm	270	- high speed; - high I_{cell}.	- complicity of control circuits; - large size; - high P_{cons}.
[10]	130 nm	200	- small size; - high WRM; - low P_{cons}.	- complicity of control circuits; - decreased speed.

7. References

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