Enhancement of Extracted Maximum Power from Partially Shaded Multi-string PV Panels Using a New Cascaded High Step-Up DC-DC-AC Converter

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Abstract

Partially shaded problem in multi-string PV panels is a major challenge because it reduces the value of generated power from PV panel. In this paper, a new cascaded high step-up DC-DC-AC converter based on SEPIC converter is proposed for partially shaded multi-string PV panels. To solve the challenge of partially shaded in PV system, a SEPIC dc-dc converter is connected for each string and the duty cycle of the each SEPIC converter is controlled to extract maximum power from each string using Perturb and Observe (P&O) algorithm. It increases the total extracted power from PV panel substantially. The proposed DC-AC converter can generate a large number of levels at output to reduce total harmonic distortion. This converter uses the least number of components such as IGBTs, drivers, capacitors and anti-parallel diodes which is an important advantage. Simulation results based on PSCAD/EMTDC software are verified the operation of presented structure.

1. Introduction

Photovoltaic system is an important source because it is a maintenance-free, low cost, clean, safe, and abundant resource of nature. However, Partial shading is a big challenge in PV systems which occur due to the shadows of buildings, trees and clouds. The intensity of solar illumination on shaded strings is lower than unshaded strings which lead to the reduction in power generation from these strings [1, 2]. To extract maximum power from a shaded PV panels, several algorithms and power electronic converters have been proposed recently. Fig. 1 indicates the general structure of PV systems which consists of a DC-DC converter to increase the value of generated voltage by PV and a DC-AC converter to deliver the power to the load [3, 4]. As shown in this figure, the whole PV panel is connected only one DC-DC converter to increase the level of generated voltage by PV. This is a traditional structure of a PV panel. In partially shaded condition of a PV panel, only some strings are under shading, not all strings. Then, obtaining a way to extract maximum power from shaded strings is a challeng which researches have been tried to solve this problem using several maximum power point algorithms and DC-DC-AC converters.

For DC-DC converter, High step-up converters such as boost, interleaved, cuk, SEPIC, quadratic, Z-source converter, and switched-capacitor converters have been recommended. Each one of these structures has some advantages and disadvantages. For instance, the voltage gain of boost converter is low and voltage rating of semiconductors is high [5-7].

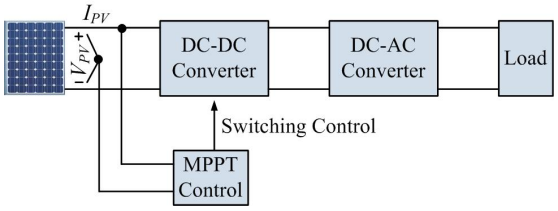


Fig. 1. The general structure of PV systems.

For DC-AC converter, the structures of N-level converter have been presented which are named multilevel converters. For this section, the structure of flying capacitor, diode clamed and cascade H-bridge topologies were used as a multilevel converter. However, these topologies use a large number of components and imbalance voltage of the capacitors of flying capacitor and diode clamed converters is a big challenge [8-11].

In this paper, a new structure of DC-DC-AC converter based on SEPIC converter is proposed for partially shaded multi-string PV panel. The proposed topology increases the value of extracted power from PV panel significantly. The number of used power electronic components in the structure of DC-AC converter is low. Also, inherent voltage balancing of the input capacitors of proposed multilevel converter are another important advantage of presented topology.

2. PV Panel modeling under partially shaded conditions and P&O algorithm.

Equivalent circuit model of a PV string is indicated in fig. 2 (a). In this model, I_{Sc} is the generated current of a PV string and R_S and R_P are the series and parallel resistances of a string. Also, equivalent circuit model of multiple strings are shown in fig. 2(b). In this figure, bypass diode is considered for each string. To obtain the V-I characteristic of a PV, below equation is used:

$$I = I_{sc} - I_o\left(e^{\frac{q(v+R_S I)}{kT}} - 1\right) - \left(\frac{v + R_S I}{R_p}\right) \quad (1)$$

Where T, q, k and I_0 are the temperature (K), the electron charge (C), $q=1.602\times10^{-19}$ (C), Boltzmann's constant ($k=1.381\times10^{-23}$ (J/K)) and the reverse saturation current (A), respectively. In a PV panel, the generated maximum power is the point that the product ($V\times I$) is maximum which is called maximum power point (MPP). It is obvious that the irradiation and temperature are two important factors in the value of generated electricity by a PV panel which affect the point of generated maximum power.

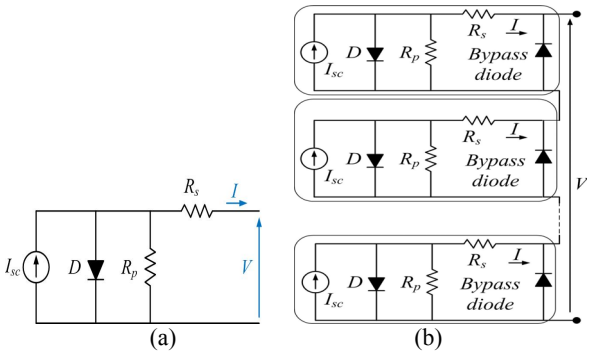


Fig. 2. Equivalent circuit model of (a) a PV string model, (b) multiple PV strings model.

To extract maximum power of PV panel and tracking this point, duty cycle of DC-DC converter (D) is a control parameter. Several algorithms have been presented for tracking MPP such as Perturb and Observe (P&O) algorithm, Incremental Conductance (InCond), Constant Voltage Method. P&O algorithm is the simplest algorithm in comparison with other algorithms due to easy feedback arrangement, little measured parameters and low computational power. The operating voltage is sampled and the P&O algorithm changes the operating voltage towards the MPP by periodically increasing or decreasing the PV system voltage. The block diagram of P&O algorithm is shown in Fig. 3.

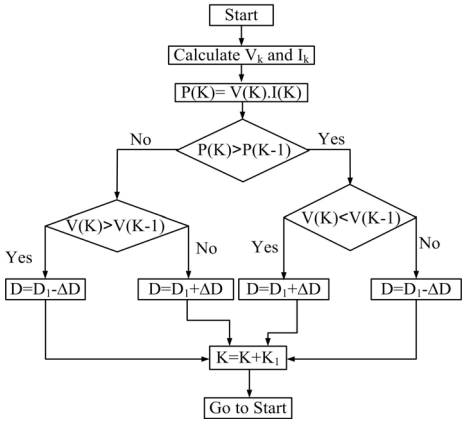


Fig. 3: P&O algorithm to track MPP.

3. Proposed Cascaded High Step-Up DC-DC-AC Converter Topology.

Fig. 4 indicates the structure of SEPIC converter. This topology can acts as a buck and boost converter by controlling duty cycle. The value of output voltage of SEPIC converter is:

$$V_o = \frac{D}{1-D} V_{in} \tag{1}$$

Where D is duty cycle of the switch *S*. Considering the structure of SEPIC converter, the proposed basic unit topology of DC-DC-AC converter is indicated in fig. 5.

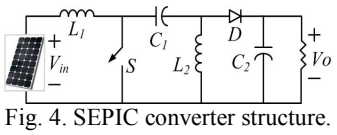


Fig. 4. SEPIC converter structure.

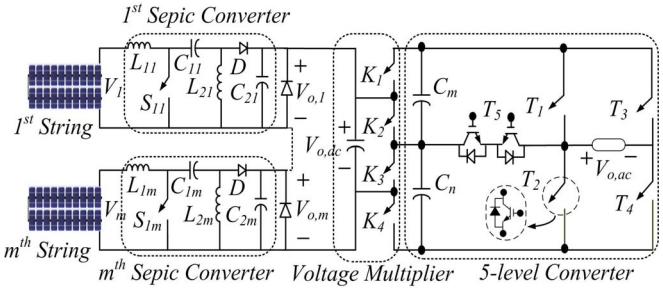


Fig. 5. Proposed basic unit structure for high step-up DC-DC-AC converter.

As shown in this figure, the presented topology consists of *m* PV strings, *m* SEPIC converters, a voltage multiplier and a 5-level converter. Considering partially shaded condition of PV panel, it is clear that the generated voltage by partially shaded strings will be different from unshaded strings due to the difference of irradiation. In fact, the values of $V_1, \ldots, V_m$ will be non-equal. Then, a SEPIC converter is used for each string to increase the value of generated power of each string and apply MPPT algorithm for each SEPIC topology to obtain maximum power from each string. The value of generated voltage by all strings ($V_{o,dc}$) will be:

$$V_{o,dc} = \frac{D_1}{1-D_1} V_1 + \ldots + \frac{D_m}{1-D_m} V_m \tag{2}$$

D_1 and D_m are the duty cycle of the first and m^{th} SEPIC converter, respectively. The main challenge in the structure of DC-DC-AC converters for PV systems is the voltage balancing of the input capacitors of DC-AC converter. These capacitors are shown by C_m and C_n in fig. 6. To solve this problem, a voltage multiplier converter is used to balance the voltage of each input capacitor. Based on this figure, it is clear that when the switches K_1 and K_3 are turned ON, the voltage of upper input capacitor (C_m) will be $V_{o,dc}$. Also, when the power switches of K_2 and K_4 are turned ON, the voltage of lower input capacitor (C_n) will be $V_{o,dc}$. Then, the input voltage of 5-level converter is increased to $2V_{o,dc}$. Table 1 indicates the switching states of proposed 5-level converter to generate the levels of 0, $+V_{o,dc}$, $-V_{o,dc}$, $+2V_{o,dc}$, $-2V_{o,dc}$ at output ($V_{o,ac}$).

Table 1. The switching states of proposed 5-level converter.

NO.	Switches					$V_{o,ac}$
	T_1	T_2	T_3	T_4	T_5	
1	ON	OFF	ON	OFF	OFF	0
2	OFF	OFF	OFF	ON	ON	$V_{o,dc}$
3	OFF	OFF	ON	OFF	ON	$-V_{o,dc}$
4	ON	OFF	OFF	ON	OFF	$2V_{o,dc}$
5	OFF	ON	ON	OFF	OFF	$-2V_{o,dc}$

It is clear that the value of total harmonic distortion of presented 5-level converter is high. Then, its power quality will be poor. Moreover, the switches T_1, T_2, T_3, T_4 should withstand high voltage equal to $2V_{o,dc}$. In fact, the voltage rating of these switches is high. Then, this topology cannot be used in high voltage application. Hence, to solve these two problems, the proposed basic unit topology can be extended as indicated in fig. 6. As shown in this figure, the presented multilevel converter is based on cascaded connection of 5-level converters. The number of IGBTs (N_{IGBT}) , drivers (N_{driver}) and input capacitors ($N_{capacitor}$) are obtained by (3-5), respectively:

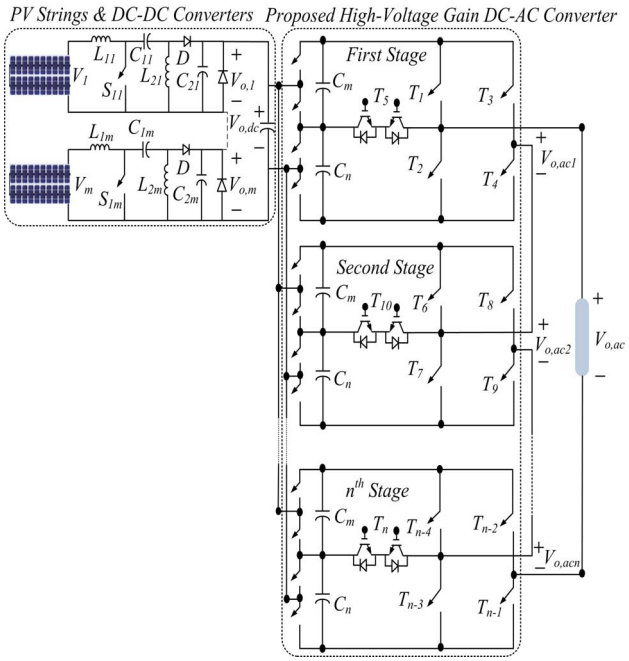


Fig. 6. The general structure of proposed cascaded high step-up DC-DC-AC converter.

$$N_{IGBT} = 6n \tag{3}$$

$$N_{driver} = 5n \tag{4}$$

$$N_{capacitor} = 2n \tag{5}$$

Where n is the number of stages or 5-level converters. The number of generated levels at output voltage will be:

$$N_{level} = 4n + 1 \tag{6}$$

Substituting (3-5) in (6), the relations among the number of levels with N_{IGBT}, N_{driver} and $N_{capacitor}$ are, respectively:

$$N_{IGBT} = 1.5(N_{level} - 1) \tag{7}$$

$$N_{driver} = 1.25(N_{level} - 1) \tag{8}$$

$$N_{capacitor} = N_{level} - 1 \tag{9}$$

Also, the voltage gain of the proposed topology is:

$$V_{gain} = 2n\left(\frac{D_1}{1-D_1}.V_1 + \ldots + \frac{D_n}{1-D_n}.V_n\right) \tag{10}$$

The comparison results among diode-clamed (DC), flying capacitor (FC), cascade H-bridge (CHB) and suggested multilevel converter in terms of the number of components for an N-level (N_l) output voltage is listed in Table 2. IGBTs and drivers are most important Part in multilevel converters which increase the cost and control complexity and tend to reduce the overall reliability and efficiency. This table shows that recommended multilevel converter needs minimum number of IGBTs and drivers in comparison with other topologies. Also, it is clear that the proposed topology needs minimum number of DC bus capacitor.

It is noticeable that the proposed topology (fig. 6) can be designed as a traditional type which is indicated in fig. 7. This topology consists of only one SEPIC converter to track MPP. This leads to decrease the value of generated power from panel.

Table 2. Comparison results of multilevel converters.

Devices	Topology			
	DCC	FCC	CHBC	Proposed
Diode	$(N_l\text{-}1)(N_l\text{-}2)$	0	0	0
Capacitor	0	$(N_l\text{-}1)(N_l\text{-}2)/2$	0	0
IGBT	$2(N_l\text{-}1)$	$2(N_l\text{-}1)$	$2(N_l\text{-}1)$	$1.5(N_l\text{-}1)$
Driver	$2(N_l\text{-}1)$	$2(N_l\text{-}1)$	$2(N_l\text{-}1)$	$1.25(N_l\text{-}1)$
DC Bus Capacitor	$(N_l\text{-}1)$	$(N_l\text{-}1)$	$0.5(N_l\text{-}1)$	$0.5(N_l\text{-}1)$

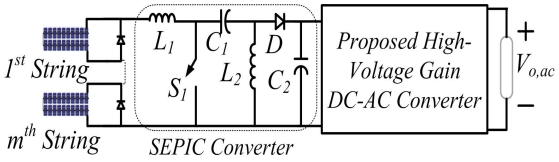


Fig. 7. Traditional type of proposed high step-up DC-DC-AC converter topology.

4. Switching control strategy

In the proposed topology, there are two kinds of switches. The first kind is related to the switches of SEPIC converters which are shown with S_{11}, S_{12}, …, and S_{1m}, respectively. These switches are controlled to track the maximum power point which their switching pattern is shown in fig. 8 (a). Based on this figure, it is clear that each switch of SEPIC converter is individually controlled using P&O algorithm to extract maximum power from each string. Also, the control method of the switch S_1 in the proposed traditional type (fig. 7) is shown in fig. 8 (b).

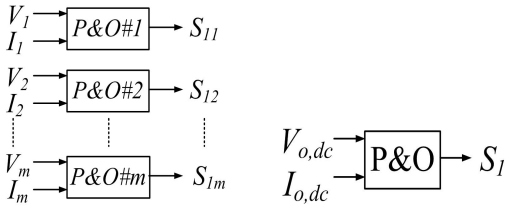


Fig. 8. Control method of the switches of SEPIC converters.

Several modulation strategies for multilevel converter can be used such as fundamental frequency switching, space vector method, multicarrier PWM method and so on. The widely used multi-carrier PWM methods are known as Phase Shifted (PS), Phase Disposition (PD), Phase Opposition Disposition (POD), and so on. These methods use a large number of carriers to control of the switches which leads to control complexity [12-15]. In fact, these techniques employ (m-1) carriers for an m-level waveform. In this paper, another new multi-carrier PWM method is used. In this method, the carries are saw tooth and rectified sine carrier waveforms. Based on this method, only one saw tooth wave used and is compared with (m-1)/2 rectified sine carrier waveforms for a m-level converter. For instance, these carrier for a 5-level converter is shown in fig. 9.

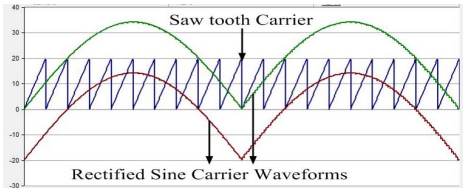


Fig. 9. New multi-carrier PWM method for a 5-level converter.

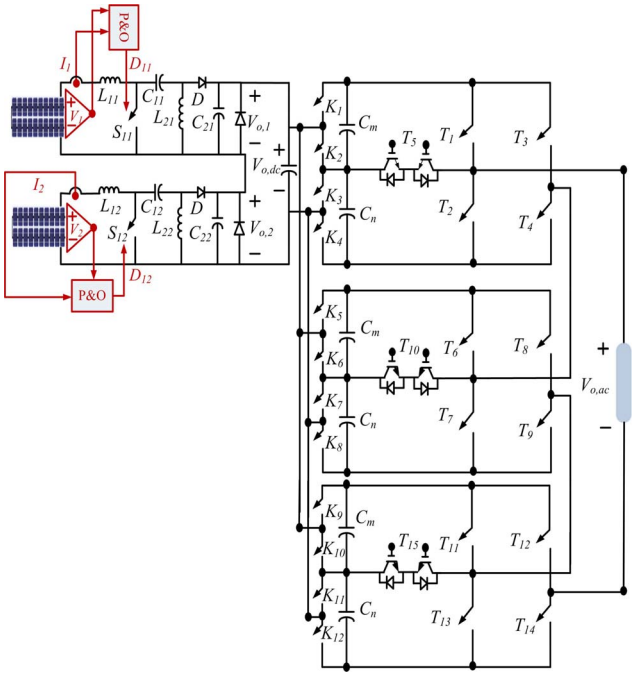
The saw tooth carrier is defined with the same frequency (F_{saw}). The frequency of the rectified sine carrier waveforms is denoted as F_{sin},. In multilevel converters, the frequency ratio (M_f) is given by (11):

$$M_f = \frac{F_{saw}}{F_{\sin e}} \tag{11}$$

The switching functions of proposed converter are then given by the use of logical AND, OR, NOT gates.

5. Simulation results

Fig. 10 (a) indicates the proposed cascaded topology which consists of two strings and three stages. As shown in this figure, the switches S_{11} and S_{12} are separately controlled using individual P&O algorithms to extract maximum power from each string. For the same number of stages, the traditional type of proposed topology is indicated in fig. 10(b). The irradiations levels of the first and second strings are assumed to be 500 W/m^2 and 1500 W/m^2, respectively. The magnitudes of used elements are listed in table 3.



(a)

(b)

Fig. 10. The simulated topologies, (a) cascaded topology, (b) traditional type of presented topology.

Table 3. Magnitudes of elements of proposed topology.

L_{11}= L_{12}	20mH	C_{11}=C_{12}	39.37μF
C_m= C_n	1000μF	R_{Load}	50Ω
L_{Load}	40mH	Temprature	40 °□

Fig. 11 shows the used carriers for a 13- level PWM using proposed technique with $M_f = 24$ and carrier frequency 1200 Hz to control the switches of K_1,K_2, ..., K_8, T_1, T_2, ..., T_8.

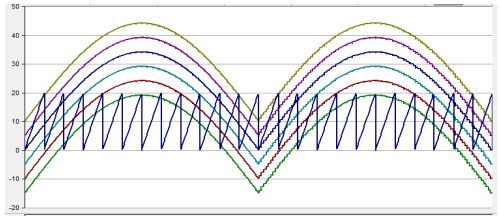


Fig. 11. The carriers for a 13- level converter.

Fig. 12 indicates the P_{pv}-V_{pv} characteristics of the PV of proposed cascaded and traditional type. Based on this figure, it is clear that the maximum power that can be extracted from PV strings are 315W and 480W in proposed cascaded and traditional type, respectively.

Fig. 13 (a) shows the extracted power and voltage from traditional type of presented topology which is 315W and 110V, respectively. Also, Fig. 13 (b) indicates the extracted power and voltage from presented cascade topology which are 480W and 81V, respectively. These values are in full agreement with the P_{pv}-V_{pv} characteristics of traditional type and cascaded topologies (See Fig. 12). Comparing these values, it is clear that the value of extracted power and voltage from proposed cascade topology is much more than the values of traditional type of presented structure which it is an important advantage.

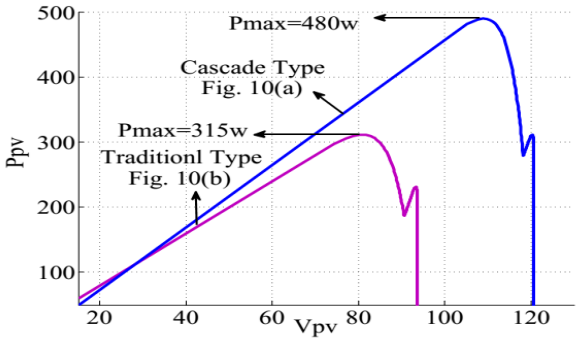
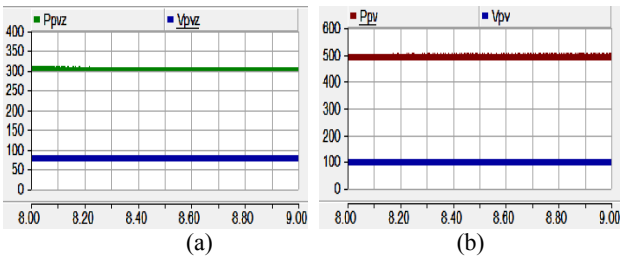


Fig. 12. P_{pv}-V_{pv} characteristics of the PV of proposed cascaded and traditional type.



(a) (b)

Fig. 13. Extracted power and voltage from (a) proposed traditional type, (b) proposed cascaded.

Fig. 14 indicates the voltage waveform of balancing capacitor which its value is 102V (V_{Cm}=V_{Cn}=100V). The output voltage and current waveforms of proposed cascade structure are shown in Fig. 15 (a) and (b), respectively. it is clear that thirteen levels has been produced at output voltage waveform. Based on the output current waveform, it is clear that the load current is

almost sinusoidal. Because, the R-L load of the proposed converter (R-L) behaves as a low-pass filter for the current. İt is clear that maximum value of output voltage is 600V. İn fact, the used voltage multipliers have been increased the level of generated voltage by PV (100V) substantially.

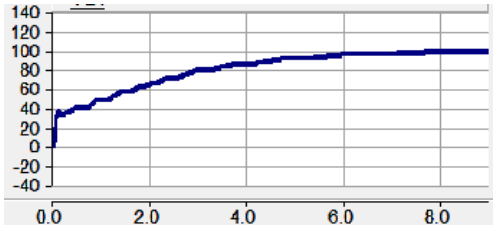
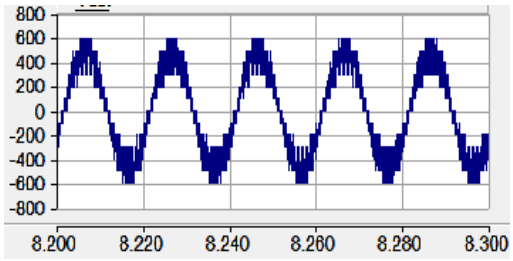
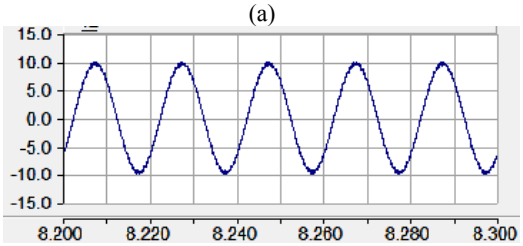


Fig. 14. Voltage waveform of balancing capacitor (V_{Cm}=V_{Cn}).



(a)



(b)

Fig. 15. (a) output voltage, (b) output current waveforms of proposed cascade structure.

6. Conclusions

In this paper, a new cascaded high step-up DC-DC-AC converter is presented for partially shaded multi-string PV panel. Based on the proposed topology, each string was connected to a SEPIC converter for applying MPPT. It was shown that this scheme causes to extract maximum power from each string using Perturb and Observe (P&O) algorithm. The proposed DC-AC converter could generate a large number of levels at output voltage waveform to reduce total harmonic distortion. Also, the proposed DC-AC converter has been utilized minimum number of IGBTs, drivers, capacitors and anti-parallel diodes in comparison with traditional DC-AC converters. Moreover, the voltage gain of proposed structure has been increased using voltage multiplier converters. Also, inherent voltage balancing of the input capacitors i proposed multilevel converter was another important advantage of presented topology.

7. References

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