

DXCCII-BASED FOUR-QUADRANT ANALOG MULTIPLIERS USING TRIODE MOSFETS

Ali Zeki * Ali Ümit Keskin † Ali Toker *

e-mail: alizeki@ehb.itu.edu.tr e-mail: auk@e-kolay.net e-mail: alitoker@ehb.itu.edu.tr

* Istanbul Technical University, Faculty of Electrical and Electronics Engineering, Department of Electronics & Communications Engineering, 34469, Maslak, Istanbul, Turkey

† Yeditepe University, Faculty of Engineering & Architecture, Department of Electrical Engineering, 34755, Kayışdağı, Istanbul, Turkey

Key words: Analog multipliers, current conveyors, DXCCII

ABSTRACT

In this work, two four-quadrant analog multipliers are proposed based on a recently presented active device, the dual-X current conveyor (DXCCII) and triode MOSFETs. The performance of each presented analog multiplier is obtained via SPICE simulations to show the functionality of the proposed multipliers. A CMOS implementation of DXCCII is used in simulations.

I. INTRODUCTION

Analog multipliers are among the most important building blocks for analog signal processing. They are used widely in modulators, mixers, adaptive filters, neural networks, etc [1]. Therefore, design of high-performance integrated analog multipliers has received much interest [2-7].

It was revealed recently that, a new active device, the dual-X second generation current conveyor (DXCCII), brings versatility to design of continuous-time tunable filters [8,9]. Figure 1(a) shows the symbol of DXCCII, whose defining equations are as follows:

$$I_Y=0, \quad V_{Xp}=V_Y, \quad V_{Xn}=-V_Y, \quad I_{Zp}=I_{Xp}, \quad I_{Zn}=I_{Xn} \quad (1)$$

Figure 1(b) shows a DXCCII-based voltage-mode tunable lossless integrator [8]. Tuning is performed by adjusting the gate voltage (V_C) of the MOSFET which is operating in triode region. Thanks to the DXCCII, which supplies $V_{Xp}=V_Y$ and $V_{Xn}=-V_Y$, the drain-source voltage of the triode MOSFET is fully differential. This enhances the linearity of this tunable MOSFET resistor, thus, sufficiently linear filtering is possible, besides tunability.

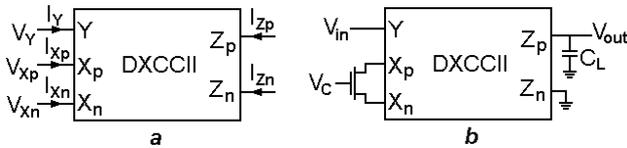


Figure 1. (a) DXCCII symbol, (b) DXCCII-based tunable lossless integrator.

In this study, two DXCCII-based four-quadrant analog multipliers are proposed. The two inputs of the multiplier are applied to the Y terminal(s) of the DXCCII(s) and gate terminal(s) of the triode MOSFET(s).

II. THE FIRST FOUR-QUADRANT MULTIPLIER

Figure 2(a) shows a lossy integrator, whose loss is determined by the second triode MOSFET connected to the output. The transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{2}{s + \frac{2}{R_{M2}C}} \quad (2)$$

where $R_{M1}=[\beta_1(V_{C1}-V_{Tn})]^{-1}$ and $R_{M2}=[\beta_2(V_{C2}-V_{Tn})]^{-1}$. It was revealed that, M_2 also receives a fully differential voltage across its drain-source terminals [8]. Therefore, its linearity is also enhanced. It is interesting to note that, as will be revealed, the low-frequency voltage gain of the lossy integrator in Figure 2(a) will be even more linear than that when a linear resistor is connected instead of M_2 as a load. The reason is that, nonlinearities of the triode MOSFETs are alike and reduce themselves one step further. This idea, and the fact that $1/R_{M1}$ conductance of M_1 is linearly dependent on V_{C1} can be a starting point for obtaining a DXCCII-based analog multiplier.

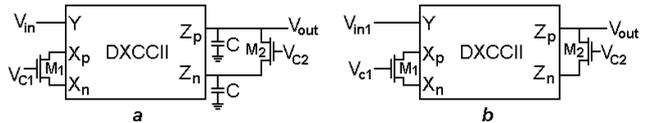


Figure 2. (a) DXCCII-based tunable lossy integrator, (b) DXCCII-based circuit used to obtain the multiplier.

Figure 2(b) shows the DXCCII-based circuit to be used as the analog multiplier. The Y terminal is the first input (V_{in1}). The gate voltage of M_1 (V_{c1}) is no longer pure DC, but has a signal part (the second input V_{in2}) besides its DC

component (V_{C1}); i.e. $V_{c1}=V_{in2}+V_{C1}$. Equation (2) can be used for $C=0$ (i.e. for $2/C = \infty$) to express the output voltage at the Z_p terminal as

$$V_{out} = R_{M2}/R_{M1} V_{in1} \quad (3)$$

By substituting $R_{M1}=[\beta_1(V_{c1}-V_{Tn})]^{-1}$ into Equation (3), V_{out} is obtained in terms of V_{in1} and V_{in2} as,

$$V_{out} = R_{M2}\beta_1 V_{in1} (V_{c1}-V_{Tn}) \quad (4)$$

V_{in1} can take values around the ground level, i.e. it can be positive or negative. So, its DC component is zero. However, V_{c1} should be positive, because the condition

$$V_{c1} > V_{in1,max} + V_{Tn} \quad (5)$$

(equivalent to the condition $V_{G1} > V_{D1} + V_{Tn}$) should be satisfied so as to guarantee that M_1 is in triode region, even for the largest possible V_{in1} value. Actually, when the positive DC component (V_{C1}) of V_{c1} is considered, it is observed that, besides the multiplication component, an additional component appears at the output, such that,

$$V_{out} = k V_{in1} V_{in2} + k V_{in1}(V_{C1}-V_{Tn}) \quad (6)$$

Here, $k=R_{M2}\beta_1$ is the scale factor of the multiplier. It is possible to get rid of the second term on V_{out} , by retrieving the output with respect to a voltage equal to $kV_{in1}(V_{C1}-V_{Tn})$. However, this voltage is not easy to obtain and control, since it is dependent on V_{Tn} which will change with temperature and other effects and also on V_{in1} . Nevertheless, if M_1 and M_2 are matched and V_{C2} is chosen equal to V_{C1} , then, the unwanted additional component becomes

$$k V_{in1}(V_{C1}-V_{Tn}) = V_{in1} \quad (7)$$

which yields

$$V_{out} = k V_{in1} V_{in2} + V_{in1} \quad (8)$$

This means, if the output voltage is taken with respect to a voltage equal to V_{in1} , we can obtain a pure multiplication. It is usually avoided to refer the output voltage to the input node, but fortunately, a copy of V_{in1} available at the X_p terminal. So, the new output can be taken across the terminals Z_p and X_p , such that,

$$V_{Zp} - V_{Xp} = V_{out} - V_{in1} = k V_{in1} V_{in2} \quad (9)$$

Alternatively, the same voltage is available across the terminals X_n and Z_n . Figure 3(a) shows a more detailed structure of the first four-quadrant analog multiplier, with the output modified to its new form given in Equation (9).

III. THE SECOND FOUR-QUADRANT MULTIPLIER

Figure 3(b) shows the second four-quadrant multiplier. For this circuit, two DXCCII are employed to avail fully

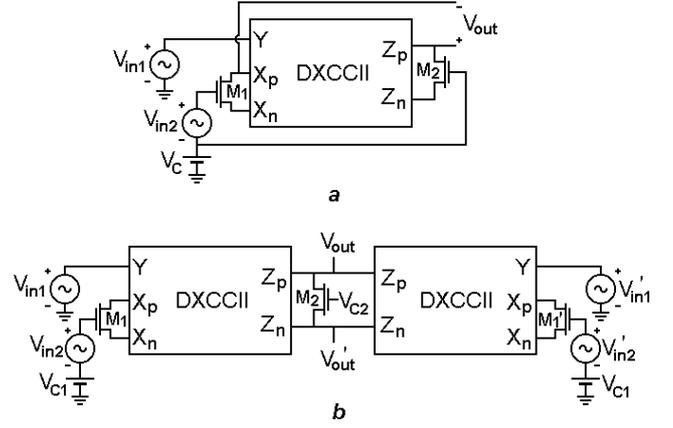


Figure 3. (a) First DXCCII-based four-quadrant analog multiplier, (b) Second DXCCII-based four-quadrant analog multiplier.

balanced (differential) inputs and outputs, defined as

$$V_{out,d} = V_{out} - V_{out}', \quad V_{in1,d} = V_{in1} - V_{in1}', \quad V_{in2,d} = V_{in2} - V_{in2}' \quad (10)$$

where, $V_{in1} = -V_{in1}'$, $V_{in2} = -V_{in2}'$ and $V_{out} = -V_{out}'$. The gates of M_1 and M_1' are again receiving a positive DC component V_{C1} , besides the signals V_{in2} and V_{in2}' . DC components of V_{in1} and V_{in1}' are zero. So as to guarantee that M_1 , M_1' and M_2' are operating in triode region, the following conditions should be satisfied:

$$V_{in2,min} + V_{C1} > V_{in1,max} + V_{Tn} \quad (11)$$

$$V_{C2} > V_{out,max} + V_{Tn} \quad (12)$$

Once the conditions (11) and (12) are satisfied, analyses similar to those conducted for the first multiplier can be carried out to express each output voltage in terms of the input voltages:

$$\begin{aligned} V_{out} &= R_{M2}\beta_1 [V_{in1}(V_{in2}+V_{C1}-V_{Tn}) - V_{in1}(-V_{in2}+V_{C1}-V_{Tn})] \\ &= R_{M2}\beta_1 [V_{in1}V_{in2} - V_{in1}(-V_{in2})] \\ &= 2R_{M2}\beta_1 V_{in1}V_{in2} \end{aligned} \quad (13)$$

Again, $R_{M2}=[\beta_2(V_{C2}-V_{Tn})]^{-1}$. Equation (13) was obtained by using $\beta_1=\beta_1'$ since M_1 and M_1' are matched. Similarly,

$$V_{out}' = -2R_{M2}\beta_1 V_{in1}V_{in2} \quad (14)$$

As can be noticed, the differential signals and the way of connection of the DXCCII helped to cancel the unwanted term, which was a problem in the first four-quadrant multiplier (the second term in Equation (6)). Although, the output can be taken single ended from either V_{out} or V_{out}' , taking the output differentially doubles the voltage swing and helps to improve the linearity further, since even-order non-linearities can be cancelled in this way:

$$V_{out,d} = V_{out} - V_{out}' = 4R_{M2}\beta_1 V_{in1}V_{in2} \quad (15)$$

Since $V_{in1,d}=2V_{in1}$ and $V_{in2,d}=2V_{in2}$, the differential output voltage can also be expressed in terms of the differential input voltages as

$$V_{out,d} = R_{M2}\beta_1 V_{in1,d} V_{in2,d} = k V_{in1,d} V_{in2,d} \quad (15)$$

where again, $k=R_{M2}\beta_1$ is the scale factor.

In this second multiplier, it is no longer required to match M_1 (and M_1') with M_2 and/or set $V_{C2}=V_{C1}$. Therefore, the designer is free to size M_1 (M_1') and M_2 during design, so as to set k to a predetermined value. Also, V_{C2} can be chosen equal to or different than V_{C1} during design. Furthermore, V_{C2} can be varied during operation to adjust the scale factor of the multiplier. Thus, the multiplier has an electronically tunable scale factor, which is an appreciated feature in analog signal processing.

IV. SIMULATION RESULTS AND DISCUSSION

SPICE simulations were performed for both multipliers to reveal their functionality. PSpice9.0 was used with the BSIM3v3 model parameters of a $0.35\mu\text{m}$ 5-V n-well CMOS process. The CMOS implementation shown in Figure 4 was used as the DXCCII, with $V_{DD}=-V_{SS}=2.5\text{V}$, whose operation principle, design considerations, device geometries and performance properties were supplied in [8]. Aspects for the triode MOSFETs were chosen as $(W/L)_1=(W/L)_2=1\mu\text{m}/2.5\mu\text{m}$ in the first multiplier and $(W/L)_1=(W/L)_1'=1\mu\text{m}/3\mu\text{m}$, $(W/L)_2=1\mu\text{m}/1\mu\text{m}$ in the second multiplier.

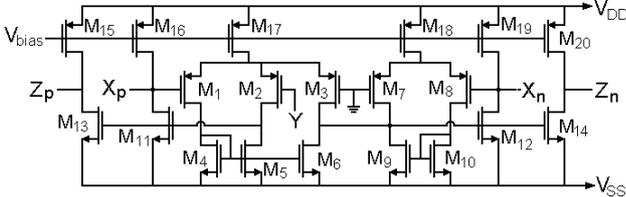


Figure 4. A CMOS implementation of DXCCII.

Figure 5 gives the DC curves for the first four-quadrant multiplier of Figure 3(a). In Figure 5(a), $V_{out}-V_{in1}$ and $\partial V_{out}/\partial V_{in1}-V_{in1}$ curve families are supplied, for which V_{in2} was swept from -0.5V to 0.5V by 0.25V steps. The control voltages for both triode MOSFETs were $V_{C1}=V_{C2}=V_C=2\text{V}$. Besides the $V_{out}-V_{in1}$ curve family, the $\partial V_{out}/\partial V_{in1}-V_{in1}$ curve family which shows the derivative of V_{out} with respect to V_{in1} , supplies a neat idea about the linearity of the multiplier. The more $\partial V_{out}/\partial V_{in1}$ remains constant (for a constant V_{in2}) as V_{in1} is changed, the more linear the multiplier is. Similarly, Figure 5(b) shows $V_{out}-V_{in2}$ and $\partial V_{out}/\partial V_{in2}-V_{in2}$ curve families, which are obtained by changing V_{in1} from -0.5V to 0.5V by 0.25V steps.

Figure 6(a) shows $V_{out,d}-V_{in1,d}$ and $\partial V_{out,d}/\partial V_{in1,d}-V_{in1,d}$ curve families of the second analog multiplier of Figure 3(b), which are obtained by changing $V_{in2,d}$ from -1.5V to

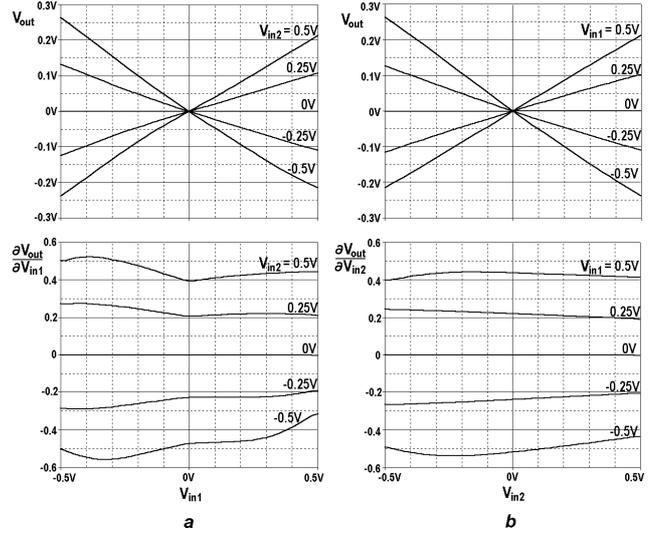


Figure 5 (a) $V_{out}-V_{in1}$ and $\partial V_{out}/\partial V_{in1}-V_{in1}$ curve families, (b) $V_{out}-V_{in2}$ and $\partial V_{out}/\partial V_{in2}-V_{in2}$ curve families for the first analog multiplier of Figure 3(a).

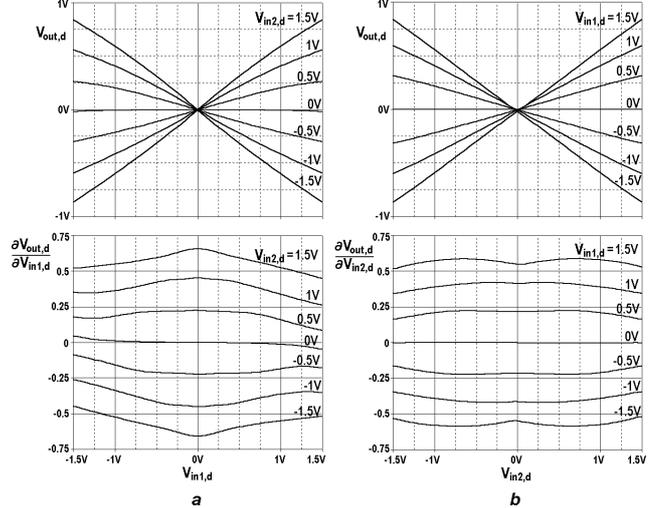


Figure 6 (a) $V_{out,d}-V_{in1,d}$ and $\partial V_{out,d}/\partial V_{in1,d}-V_{in1,d}$ curve families, (b) $V_{out,d}-V_{in2,d}$ and $\partial V_{out,d}/\partial V_{in2,d}-V_{in2,d}$ curve families for the second analog multiplier of Figure 3(b).

1.5V by 0.5V steps (i.e., V_{in2} was swept from -0.75V to 0.75V by 0.25V steps). The control voltages for all three triode MOSFETs were $V_{C1}=V_{C2}=1.75\text{V}$. For the same multiplier, $V_{out,d}-V_{in2,d}$ and $\partial V_{out,d}/\partial V_{in2,d}-V_{in2,d}$ curve families are supplied in Figure 6(b), for which $V_{in1,d}$ was swept from -1.5V to 1.5V by 0.5V steps.

The first multiplier has a narrower input range than that of the second multiplier. This is because the second multiplier operates with differential voltages. Also, the asymmetrical structure of the first realization is another reason for the limited input range. A limitation in one direction is not compensated for by a copy of the circuit which is receiving the complementary value of the input. However, the second circuit makes use of this facility. The asymmetry of the first circuit can also be observed

from its curve families in Figure 5. Nevertheless, it uses a single DXCCII, which is its significant advantage over the second multiplier employing two DXCCIIs.

Besides the input range width and symmetry advantages, the second multiplier supplies another flexibility, which is the tunability feature. As revealed theoretically above, the control voltage V_{C2} of M_2 can be tuned to electronically adjust the scale factor k . This feature of the second multiplier is illustrated in Figure 7 which shows $V_{out,d}$ – $V_{in1,d}$ curve families for two different V_{C2} values. Figure 7(a) and 7(b) shows the curve families for $V_{C2}=1.75V$ and $V_{C2}=2.25V$, respectively, while $V_{C1}=1.75V$.

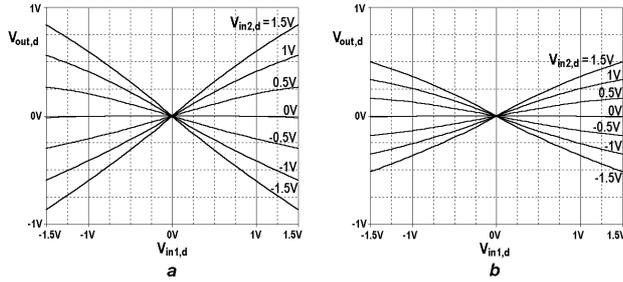


Figure 7 Tunability of the scale factor of the second multiplier: $V_{out,d}$ – $V_{in1,d}$ curve family for (a) $V_{C2}=1.75V$, (b) $V_{C2}=2.25V$.

It is worth mentioning an additional detail: With a triode MOSFET load (i.e. M_2), both multipliers operate more linearly than the case when M_2 is replaced by a linear resistor with an equivalent resistance value. This is because the nonlinearities of M_2 and M_1 (M_1') further eliminate each other with the help of the way of connections of their terminals.

SPICE .AC analyses have shown that both multipliers are capable of operating within acceptable limits roughly up to 100MHz of input signal frequency (for both inputs). However, this result is valid only for very small signal amplitudes. For large signals, it is very likely that the operation will be degraded by static and dynamic nonlinearities (e.g. MOSFET and junction capacitance nonlinearities).

Frequency doubling was taken as a large signal application to reveal the large signal and high frequency performance of the proposed multipliers. The two inputs of the multipliers were driven by the same signal source with an amplitude of 0.5V. In this case, the output voltage is expected to possess a single frequency component twice as much the input signal frequency.

The first multiplier was able to obtain the doubled frequency at the output but an imbalance was observed on the output signal, as shown in Figure 8(a), which is because of the additional frequency components at the output. This result is partly due to the different delays from two inputs to the output. Actually, the dominant

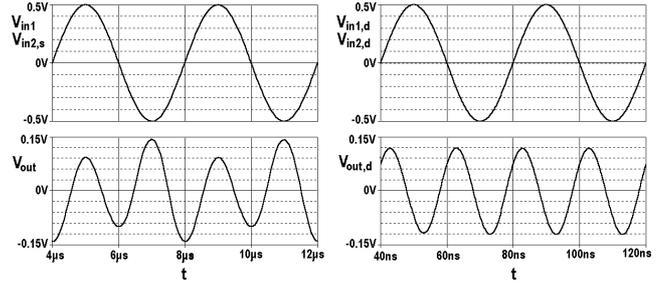


Figure 8 Frequency doubler application with (a) the first multiplier ($V_{C1}=V_{C2}=1.75V$, amplitudes: $V_{in1}=V_{in2}=0.5V$ @ $f=250kHz$), (b) the second multiplier (amplitudes: $V_{in1,d}=V_{in2,d}=0.5V$ @ $f=25MHz$, $V_{C1}=1.75V$, $V_{C2}=1V$).

reason is the significantly different two delays from the inputs to the terminals X_p and from the inputs to the terminal Z_p , caused by the asymmetrical structure and the way of retrieving the output voltage. That is to say, taking the output voltage across the terminals X_p and Z_p degrades the large signal behavior significantly as input signal frequency is increased. For input signal frequencies above roughly 250kHz, the “imbalance” of the output signal was observed to increase further, as can be observed from Figure 8(a), which shows the behavior of the frequency doubler built with the first multiplier, for an input signal frequency of $f=250kHz$. The main component of the output signal is observed as 500kHz.

The second multiplier, with its fully balanced structure, does not possess the disadvantages of the first multiplier mentioned above. Therefore, the large signal behavior is much better, even for much higher frequencies. Figure 8(b) shows the inputs ($f=25MHz$) and output for the frequency doubler which utilizes the second multiplier, with $V_{C1}=1.75V$ and $V_{C2}=1V$. As can be observed from the figure, the output signal possesses a 50MHz component, which is apparently very dominant.

V. CONCLUSION

The two multipliers proposed in this work have different properties. The first multiplier has the advantage of employing a single DXCCII, which helps to keep the consumed power and occupied chip area smaller (almost half) with respect to the second multiplier. However, its large signal and high frequency behavior is apparently worse, mainly due to its asymmetrical structure. The second multiplier uses two DXCCIIs, but it has a fully balanced structure which enhances its linearity, input and output voltage swings and large signal high frequency behavior. So, the first multiplier is suitable for applications where power and/or area consumption is the main concern but a high-frequency operation is not demanded. In higher frequency large-signal applications, the second multiplier is much more suitable, but with increased area and power consumption. Tunability of the second multiplier is an advantageous feature, which brings flexibility to both design and operation.

REFERENCES

1. S. Franco, Design with Operational Amplifiers and Analog Integrated Circuits, Mc Graw-Hill, third edition, pp.615-620, 2001.
2. B. Gilbert, A Precise Four-Quadrant Multiplier with Subnanosecond Response, IEEE J. Solid-State Circuits, Vol. SC-3, No. 4, pp. 365-373, 1968.
3. J.N. Babanezhad and G. C. Temes, A 20-V Four-Quadrant CMOS Analog Multiplier, IEEE J. Solid-State Circuits, Vol. SC-20, No. 6, pp. 1158-1168, 1985.
4. J.S. Pena-Finol and J.A. Connelly, A MOS Four-Quadrant Analog Multiplier Using the Quarter-Square Technique, IEEE J. Solid-State Circuits, Vol. SC-22, No. 6, pp. 1064-1073, 1987.
5. Z. Wang, A CMOS Four-Quadrant Analog Multiplier with Single-Ended Voltage Output and Improved Temperature Performance, IEEE J. Solid-State Circuits, Vol. SC-26, No. 9, pp. 1293-1301, 1991.
6. Y.K. Seng and S.S. Rofail, Design and Analysis of a $\pm 1V$ CMOS Four-Quadrant Analogue Multiplier, IEE Proc. Circuits Devices Syst., Vol. 145, No. 3, pp. 148-154, 1998.
7. H. F. Hamed, F.A. Farg and M.S.A. El-Hakeem, A New Wideband BiCMOS Four-Quadrant Analog Multiplier, Proc. Int. Symposium Circuits and Systems (ISCAS'2002), Vol. 1 pp. 729-732, 2002.
8. A. Zeki and A. Toker, The Dual-X Current Conveyor(DXCCII): A New Active Device for Tunable Continuous-Time Filters, Int. J. Electronics, Vol. 69, No. 12, pp. 913-923, 2002.
9. A. Zeki and A. Toker, DXCCII-based Tunable Gyrator, , Int. J. Electronics and Communications (AEÜ), Vol. 59, No. 1, pp. 59-62, 2005.