New Trends in Circuit Design for Analog Signal Processing

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Abstract

A large number of circuit topologies have been proposed in the literature for analog signal processing such as active filters, oscillators, immittance simulators etc. At the beginning, let's say until twenty years ago, the researchers were proposing this type circuit topologies without giving any realization circuit and application example. Therefore, the main problem was how to realize these topologies and how to apply them to practical work. Another important missing main factor was the influence of the limitations caused by the realization topologies and employed active elements such as bandwidth, slew-rate, input and output impedances etc. This paper covers the main features combining the circuit design with the actual realization circuit demonstrating several performance limitations on chosen circuit examples.

1. Introduction

A large number of circuit topologies have been proposed in the literature for analog signal processing such as active filters, oscillators, immittance simulators etc.[1-22] . At the beginning, let's say until twenty years ago, the researchers were proposing this type circuit topologies without giving any realization circuit and application example. Therefore, the main problem was how to realize these topologies and how to apply them to practical work. Another important missing main factor was the influence of the limitations caused by the realization topologies and employed active elements such as bandwidth, slew-rate, input and output impedances etc.

With the advances in modern technologies such as CMOS, BiCMOS etc., it is possible today to realize simply these type topologies for analog signal processing; as a result, it is no more sufficient and meaningful to propose only these type circuit without considering the above mentioned items. The trend in analog circuit design is now also to demonstrate how to realize the circuit proposed, what are the limitations of circuit performance and what kind of applications these circuits can find in practical world or how to pick-up the desired output signal? It is a well-known fact that there is a large application area of analog signal processing ranging from very low frequencies at several Hz levels of biomedical signals to RF applications operating at GHz level, from EEG signals to cognitive radio and encrypted communications or low-noise amplifiers in wireless communications [3,22]. Therefore the designer should know the limitations that influence the performance of his circuit before realization phase. In other words, without considering the circuit from the point of view of microelectronics and realization technology the work performed is incomplete [1,2,7,8].

This paper covers the main features combining the circuit design with the actual realization circuit demonstrating several performance limitations on chosen circuit examples.

2. Design Examples: OTA-C Filter

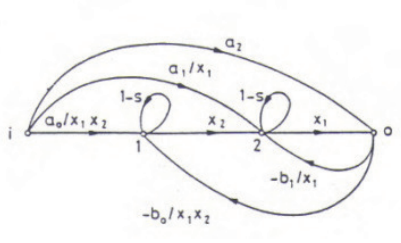
In realization of active filters, the designers assume that active components are linear components. In fact they are non-linear and they behave linear under certain conditions. These conditions depend on design parameters of active components. Violation of these conditions cause non-linear distortion in filters. Hence, the designers should know in advance linear operation conditions of the filter to be realized.

Linear operation conditions for several active components such as OPAMPs, OTAs, CCIs and CCIIs are investigated by introducing macromodels [1–6]. But, not much study is performed as to linear operation of active filters.

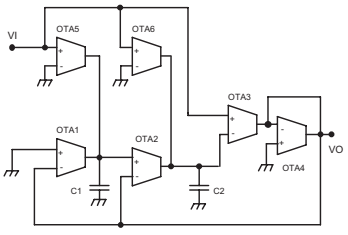
2.1. OTA-C Filter Design

If a given transfer function can be represented by the signal flow graph shown in Fig.1a, the circuit realization can be given asn shown in Fig.1b. The aim is to present a synthesis procedure for the realization of biquadratic active filters using a minimum number of OTAs and grounded capacitors [1].

$$G(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$$



(a)



(b)

Fig. 1. a) signal flow chart b) realization circuit [1]

Various second-order OTA-C filters with a minimum number of OTAs can be derived from the general circuit. These filters realize different filter characteristics such as LP, HP, BP, AP, BS functşons.

2.2. Limitations for input signal

In the implementation of an OTA-C filter the designer must be careful in the determination of the input signal. In practice OTAs do not operate linearly if their output signals exceeds certain limits. If the output voltage of any OTA saturates, we get a clipped wave-form. If the output current saturates, we get a saw-tooth form, which is known as the slew-rate limiting problem.

In the following the maximum input signal level not causing clipping and slew rate limiting is studied. For linear operation the input signal level must be adjusted so that

$$\begin{aligned} |V_k| &\le V_{ks} \quad , \quad k = 1,2,\ldots,n \\ |I_k| &\le I_{ks} \quad , \quad k = 1,2,\ldots,n \end{aligned} \tag{1}$$

Be simultaneously satisfied for the designer specified frequency band $\omega \in [\omega_1, \omega_2]$. Here n is the total number of OTAs used in the design $V_k = V_k(j\omega)$ ve $I_k = I_k(j\omega)$ are the phasor voltage and current respectively at the output of kth =OTA. Vks and Iks are bounds of linear region and we call them the saturation voltage and current respectively of the kth OTA. In the case

$$\begin{aligned} V_{1s} &= \ldots = V_{ns} = V_s \\ I_{1s} &= \ldots = I_{ns} = I_s \end{aligned} \tag{2}$$

where the OTAs are identical, these bounds are equal

In terms of the input voltage these conditions can be written as

$$\begin{aligned} |V_i| . |H_k| &\le V_{ks} = V_s \ , \ k = 1,2,..,n \\ |V_i| . |Y_k| &\le I_{ks} = I_s \ , \ k = 1,2,..,n \end{aligned} \tag{3}$$

where Vi is the amplitude of the filter's input voltage, $|H_k|$ is the voltage transfer function which is defined as the ratio of the kth OTA's phasor voltage to phasor input voltage, $|Y_k|$ is the transfer admittance function which is defined as the ratio of the kth OTA's phasor output current to phasor input voltage.
There exist 2n inequalities. They put the following constraints on the input voltage amplitude for $\omega \in [\omega_1,\omega_2]$:

$$\begin{aligned} |V_i| &\le = \frac{V_s}{|H_k|} \ , \ k = 1,2,..,n \\ |V_i| &\le \frac{I_s}{|Y_k|} \ , \ k = 1,2,..,n \end{aligned} \tag{4}$$

The common solution of these inequalities which gives the maximum value of the input voltage amplitude not causing clipping and slew rate limiting can be expressed as

$$\begin{aligned} |V_i|_{max} &= \min\left(\frac{V_s}{|H_k(j\omega)|_{max}}, \frac{I_s}{|Y_k(j\omega)|_{max}} \right), \\ k &= 1..n \end{aligned} \tag{5}$$

where H_{kmax} and Y_{kmax} are maximum value of H_k and Y_k respectively for the designer specified band.

The method is demonstrated on a 3MHz Butterworth LP filter design illustrated in Fig 2.

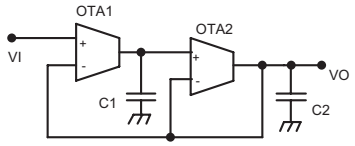


Fig. 2. LP filter derived from Fig.1b.

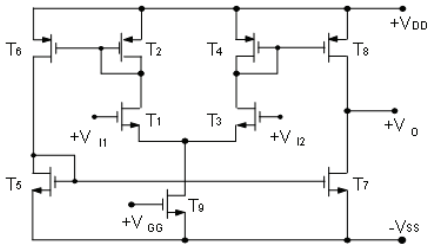


Fig. 3. Simple symmetrical CMOS OTA structure.

The OTAs are designed using the simple symmetrical CMOS OTA structure shown in Fig.3. To get a transconductance of 1.33mA/V the amplifier bias current is chosen as I_B=336µA. The limits are specified as V_S = 3.27v, I_S = 560µA; the capacitances are determined as C_1 = 100pF, C_2 = 50pF. The related voltage transfer functions and the admittance functions are

$$\begin{aligned} H_1 &= \frac{V_1}{V_I} = \left(1 + j\omega\frac{Q_P}{\omega_P}\right).H_2(j\omega) \\ H_2 &= \frac{V_2}{V_I} = \frac{{\omega_P}^2}{(j\omega)^2 + (\frac{\omega_P}{Q_P}).(j\omega) + \omega_P^2} \\ Y_1 &= \frac{I_1}{V_I} = g_m.(1 - H_2) \\ Y_2 &= \frac{I_2}{V_I} = g_m.(H_1 - H_2) \end{aligned} \tag{6}$$

Using these equations and the linearity boundaries of active elements we obtain

$$\begin{aligned} |H_1(j\omega)|_{max} &= 1.029 \\ |H_2(j\omega)|_{max} &= 1 \\ |Y_1(j\omega)|_{max} &= 1632\,\mu A/V \\ |Y_2(j\omega)|_{max} &= 666\,\mu A/V \end{aligned}$$

The maximum input voltage value of the filter can be calculated as

$$|V_1|_{max} = 0.34V$$

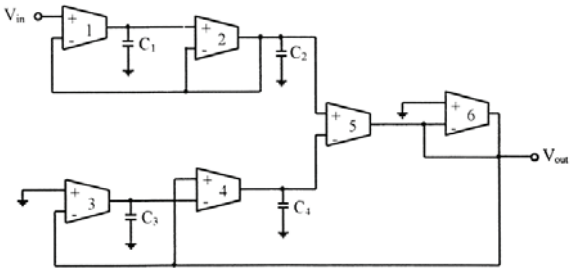
2.3. Application example: Design of EEG filters for biomedical applications

The rapid increasing use of battery-operated portable equipment in application areas such as telecommunications and medical electronics imposes the use of low-power and small-sized circuits realized with VLSI (very large scale integrated) technologies. CMOS (complementary metal–oxide semiconductor) circuits operating in the subthrehold (weak inversion) region introduce a versatile solution for the realization of low-power VLSI building blocks . Circuits needed for processing of biological signals are a typical and good example of low-power and small-sized building blocks. The main features of biological signals are their low amplitude and low frequency range.

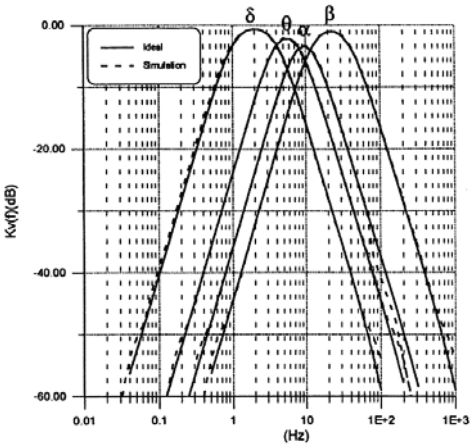
The human electroencephalogram (EEG), which provides a rich picture of the electrical activities of the brain, is one of the most important biological signals. The voltage amplitudes of EEG signals range from about 1–100 mV peak-to-peak at low frequencies (0.5–100 Hz) at the cranial surface.

It is possible to realize low-frequency OTA-C active filters with small capacitance values of the order of 25–400 pF. The circuit technique described is applied to the α (8–12 Hz), β (13–40 Hz), θ (4–8 Hz) and δ (1–4 Hz) band filters for EEG signals. Because of small capacitance values the filter circuit is suitable for realization on a single VLSI chip using the CMOS technology, and enables the user to implement the circuit on implantable biotelemetric applications.

The filter chip is fabricated in Turkish Scientific and Technological Council (TUBITAK) laboratory. Realized filter topology, filter frequency responses, CMOS OTA structure, chip layout, capacitance values, biasing currents and OTA transconductances are shown in Fig.4 [1,3].



(a)



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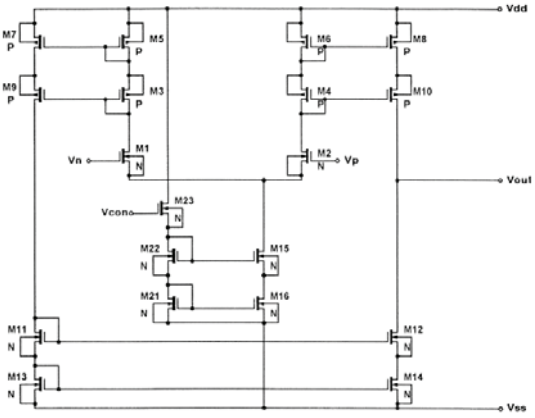

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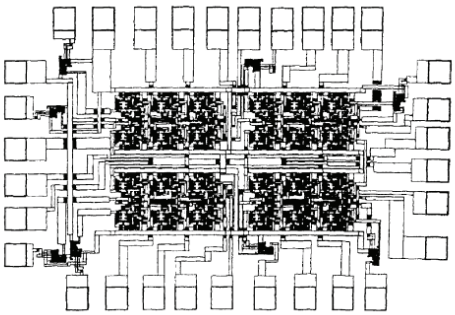

(d)

Capacitance values for the α, β, θ and δ bands of the EEG signal

Band	f_{P1} (Hz)	f_{P2} (Hz)	C_1 (pF)	C_2 (pF)	C_3 (pF)	C_4 (pF)	I_B (nA)	G_{mf} (nA/V)
α	12	8	166	81	250	122	0.69	8.8
β	40	13	81	40	250	122	1.125	14.3
θ	8	4	125	61	250	122	0.347	4.4
δ	4	1	62.55	30.6	250	122	0.1	1.1

(e)

Fig. 4. (a) Fourth order OTA-C based EEG filter, (b) frequency responses, (c) CMOS OTA, (d) filter layout, (e) capacitance values, biasing currents and OTA transconductances [3].

2.4. Design of high performance DOTA with high output resistance

The use of current-output-based active devices (COBADs), such as OTAs, current conveyors, etc. in continnous time filter design, has been attracting a large amount of interest, especially because of their wider bandwidths with respect to those of equivalent opamps. An important drawback of COBAD-based continuous time filters is the finite output resistance *(Rout)* of a COBAD, which, in a basic integrator structure, is in parallel with the load capacitor $\boldsymbol{C_L}$ causing a lossy integration, thus generating filtering errors. Classical cascode current output stages cannot handle a load capacitor of the order of several picofarads at low frequencies (e.g. for f < 1 kHz): therefore integration cannot be performed beyond this limit [4-6]. Choosing large C, values (e.g. scveral nanofarads) is not a reasonable solution, since this requires very large areas on a chip. Therefore, very high output impedance current output stages are required, both to enable filtering at low frequcncies and to reduce filtering errors.

Precision current mirrors with very high R_{out}: The regulated cascode (RGC) stage (Fig. *5a)* achieves a very high output impedance with the aid of active negative feedback through amplifier MK-I_K, and source follower M3. The current mirror (CM) in Fig. *5b* employs the RGC stage to achieve a very large *Rout* [4]. Precision is maintained by making $\boldsymbol{I_K}$ dependent on I_{IN} to, achieve $\boldsymbol{V_{GSK}}$ = V_{GSI} equality (thus, V_{DS2} = V_{DSI} equality), for any input current level. To save power and area, MA and MK can be relatively smaller than M1, i.e. $(W/L)_A = (W/L)_K = (W/L)_1/\kappa$; where $\kappa > 1$ [5,6]. Then, matching MB and MC will be sufficient to achieve the $\boldsymbol{I_K} = I_{IN}/\kappa$ equality satisfactorily. Further precision improvements can be maintained by choosing long channel lengths for MB and MC; and, as in the CM of Fig. *5c,* by using additional devices (MD and ME) to maintain $V_{DSA} = V_{DSK} = V_{DSI}$.

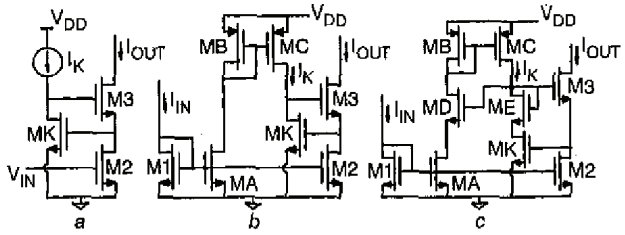

Fig. 5. Active-feedback cascode structures *a)* RGC surge *b)* Active-feedback cascode CM **c)** Improved active-fccdback cascode CM [4]

In fully-differential structures, better PSRR, CMRR, distortion and input/output swing perrormances are achieved with respect to those of single-ended structures [4]. Also fewer active devices are required in a filter or oscillator. It is possible to efficiently implement the active-feedback CMs of Fig. 5 into a differential-output COBAD (e.g. a DOTA or a dual output current conveyor), enabling further reduction of excess power and area consumption. The incorporation of the CM of Fig. *5b* into a DOTA structure is described below. The method is also valid for the CM of Fig. *5c* and can be applied to other differential- output COBADs.

Since inverted and non-inverted copies of output-stage currents are conveyed both by PMOS and NMOS CMs in a DOTA (or in a differential-output COBAD) the dependent I_K current of each active-feedback CM can be obtained easily, simply by connecting a single transistor (MC) in parallel, to wpy this current. Thus, MA and MB are eliminated, reducing the consumed power and chip area, as well as parasitics. The resulting circuit is given in Fig. 6. It is worth mentioning that the new circuit does not need any additional biasing for the cascode stages. Actually, an 'adaptive biasing' is performed by the active feedback within each RGC stage.

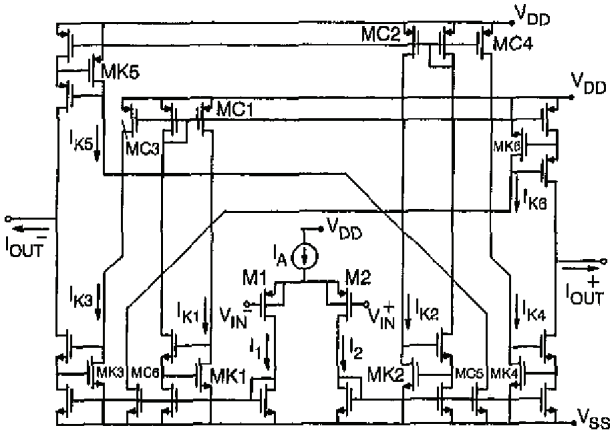

Fig. 6. Proposed CMOS DOTA structure [4]

Table-1. Comparison of the performance with DOTA conventional structure.

	Classical cascode DOTA	Proposed cascode DOTA
DC Gain (differential)	81.9dB	122dB
GBW	234MHz	392MHz
R_{out} (differential)	283MΩ	28.5GΩ
C_{out} (differential)	30fF	18fF
Power dissipation	450μW	496μW

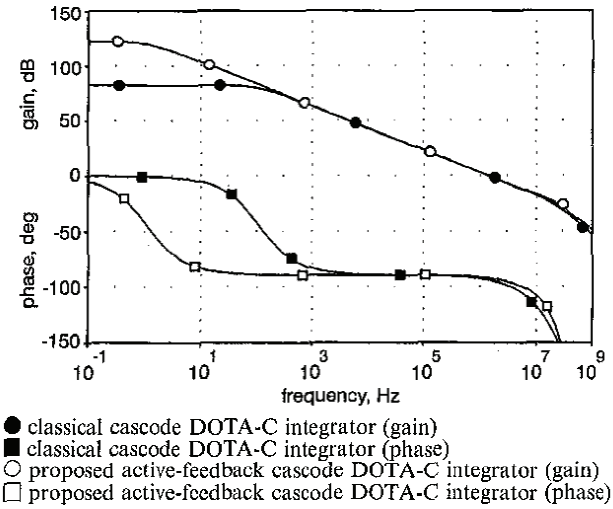

Fig. 7. Gain and phase response of simulated DOTA-C integrators [4]

Fig. 7 shows the gain and phase responses of two DOTA-C integrators constructed with the proposed DOTA and the equivalent classical cascode DOTA, with C_L = 5pF. AC plots prove that the proposed structure enables integration within a much wider frequency range.

3. Design Examples: CCII-based filter design

Limitations on input signal level in voltage- and current mode CCII-based active RC filters have appeared recently in literature [7,8].

In the following, using linear operation conditions of typical CMOS current conveyors, limitations on input signal amplitiude in voltage-mode and currnet-mode current conveyor filters will be studied. A simple formula is derived for maximum input signal amplitudes not causing a non-linear operation.

3.1. CCII-based voltage mode filter

The circuit representation of noninverting (CCII+) and inverting (CCII-) types of second generation current conveyors are shown in Fig. 8(a) and (b). Circuit configurations [10] for CMOS realization of CCII+ and CCII- are also illustrated in Fig. 5(c) and (d), respectively, where *vx*(t), *vy*(t), *vz*(t), *ix*(t), *iy*(t) and *iz*(t) are terminal voltages and currents, respectively.

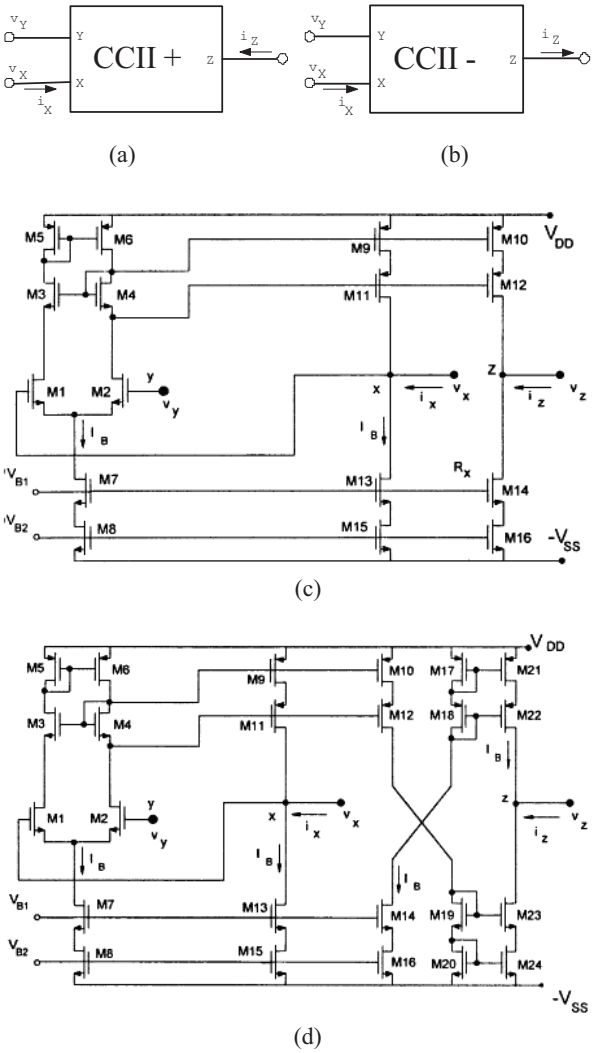

Fig. 8. (a) Circuit represantation of an ideal CCII+; (b) circuit represantation of an ideal CCII- CMOS realization of an CCII+ and (d) CMOS realization of an CCII- [7]

In ideal case CCIIs are characterized by

$$\begin{aligned} i_y(t) &= 0 \\ v_x(t) &= v_y(t) \\ i_z(t) &= \pm i_x(t) \end{aligned} \tag{7}$$

In actual case CCIIs are non-linear components and behave linearly if the following conditions are satisfied:

$$\begin{aligned} I_{xm-} \le i_X(t) \le I_{xm+} \\ V_{xm-} \le v_X(t) \le V_{xm+} \\ V_{zm-} \le v_Z(t) \le V_{zm+} \end{aligned} \tag{8}$$

where V_{xm+} , V_{xm-} , V_{zm+} , V_{zm-} , I_{xm+}, I_{xm-} represent maximum positive and negative voltage at the *x*-terminal, maximum positive and negative voltage at the *z*-terminal and the maximum positive and negative current at the *x*-terminal, respectively.

There are saturations in *x*-terminal and *z*-terminal voltages and currents. If *x*-terminal or *z*-terminal voltage of any current conveyor saturates, this causes clipped waveform in filter. If *x*-terminal or *z*-terminal current of any current conveyor saturates, this causes sawtooth waveform, which is known as the slew-rate limiting problem [1,2]. For a filter employing n CCIIs we can write the following equations:

$$\begin{aligned} &|V_i| \,.\, |T_{xk}| \le V_{sxk} \\ &|V_i| \,.\, |T_{zk}| \le V_{szk} \qquad k = 1,2,..,n \\ &|V_i| \,.\, |Y_{kx}| \le I_{sxk} \end{aligned} \tag{9}$$

where the quantities are defined as follows:

$$\begin{aligned} T_{xk} &= \frac{V_{xk}(j\omega)}{V_i}, k = 1,2,..,n \\ T_{zk} &= \frac{V_{zk}(j\omega)}{V_i}, k = 1,2,..,n \\ Y_{xk} &= \frac{I_{xk}(j\omega)}{V_i}, k = 1,2,..,n \end{aligned} \tag{10}$$

In order to operate the current conveyors in the linear region we have to impose the specified restrictions on *vx*, *vz* and *ix*. In other words, for a proper operating region the following inequalities must be satisfied for each of CCIIs:

$$\begin{aligned} |V_i| &= \frac{V_{sxk}}{|T_{xk}|} \\ |V_i| &= \frac{V_{szk}}{|T_{zk}|} \\ |V_i| &= \frac{I_{sxk}}{|Y_{kx}|} \end{aligned} \tag{11}$$

Similar to OTA-based filter circuits, the maximum input level can be expressed as:

$$|V_i|_{max} = \min\left(\frac{V_{sxk}}{|T_{xk}|_{max}}, \frac{V_{szk}}{|T_{zk}|_{max}}, \frac{I_{sxk}}{|Y_{kx}|_{max}}, k = 1..n\right) \tag{12}$$

for the specified frequency region $\omega \in [\omega_1, \omega_2]$.

The result is demonstrated on the following 3rd order Butterworth filter circuit shown in Fig.9.

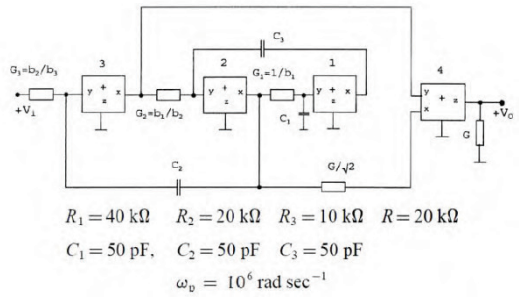

Fig. 9. 3rd order Butterworth filter [7]

The maximum values of the related transfer functions and transfer admittances are specified as follows:

$$|T_{x1}(j\omega)|_{max} = 1 \qquad |Y_{x1}(j\omega)|_{max} = 72.516\mu A/V$$
$$|T_{x2}(j\omega)|_{max} = 1.667 \qquad |Y_{x2}(j\omega)|_{max} = 127.636\mu A/V$$
$$|T_{x3}(j\omega)|_{max} = 1.58 \qquad |Y_{x3}(j\omega)|_{max} = 72.658\mu A/V$$
$$|T_{x4}(j\omega)|_{max} = 1.58 \qquad |Y_{x4}(j\omega)|_{max} = 51.334\mu A/V$$
$$|T_{zi}(j\omega)|_{max} = 0, \qquad i = 01,2,3$$
$$|T_{z4}(j\omega)|_{max} = 1.027$$

Using these values the maximum input signal level is calculated as

$$|V_I|_{max} = 1.6V$$

This result is verified by the SPICE simulations of the filter.

3.2. CCII-based current mode filter

For linear operation of filter employing n CCIIs, the input signal level must be adjusted so that the following conditions are simultaneously satisfied for every current conveyor in the filter for the specified frequency band $\omega \in [\omega_1, \omega_2]$:

$$\begin{aligned} |V_{xk}| &\le V_{sxk} \\ |V_{zk}| &\le V_{szk} \qquad k = 1,2,...,n \\ |I_{xk}| &\le V_{szk} \end{aligned} \tag{13}$$

where n denotes the total number of current conveyors used in the design. *Vxk and Vzk* are, respectively, the phasor voltages at the x- and z-terminal of the kth current conveyor. *Ixk* is also the phasor current through the x terminal of the kth current conveyor. Vsxk, *Vszk* and Isxk are the bounds of the linear region obtained from the transfer characteristics or from the linear operation conditions, and these are termed the saturation voltages and current of the kth current conveyor [8].

$$|I_{in}| \le \frac{V_{sxk}}{|Z_{xk}|}, |I_{in}| \le \frac{V_{szk}}{|Z_{zk}|}, |I_{in}| \le \frac{I_{sxk}}{|A_{xk}|}, \ k = 1,2,..,n \tag{14}$$

where I_{in} is the amplitude of the filter's input current, and *Zxk, Zzk,* and *Axk,* are the transfer functions defined as

$$Z_{xk} \le \frac{V_{xk}(j\omega)}{I_{in}}, Z_{zk} \le \frac{V_{zk}(j\omega)}{I_{in}}, A_{xk} \le \frac{I_{xk}(j\omega)}{I_{in}}$$
$$k = 1,2,..,n \tag{15}$$

Using these the maximum input level can be specified for the specified frequency region $\omega \in [\omega_1, \omega_2]$ as

$$|I_i|_{max} = \min\left(\frac{V_{sxk}}{|Z_{xk}|_{max}}, \frac{V_{szk}}{|Z_{zk}|_{max}}, \frac{I_{sxk}}{|A_{xk}|_{max}}, k = 1..n\right) \tag{16}$$

where $|Z_{xk}|_{max}$, $|Z_{zk}|_{max}$, $|A_{xk}|_{max}$ are the maximum values of $|Z_{xk}|$, $|Z_{zk}|$, $|A_{xk}|$.

The method is applied to an example of third order Butterworth filter shown in Fig.9. The results obtained are:

$$|Z_{xi}(j\omega)|_{max} = 0, i = 1,2,3 \qquad |Z_{x4}(j\omega)|_{max} = 20k\Omega$$
$$|Z_{z1}(j\omega)|_{max} = 20.19k\Omega$$
$$|Z_{z2}(j\omega)|_{max} = 23.4k\Omega \qquad |Z_{z3}(j\omega)|_{max} = 10k\Omega$$
$$|Z_{z4}(j\omega)|_{max} = 0$$
$$|A_{x1}(j\omega)|_{max} = 1.11, \qquad |A_{x2}(j\omega)|_{max} = 1.56$$
$$|A_{x3}(j\omega)|_{max} = 1.17, \qquad |A_{x4}(j\omega)|_{max} = 0.69$$

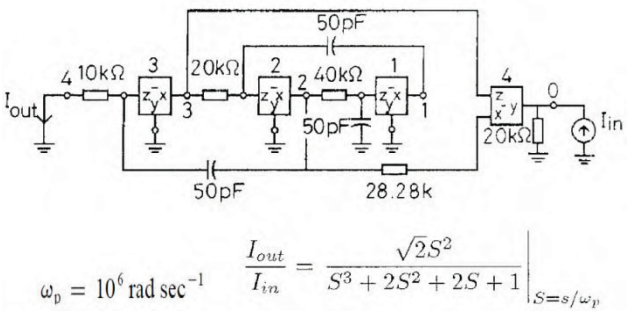

Fig. 10. CCII-based current-mode active filter.

Resulting value for the maximum input level is specified as

$$|I_i|_{max} = \min\left(\begin{matrix}\infty,\infty,\infty, 397\ \mu A, 450\ \mu A, 388\ \mu A, \infty \\ 104.6\mu A, 74.4\mu A, 99.3\mu A, 167\ \mu A\end{matrix}\right)$$
$$= 74.4\mu A$$

4. CMOS FTFN Realization and Application

Current-mode circuits have received significant attention due to their particular advantages compared with voltage-mode circuits. They offer the designer several salient features such as inherently wide bandwidth, greater linearity, wider dynamic range, simple circuitry and low power consumption. Recently, attention has turned to use of the four terminal floating nullor (FTFN) as current-mode active element since it has been shown that the FTFN is a more flexible, versatile and stable active element.

The FTFN is ideally a transconductance amplifier featuring infinite gain and two output currents. The basic equation describing its operation is $Iw = Iz = Gm.(V\,x\text{-}V\,y)$ For a infinite open loop transconductance gain Gm, the difference between the two differential voltages increases as Gm decreases. Therefore the open loop transconductance gain should be as large as possible to acheive high performance operation. Symbol of FTFN is illustrated in Fig.11, providing the definition equations:

$$I_1 = I_2 = 0 \qquad I_{O1} = I_{O2} \qquad Vx = Vy \tag{17}$$

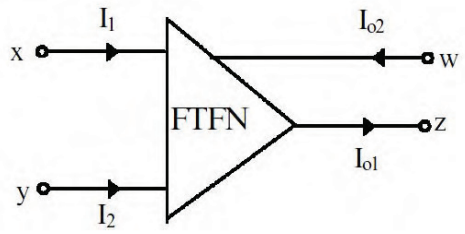

Fig. 11. Symbol of the FTFN [9].

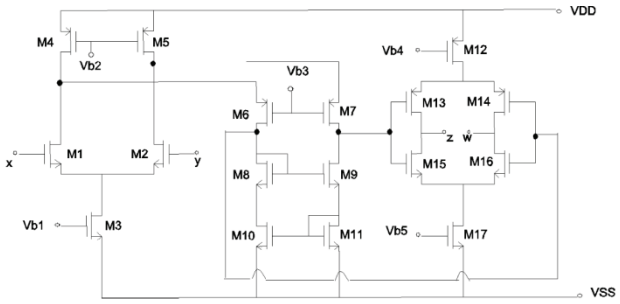

Fig. 12. CMOS realization of FTFN [9].

A CMOS realization example of FTFN is given in Fig.12 [9]. It consist of a common-source and common-gate amplifiers and a floating current source, Arbel and Goldminz outputstage.

4.1 Application Example: Realization of mixed-mode chaotic circuit employing FTFNs

Chaotic circuits can be effectively used in chaotic secure communication systems. Chaotic circuits for use in chaotic secure communication systems must not only have a simple design but also a structure that is able to provide greater reliability in the form of a wide range of parameter variations and extra security keys. Mixed-mode chaotic circuit has such a chaotic circuit structure, that exhibits both autonomous and nonautonomous chaotic Dynamics via switching method. This circuit's structure is extremely simple and it contains only one nonlinear resistor.

In this section, the inductorless realization of mixed-mode chaotic circuit is described. For this purpose, instead of inductor elements in mixed-mode chaotic circuit, FTFN based inductance simulators have been used [12,13].

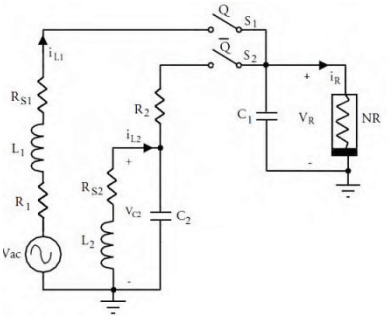

Fig. 13. Mixed-mode chaotic circuit.

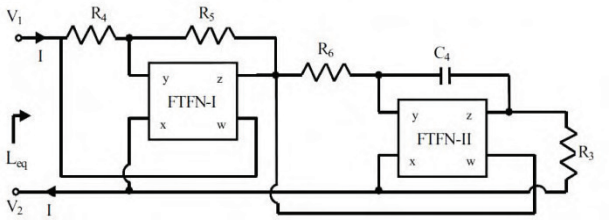

Fig. 14. FTFN-based inductance Simulator [12,13].

FTFN-based inductance simulators are used instead of floating inductance L1 and grounded inductance L2 in Fig. 13. FTFN based floating inductance Simulator is shown in Fig. 14. Routine analysis yields equivalent inductance between terminals 1 and 2 as:

$$L_{eq} = \frac{C_4 R_3 R_4 R_6}{R_5} \tag{18}$$

In Fig. 14, the following element values are chosen: R3 = R4 = R5 = R6 = 1 K, C4 = 18 nF to simulate L1 = L2 = 18 mH. Floating inductance is also used as grounded inductor by connecting to ground one port of the floating inductance for simplicity. Chaotic waveform and double-scroll attractor are illustrated in Fig. 15.

The simulation results indicate that improved mixed-mode chaotic circuit using FTFN and CFOA topology exhibit its original chaotic behaviors. The CMOS implementation of mixed-mode chaotic circuit using FTFN-based inductance simulators provides new possibilities to the design of the integrated circuit realization of chaotic communication systems.

5. Conclusions

This paper describes the main features combining the circuit design with the actual realization circuits demonstrating several performance limitations on chosen circuit examples of OTA-C based filters, CCII-based voltage and current-mode filters. Furtheremore, a CMOS FTFN realization is given with an application example of inductorless chaotic circuit realization.

The examples given demonstrate clearly how to realize a circuit topology and how to apply them to practical work.

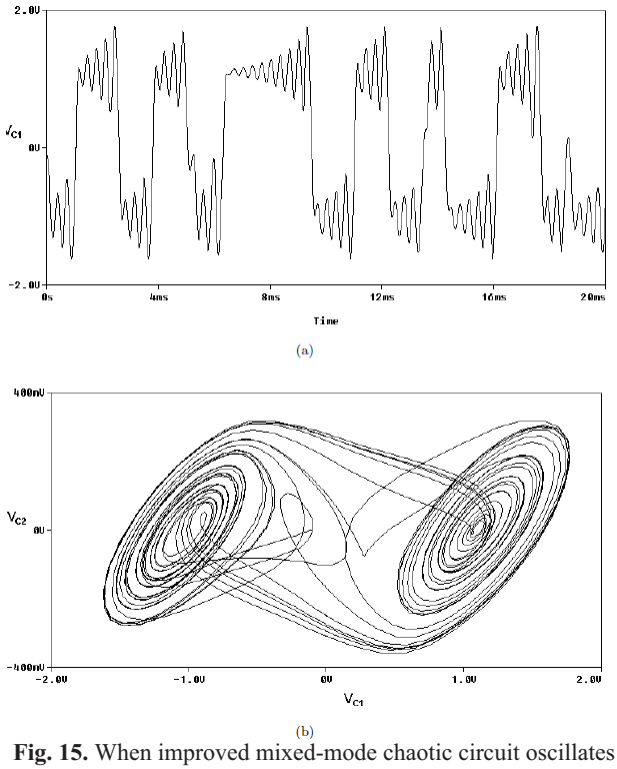

Fig. 15. When improved mixed-mode chaotic circuit oscillates in autonomous mode (S1-OFF, S2-ON), (a) the chaotic waveform of the voltage across capacitor C1 in Fig. 13, and (b) double-scroll chaotic attractor.

6. References

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