Modeling Single Event Crosstalk in Nanometer Technologies

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Abstract

With advances in CMOS technology, circuits become increasingly more sensitive to transient pulses caused by single event (SE) particles. On the other hand, coupling effects among interconnects can cause SE transients to contaminate electronically unrelated circuit paths which may increase the SE susceptibility of CMOS circuits. This work, for the first time, proposes an SE crosstalk noise estimation method for use in design automation tools. The proposed method uses an accurate 4-π model for interconnect and correctly models the effect of non-switching aggressors and tree branches noting the resistive shielding effect. The SE crosstalk noise expressions derived show good results in comparison to HSPICE results. Results show that average error for noise peak is about 5.2% while allowing for very fast analysis in comparison to HSPICE.

1. Introduction

Terrestrial soft errors in memory have been a very well known problem [1]. However, due to increasing clock frequencies and shrinking feature sizes soft errors are now affecting CMOS logic. It has been predicted that for 45 nm technologies and below the majority of the observed radiation induced soft failures will be due to transients that will occur in combinational logic (CL) circuits [2].

For commercial chips at ground level, soft errors are mainly induced by alpha particles emitted from radioactive decay of uranium and thorium impurities located within the chip packaging and due to atmospheric neutrons [1]. When an energetic radiation particle strikes the sensitive area within a combinational circuit such as the depletion region of transistor drains, many hole-electron pairs can be created due to ionization mechanism. These free carriers can later drift under the electric field creating a transient voltage pulse. This transient is named as single event transient (SET) and can pass through a series of CL gates and reach to storage elements under certain conditions. If the generated pulse arrives at the storage element during its latching window, incorrect data can be stored resulting in soft error. This is also termed as single event upset (SEU).

With increasing coupling effects, an SET pulse generated on a circuit node is no longer limited to the logic path existing between the hit node and a latch. The interconnect coupling effects can cause SETs to contaminate electronically unrelated circuit paths which can in turn increase the "SE Susceptibility" of CMOS circuits to SETs [3], [4].

Although SETs are considered as the main reason for radiation induced soft errors in CL, for mission-critical high-reliability applications such as avionics [5], medical systems [6], and etc., additional sources such as SE coupling effects must also be included in analysis in addition to SETs.

The interaction caused by parasitic coupling between wires, the crosstalk, may cause undesired effects such as voltage glitches, signal delays or even delay reduction [7-9]. If crosstalk effects on the victim (affected) net are large, they can propagate into storage elements that connected to victim line and can cause wrong data storage.

It is no longer just the normal signal switching events on aggressor (affecting) lines that are responsible for such crosstalk effects. As technology scaling continues, the charge deposited due to an SE particle on aggressor line may also create cross-coupling noise effects on victim line, and in some cases the effects can be larger than a normal crosstalk [3].

With increased coupling effects, the SET generated on a circuit node may affect multiple paths due to strong coupling among wires. Fig. 1 shows aggressor victim pair along with its drivers and receivers. An SE hit at the drain of OFF PMOS transistor of the inverter driver causes output to go towards logic 1 (or VDD) for some pulse duration. The SE transient voltage created, in turn, can affect the victim line through coupling capacitor C_c inducing SE crosstalk noise on the victim.

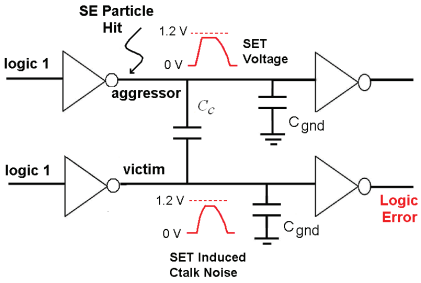

Fig. 1. SE crosstalk noise (lumped wire model is for demonstration).

The cross-coupling noise effects produced by SE hits can violate noise margins of gates connected to victim line and may result in logic errors. Serious effects may occur if the affected line is somewhat important such as a clock line [5].

Balasubramanian *et al*. have shown that SETs can produce crosstalk effects on neighboring lines that can induce logic level state changes for interconnects as small as 100 µm on technologies 90 nm and lower [3]. Later work in [10] has experimentally measured the SE induced crosstalk in a 90 nm process and proved the existence of the problem. Recent work in [4] studied the SE crosstalk effects using an accurate distributed model for interconnect, and suggested hardening techniques for SE crosstalk. Although, the problem is studied in detail, there has not been any work in the modeling of SE crosstalk effects.

Traditional SPICE simulators can be used to estimate crosstalk effects in signal lines. While results are accurate, due to density of interconnect lines, these simulations are time

inefficient [7-9]. A rapid and accurate crosstalk noise estimation alternative is needed in a limited design cycle time so that one can quickly verify if a given wire routing solution will not lead to logic failures caused by the coupled noise.

In this work, the crosstalk noise generated on victim line due to an SET pulse on aggressor will be calculated for the first time to our knowledge. The formulas developed will provide good basis to gain insight into the effects of SE pulse transients on the crosstalk noise. With closed-form expressions, the crosstalk pulse dependency on various design parameters can be observed via sensitivity expressions obtained.

2. Single Event Crosstalk Modeling

The proposed SE crosstalk model uses a 4-π interconnect model in which both the victim and aggressor nets are modeled using the 2-π circuits [8], [9]. Fig. 2 shows the 4-π template used in SE crosstalk calculation. In this model, RC parameter values are calculated based on technology and geometric information from Fig. 2a. The coupling node (node 2) is set to be the center of the coupling portion of the victim net. We assume the upstream and downstream resistance/capacitance at node 2 to be R_{1a}/C_{ua} and R_{2a}/C_{da}, respectively. Similarly for victim net, let's assume upstream and downstream resistance/capacitance at node 5 to be R_{1v}/C_{uv} and R_{2v}/C_{dv}, respectively. Then, for aggressor and the victim line:

$$C_{1a} = C_{ua}/2,\ C_{2a} = (C_{ua} + C_{da})/2 \text{ and, } C_{la} = C_{da}/2 + C_{lda}$$
$$C_{1v} = C_{uv}/2,\ C_{2v} = (C_{uv} + C_{dv})/2 \text{ and, } C_{lv} = C_{dv}/2 + C_{ldv}$$

where,

C_{lda} and C_{ldv} represent the load capacitances for aggressor and victim lines, respectively.

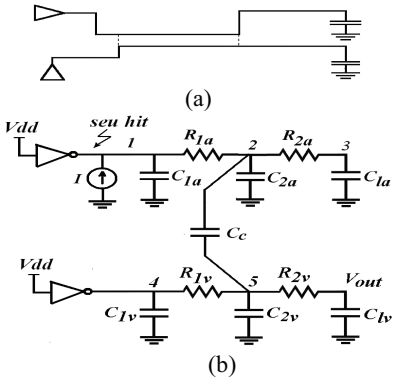

Fig. 2. The 4-π model for two coupled interconnects

For most on-chip lines or interconnects, capacitive effects are still the dominant factor [7-9], hence we ignore inductance effect in our modeling.

We assume that both driver inputs are at logic 1 and a positive charge deposition occurs on aggressor driver output due to an SE particle. It is also assumed that both the aggressor and victim drivers can be represented approximately by holding resistances of on-transistors [11], [12].

In Fig. 3, the effective resistances R_{da} and R_{dv} model the holding resistances of aggressor and victim drivers, respectively. Each holding resistance models the effect of on transistors (NMOS) that dissipate the charge and restore the node to its original logic value.

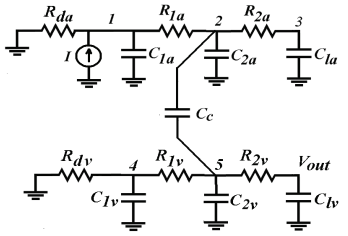

Fig. 3. SE crosstalk calculation using the 4-π template circuit.

An SE hit has been simulated at the output of the aggressor driver using a double exponential current source that can be approximated by:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

where,

Q is the charge (positive or negative) deposited by the particle strike, τ_α is the collection time constant of the p-n junction, τ_β is the ion-track establishment time constant. The time constants τ_α and τ_β are dependent on process technology and are taken as 100 ps and 5 ps, respectively based on [12].

The multiline crosstalk model proposed in [9] has been adopted for SE crosstalk estimation in this work. In this model, the loading effects of non-switching (passive) aggressors and aggressor tree branches are correctly modeled using equivalent capacitances. The model is advantageous over techniques which simply use lumped capacitors [8] at coupling/branching point.

In our work, the line where the SET generates due to particle strike is taken as the active aggressor, while any other nets coupled to the victim are considered as passive aggressor lines. It is also assumed that none of the lines switch during particle strike so that an SE crosstalk noise effect is generated rather than a delay effect.

3. Modeling of Passive Aggressor and Tree Branches

A victim line can be coupled to many non-switching (passive) aggressors. A passive aggressor follows victim waveform and contributes to the stability of the victim line. Therefore, equivalent load capacitance at the victim coupling point is less than coupling capacitance and can be formulated using coupling/branching admittance concept [9], [13]. The equivalent capacitance formula for a passive aggressor is derived assuming an exponential aggressor waveform. For this, the passive aggressor is first reduced to the simple circuit shown in Fig. 4b, where [9]:

$$R_a' = R_{th} + R_{1a} \quad (2)$$

$$C_a' = C_{2a} + C_{la} + (R_{th}^2/(R_{th} + R_{1a})^2)\, C_{1a} \quad (3)$$

Assuming an exponential waveform and zero initial condition, the equivalent capacitance, C_{eq} (Fig. 4c) can be calculated by matching the capacitor currents and integrating it over $0 \le t \le 5t_r$ interval, where t_r is the exponential rise time constant (more detail can be found in [9]) :

$$C_{eq} = C_c\left[1 + \frac{C_c R_a'}{t_r - R_a'(C_a' + C_c)} \cdot e^{\frac{-5t_r}{R_a'(C_a' + C_c)}}\right] \quad (4)$$

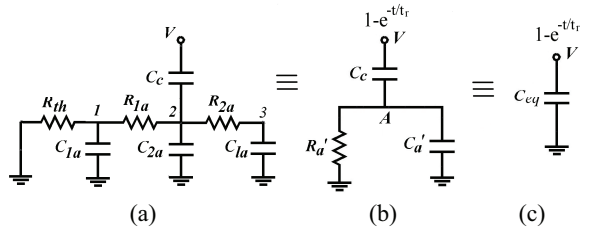

Fig. 4. A non-switching aggressor net coupled to the victim line

Most previous work also treats aggressor net branches simply as lumped capacitances at branching point [7], [8]. However, the capacitance seen at the branching node is less than the total branch capacitance due to resistive shielding effect [9].

For this, the tree branches are reduced to a simple π-model following the moment matching method as demonstrated in [13]. This model is then reduced to an equivalent branching capacitance $C_{eq\text{-}br}$ (Fig. 5).

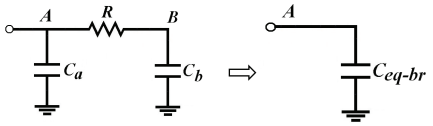

Fig. 5. Obtaining an equivalent branching capacitance

Assuming a rising exponential voltage at input node and zero initial condition, an equivalent branching capacitance can be obtained after matching input currents of both circuits [9]:

$$C_{eq-br} = C_a + C_b\left[1 + \frac{RC_b}{t_r - RC_b}e^{-5t_r/RC_b}\right] \qquad (5)$$

4. Aggressor Waveform Calculation at Coupling Node:

In the proposed model, the aggressor waveform at the coupling node is first calculated and then entered to the transfer function between the coupling node and the victim output to obtain victim noise voltage.

In order to calculate aggressor coupling node waveform correctly on node 2 (see Fig. 3), the victim loading effect needs to be included. For this, the victim line is first reduced into an equivalent capacitor C_{eqv} using the passive aggressor net reduction techniques as summarized in Section 3.

After obtaining C_{eqv}, a source transformation is also implemented on aggressor input giving the final circuit shown in Fig. 6. As shown in Fig. 6, the voltage source resulting from source transformation has been represented using two voltage sources in series. This is merely done for convenience in calculation. The sources V_{in1} and V_{in2} are given as:

$$V_{in1} = \frac{QR_{da}}{t_\alpha - t_\beta}(1 - e^{-t/t\beta}) \quad \text{and} \quad V_{in2} = \frac{QR_{da}}{t_\beta - t_\alpha}(1 - e^{-t/t\alpha}) \qquad (6)$$

respectively.

We consider one input at a time (V_{in1} or V_{in2}) using Superposition to find the coupling node waveform. For this, the aggressor branches after the coupling point (the π-network shown on the right) are also reduced to an equivalent capacitance C_{req} using the tree branch reduction techniques given earlier.

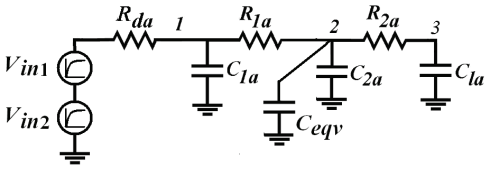

Fig. 6. Decoupled aggressor line for coupling node voltage calculation.

The equivalent branching capacitance for V_{in1} ($C_{req\text{-}\beta}$) is given by:

$$C_{req-\beta} = C_{2a} + C_{la}\left[1 + \frac{R_{2a}C_{la}}{t_r - R_{2a}C_{la}}e^{\frac{-5t_\beta}{R_{2a}C_{la}}}\right] \qquad (7)$$

Fig. 7 shows the resulting circuit for coupling node voltage calculation (shown for V_{in1} input). The transfer function between the input and coupling node 2 is calculated as:

$$\frac{V_2(s)}{V_{in}(s)} = \frac{1}{st_{a1} + 1} \qquad (8)$$

where,

$$t_{a1} = C_{1a}R_{da} + (C_{eqv} + C_{req-\beta})(R_{da} + R_{1a})$$

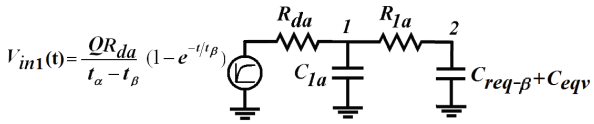

Fig. 7. Aggressor waveform calculation at coupling node.

We note that t_{a1} in fact is the Elmore delay between the input and Node 2. Finally, the delayed waveform at coupling node for the first input is calculated to be:

$$V_2'(t) = \frac{QR_{da}}{t_\alpha - t_\beta}(1 - e^{-t/t_{\beta n}}) \qquad (9)$$

where,

$$t_{\beta n} = t_\beta + t_{a1}$$

Similarly, the delayed waveform at coupling node due to V_{in2} (Fig. 7) can be calculated. Finally, the coupling waveform is given by:

$$V_2(t) = V_2'(t) + V_2''(t) = \frac{QR_{da}}{t_\alpha - t_\beta}(1 - e^{-t/t_{\beta n}}) + \frac{QR_{da}}{t_\beta - t_\alpha}(1 - e^{-t/t_{\alpha n}}) \qquad (10)$$

where,

$$t_{\alpha n} = t_\alpha + C_{1a}R_{da} + (C_{eqv-\alpha} + C_{req-\alpha})(R_{da} + R_{1a})$$

5. Output Voltage Formulation

In output voltage formulation, the aggressor waveform at coupling location is entered to the transfer function to calculate victim noise as shown in Fig. 8. Referring to Fig. 8, we have:

$$1/Z_1 = 1/R_d + sC_{1v} \qquad (11)$$

$$1/Z_2 = 1/(R_{2v} + sC_{lv}) + sC_{2v} + 1/(Z_1 + R_{1v}) \qquad (12)$$

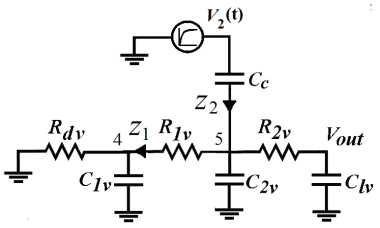

Fig. 8. Output voltage calculation.

The transfer function between the coupling node and the victim output can be obtained as:

$$V_{out}(s) = \frac{1}{sC_{lv}R_{2v}+1}\frac{Z_2}{Z_2+1/sC_c}V_2(s) \qquad (13)$$

The dominant pole approximation method can be hired to reduce complexity of the transfer function [14], [15]:

$$\frac{V_{out}(s)}{V_2(s)} = \frac{s\tau_x}{s\tau_v+1} \qquad (14)$$

where,

$$\tau_v = R_d(C_c + C_{1v} + C_{2v} + C_{lv}) + R_{1v}(C_c + C_{2v} + C_{lv}) + R_{2v}C_{lv}$$

and, $\tau_x = (R_d + R_{1v})C_c$

Finally coupling node waveform in (10) can be inserted in (14) to finally obtain the V_{out} expression In time domain, the victim output noise waveform is given by:

$$V_{out}(t) = \frac{QR_{da}\tau_x}{(t_\alpha - t_\beta)}\left[\frac{e^{-t/t\beta n}}{t_{\beta n}-\tau_v} - \frac{e^{-t/t\alpha n}}{t_{\alpha n}-\tau_v} + \frac{(t_{\beta n}-t_{\alpha n})e^{-t/\tau_v}}{(t_{\alpha n}-\tau_v)(t_{\beta n}-\tau_v)}\right] \qquad (15)$$

Noise peak has been traditionally used as a metric to determine if the noise is at an acceptable level. Since, the above equation contains three exponential terms and it is difficult to find a closed-form expression for amplitude. However, one can obtain a function $f(t)$ which can be used in Newton's iteration method to solve for the time t_{peak} where noise peak V_{peak} occurs:

$$f(t) = \frac{dV_{out}}{dt} = \frac{QR_{da}\tau_x}{(t_\beta - t_\alpha)}\left[\frac{e^{-t/t\beta n}}{t_{\beta n}(t_{\beta n}-\tau_v)} - \frac{e^{-t/t\alpha n}}{t_{\alpha n}(t_{\alpha n}-\tau_v)} + \frac{(t_{\beta n}-t_{\alpha n})e^{-t/\tau_v}}{\tau_v(t_{\alpha n}-\tau_v)(t_{\beta n}-\tau_v)}\right] = 0 \qquad (16)$$

Then, t_{peak} can be found using:

$$t_{peak\,k+1} = t_{peak\,k} - f(t_{peak\,k})/f'(t_{peak\,k}) \qquad (17)$$

This method converges very rapidly after little iteration. The noise peak voltage V_{peak} is found after inserting t_{peak} in (15):

A similar victim noise expression can also be obtained for the case that a negative particle strike occurs at the output of aggressor driver. In this case, since both driver inputs are at logic 0, the holding resistances of PMOS transistors should be utilized in noise formulation.

Summary:

The following steps summarize for the proposed model:

1. Determine the particle charge based on the environment, find constants t_α and t_β that is needed to model the SE particle strike.
2. Calculate the equivalent capacitance value $C_{eq\text{-}a}$ for each passive aggressor that is coupled to victim line. This capacitor is then placed in parallel at victim coupling node.
3. Reduce any aggressor tree branches using an equivalent branching capacitance $C_{eq\text{-}br}$ at branching point.
4. Repeat the same procedure in step (2) for the victim line, and find an equivalent capacitance value $C_{eq\text{-}v.}$ This capacitor updates the value of C_{2a} at the active aggressor coupling point. The formula for $C_{eq\text{-}v}$ is slight variation of eqn. (4).
5. Calculate the new time constants $t_{\alpha n}$ and $t_{\beta n}$ at aggressor coupling point.
6. Calculate other time constants τ_x and $\tau_{v.}$
7. Using the iteration formula find the time that noise peak occurs, which is t_{peak}.
8. Finally obtain V_{peak} by inserting t_{peak} in (15) and decide whether the noise is important or not.

6. Validation of the Proposed Model

We have tested our proposed model using over 1000 randomly generated cases to simulate real-time cases in 65nm technology. The SE crosstalk model has been coded in C++ environment and results are verified by comparing to HSPICE outputs. While the proposed model used a 4-π template, HSPICE simulation utilized a 20-π representation to model the distributed behavior. In Spice modeling, the coupling capacitances were also distributed.

We assumed two parallel interconnects on intermediate layer that are driven by minimum size inverters. It was also assumed that the loads at the end of wires are identically sized inverters. Various interconnect spacing, length and widths were examined. Interconnect lengths were varied from 200 μm up to 2 mm with coupling portion changed. Some of these nets also included some tree branches. The parameter values for these test circuits have been derived using interconnect model given in [16]. The simulated deposited charges, Q_{dep}, were selected in the range 20-150 fC.

Table 1 shows the SE Crosstalk noise calculation results for the first 15 cases. In this table, R_{agg}/C_{agg} and R_{vic}/C_{vic} denote aggressor and victim line resistance/capacitance, respectively. Finally, C_c indicates the coupling capacitance values taken for each case.

For the 15 test cases considered, the proposed model has an average error of 5.46% when compared to HSPICE. For all cases shown, the percent error stayed less than 15%.

Table II summarizes the results obtained for 1000 random test circuits considered. In this table, the percentage of nets that fall into the given error ranges has been given. For example, about 86% of nets have errors less than 10 percent when predicting the noise peak voltage. On the other hand, around 97% of all nets have errors less than 15%.

Results show an average error of 5.2% for the noise peak when compared to HSPICE results.

Table 1. Experimental results obtained in first 15 cases

Case #	Q_{dep} (fF)	R_{agg} (Ω)	R_{vic} (Ω)	C_{agg} (fF)	C_{vic} (fF)	C_c (fF)	Noise (mV) HSPICE	Noise (mV) Model	|Error %|
1	100	400	500	29	37	50	0.443	0.471	6.32
2	150	350	450	31	40	45	0.670	0.708	5.67
3	75	380	490	30	41	45	0.374	0.407	8.82
4	94	210	225	12	14	27	0.483	0.520	7.66
5	65	225	260	14	17	30	0.368	0.375	1.90
6	90	900	900	64	64	112	0.647	0.667	3.09
7	125	364	357	21	20	48	0.740	0.760	2.70
9	120	452	450	27	27	57	0.734	0.746	1.63
10	46	184	232	13	14	23	0.350	0.376	7.43
11	95	356	451	22	27	44	0.533	0.576	8.07
12	35	125	130	11	14	16	0.140	0.155	10.71
13	89	190	210	13	15	23	0.492	0.509	3.46
14	150	460	475	31	40	55	0.710	0.755	6.34
15	65	592	592	37	37	73	0.489	0.502	2.66
								Average % Error	**5.46%**

The CPU time for these test circuits ranges from 0.02 mS to 0.29 mS on a 3.0 GHz Pentium IV machine which suggests that the model calculation is at least a 1000X faster than HSPICE.

Table 2. The percentage of nets that fall into the error ranges

Error Range	V_{peak}
Within ±5 %	73.33%
Within ±10%	86.12%
Within ±15%	97.33%
Avg. Error	5.194%

7. Conclusion

In this work, we proposed a fast SE crosstalk noise estimation method for use in design automation tools. The proposed method uses an accurate 4-π model for interconnect and correctly models the loading effect of neighboring lines and net tree branches noting the resistive shielding effect. The dominant pole approximation was used in moderation which resulted in increased accuracy of model.

For the deposited charge levels considered in terrestrial environment, the derived SE crosstalk noise expressions show very good results in comparison to HSPICE results. Results show that average error for noise peak is about 5.2% while allowing for very fast analysis compared to HSPICE.

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