THE REALISATION OF DEFUZZIFICATION CIRCUIT USING IMPROVED DIFFERENTIAL DIFFERENCE CURRENT CONVEYORS

Mahmut TOKMAKÇI Mustafa ALÇI Esma UZUNHİSARCIKLI
e-mail: tokmakci@erciyes.edu.tr e-mail: malci@erciyes.edu.tr e-mail: uzunhise@erciyes.edu.tr
Erciyes University, Faculty of Engineering, Department of Electronics Engineering, 38039, Kayseri, Turkey

Key words: Defuzzification circuit, Differential Difference Current Conveyor (DDCC), Multiplier

ABSTRACT

In this study, design and analysis of improved Differential Difference Current Conveyor (DDCC) based defuzzification circuit is introduced. Since DDCCs have got high input impedance, low output impedance and arithmetic operation capability, these circuit blocks is suitable for defuzzification circuit using Center Of Gravity (COG) method. The behavior of proposed defuzzification circuit offers high speed, higher linearity, and wider frequency range than CCII-based defuzzfication circuit. The performance of the proposed circuit is illustrated on DC and AC characteristics with SPICE simulations.

I. INTRODUCTION

In hardware implementations of fuzzy systems, CMOS-based design and current-mode circuit building blocks are most preferable, due to the requirement of high speed, low power and reduced system chip size [1,2]. Current Conveyors (CC) and CC-based new circuit topologies such as CCII, Differential Difference Amplifier (DDA) and DDCC are useful in many analogue signal processing circuits [3-6]. Several applications, such as amplifiers, filters, multipliers, dividers, oscillators and signal-processing main blocks using these circuits have been proposed in the literature [4-7].

The DDA was proposed [5] and different applications have been found such as; amplifiers, a MOS grounded resistor, four quadrant multipliers, amplitude modulators [7]. Due to high input impedance, arithmetic operation capability of DDA, the components of the circuits using DDA can be lower than the CCII. Besides CCII has another disadvantage that only one of the input terminals has a high-input impedance which is especially evident if processing of differential signals is needed. To overcome these disadvantages, the DDA and CCII have been combined and functionally extended. Hence Differential Difference Current Conveyor (DDCC) was obtained [6].

Analogue multipliers are useful building blocks in the realisation of functions such as automatic gain control, modulation, filtering, defuzzification circuit, etc. Defuzzification circuit is the output stage of fuzzy systems. The center of gravity (COG) is the most popular defuzzification method in Fuzzy Logic Controllers (FLC). Various defuzzification circuits using COG method are described in literature [8]. A high-speed digital defuzzification circuit based on BiCMOS technology has been proposed in [9] but the fabrication cost is high. The other defuzzification circuit design with current-mode analog circuits [10] such as CCII-based defuzzification circuit [11] was proposed. However, above mentioned circuits have both frequency range is low and bandwidth is narrow.

In this study, it is shown that improved DDCC-based defuzzification circuit using COG method has wider frequency range than DDCC-based [6] and CCII-based defuzzification circuit [11].

II. THE PROPOSED DEFUZZIFICATION CIRCUIT

In this section, we describes the defuzzification circuit which is composed of DDCC-based multiplier and divider circuits. Therefore, it will be explained basic DDCC, improved DDCC, DDCC-based multiplier and divider circuits, respectively.

The center of gravity (COG) method in voltage-mode is expressed as

$$V_{out\,(COG)} = \frac{\sum_{i=1}^{n} V_{\mu i} . V_i}{\sum_{i=1}^{n} V_{\mu i}} \qquad (1)$$

where n represents the number of fuzzy sets on the universe of discourse, $V\mu_i$ and V_i represent the membership function output and support value of the *i* th fuzzy set, respectively. Eqn. (2) can be arranged with voltage values of input/output variables as follows:

$$V_{out} = \frac{V_{\mu 1}.V_1 + V_{\mu 2}.V_2 + ... + V_{\mu n}.V_n}{V_\Sigma} \quad (2)$$

where V_Σ is equal to $\sum_{i=1}^{n} V_{\mu i}$.

The proposed defuzzification circuit block (Eqn. 2) is constructed with building blocks as shown in Fig.1. The circuit block consists of multipliers with voltage-input and current-output [12]. The each multiplier's and divider's output are expressed as follows:

$$I_{oi} = F(V_{\mu i} \times V_i) \quad (3)$$

$$V_o = F(I_o \div V_\Sigma) \quad (4)$$

DDCC-based defuzzification circuit including multiplier and divider building blocks are presented in the next sections.

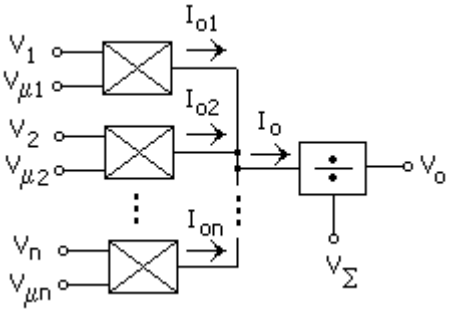


Figure 1. The block diagram of proposed defuzzification circuit

2.1. Differential Difference Current Conveyor (DDCC)

DDCC whose symbol is shown in Figure 2, is a five-terminal network with terminal characteristics described by Eqn. (5a-5c):

$$I_{y1} = I_{y2} = I_{y3} = 0 \quad (5a)$$

$$V_x = V_{y1} - V_{y2} + V_{y3} \quad (5b)$$

$$I_z = \pm I_x \quad (5c)$$

Where the plus and minus sign indicate whether the conveyor is configured as an inverting or noninverting circuit, termed DDCC- or DDCC+ [12].

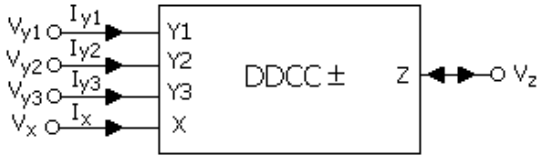


Figure 2. The DDCC's symbol

2.2. Improved DDCC

Although the improved DDCC is the same structure of DDCC [6], the building blocks of DDCC are replaced with high-performance counterparts to extend the overall performance of the DDCC. The Improved DDCC is represented very low x-input resistance and very high z-output impedance by using negative series-feedback via a class-AB current mirror and enhanced cascode current mirror, respectively [12]. Also, the frequency range of improved DDCC is wider than than CCII+ [11] and DDCC+ [6] as shown in Fig. 3.

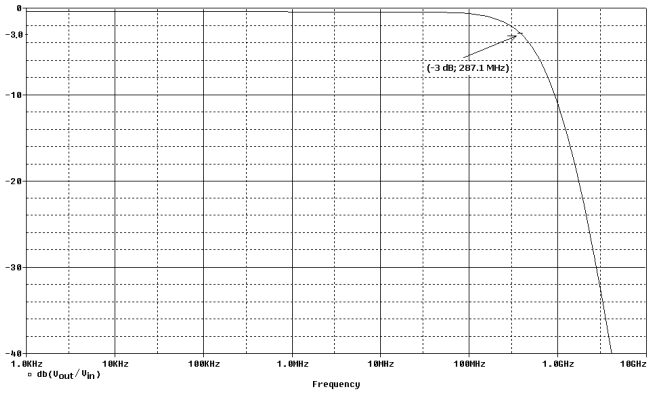


Figure 3. Frequency curve of improved DDCC+ (R_L=1K)

2.3. DDCC -Based Multiplier

DDCC-based multiplier can be constructed using DDCC-based differential squarer as shown Fig. 4. Assuming the pair of the MOS transistors in Fig 4 are well matched and V_G is high enough to ensure that both MOS transistors operate in triode region, squarer's transfer function can be derived as Eqn. (6).

$$I_0 = K_A (V_1 - V_2)^2 \quad (6)$$

Where K_A is squarer constant.

If DDCC- is used in squarer circuits, same squarer's transfer function as Eqn. (6), have been obtained [12].

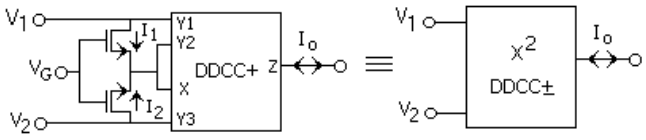


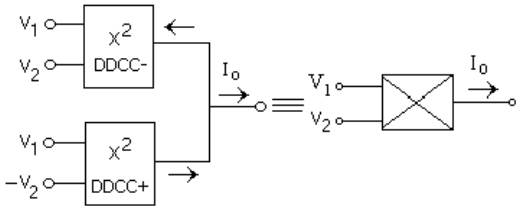
Figure 4. DDCC-based squarer

DDCC squarer-based multiplier whose block diagram are shown in Fig 5. Squarer-difference technique is used to construct in this circuit and its transfer characteristic can be obtained as Eqn. (7).

$$I_0 = K_M V_1 V_2 \quad (7)$$

Where K_M is multiplier constant and the sign of K_M can be either positive or negative.
The operation constraint of multiplier is;

$$V_1, |V_2| \le V_G - V_T \tag{8}$$



(a) (b)

Figure 5. (a) DDCC based multiplier (b) the symbol of multiplier

This paper is shown that DDCC-based multiplier is simpler than the DDA-based multiplier [7] and CCII-based multiplier [11]. Because of input signal both V_1 and V_3 connect to drain/source of the transistors, it is not necessary to use additional circuits to synthesis the 'V_G+V_1' signal at the gate of transistors in the DDCC-multiplier circuits.

2.4. DDCC-Based Divider

The divider circuit is basically composed of a multiplier circuit block with DDCC+ and DDCC- as shown in Fig. 6(a). A simple divider can be easily implemented using a DDCC-based multiplier as above explained. Also, this circuit is not required a linear voltage-to-current (V-I) convertor for DDCC-based defuzzification circuit. The output of divider as shown in Fig. 6 is given by

$$I_o = K_M V_o V_D \tag{9}$$

$$V_o = \frac{I_o}{K_M V_D} \tag{10}$$

The computation unit DDCC-based defuzzification circuit block is shown in Fig. 7. The output current of first multiplier block (Mul.1) is function of input voltages product and is expressed as

$$I_o = F(V_1 \times V_2) = K_{M1} V_1 V_2 \tag{11}$$

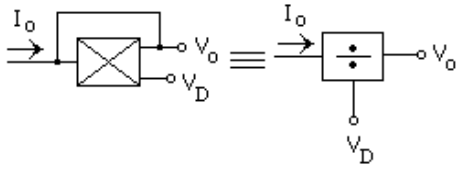
If the output current in Eqn. (11) is placed in Eqn. (10), the output voltage of the proposed divider will be expressed as follows:

$$V_o = \frac{K_{M1} V_1 V_2}{K_{M2} V_3} \tag{12}$$

where the division ratio ($K_D = K_{M1}/K_{M2}$) is related to W/L coefficients of MOS transistors in proposed circuit. If the division ratio is determined as divider constant (K_D), the output of divider circuit can be given by

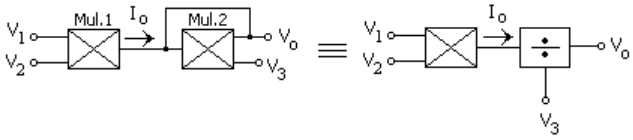
$$V_o = K_D \frac{V_1 V_2}{V_3} \tag{13}$$

Eqn. (13) is similar to Eqn. (2). If V_1, V_2 and V_3 are replaced with V_i, $V_{\mu i}$, and V_Σ, respectively, it will be obtained one term of defuzzification operation in Eqn. (2) for K_D=1.



(a) (b)

Figure 6. (a) Divider circuit block (b) corresponding symbol of divider



(a) (b)

Figure 7. A computation unit of DDCC-based defuzzification circuit . Fig.7. (a) is equal to Fig.7. (b).

III. SIMULATION RESULTS

The behaviour of the implemented improved DDCC-based multiplier circuit was confirmed with 0.5µm MIETEC CMOS process model parameters by PSPICE simulations [12]. The PSPICE-DC analysis results of multiplier circuit (Fig.5 (a)) are shown in Fig. 8, where V_1 is [-0.5 V; +0.5 V] in amplitude, V_2 is varied DC signal forms between [-0.5V; 0.5V] in 0.1 V steps.

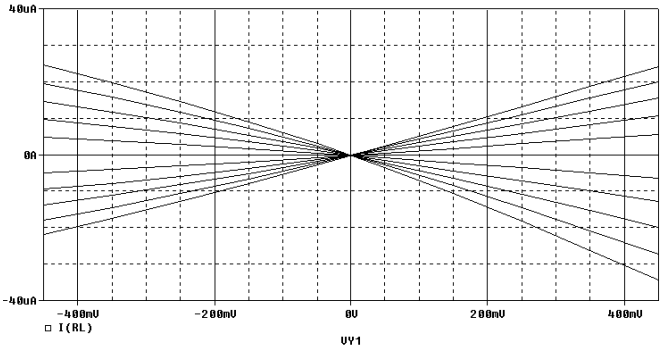


Figure 8. DC transfer curves of improved DDCC-based multiplier circuit

The PSPICE- Transient analysis results of improved DDCC-based multiplier circuit are shown in Fig. 9, where V_1 is a 10 MHz sinusoidal waveform of ±0.5 V in amplitude, V_2 is 2 MHz sinusoidal waveform of ±0.5 V in amplitude. In the simulations of proposed defuzzification circuit, the circuit parameter values are determined as follows: V_{DD}=2.5 V, V_{SS}= -2.5 V, -0.5 V ≤ V_i ≤ +0.5 V, 0 V ≤ $V_{\mu i}$ ≤ 5 V, V_G=1.76 V, R_L=10 KΩ.

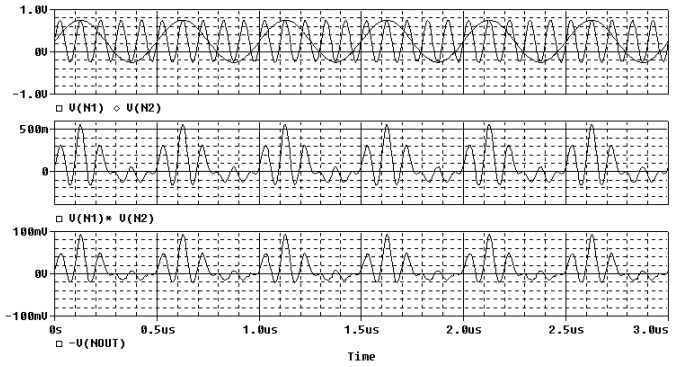


Figure 9. Transient response of improved DDCC-Based Multiplier circuit for two input signals [V_1 (10MHz; ±0.5 V; sinusoidal form), V_2 (2MHz; ±0.5 V; sinusoidal form)]

The numerical result of two-input defuzzification circuit is obtained as follows:

$$V_o = K_D((V_{i1}.V_{\mu 1}) + (V_{i2}.V_{\mu 2}))/V_\Sigma \qquad (14)$$

The numerical and simulation results of improved DDCC-based defuzzification circuit are shown together in Fig. 10. Two input sinusoidal signals, V_{i1} and V_{i2}, with different high frequencies (20 MHz and 5 MHz) are applied to defuzzification circuit that shown in Fig. 1. The membership voltages ($V_{\mu 1}$ and $V_{\mu 2}$) are selected 0.5 V. The sum of membership voltages, V_Σ, is 1.0 V value. Since all multipliers in defuzzification circuit is identical, the division constant K_D is equal to 0.5. The simulation data is measured with a 10 kΩ output resistor.

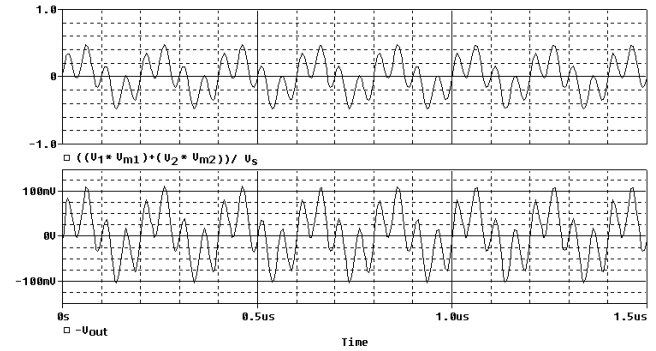


Figure 10. The numerical and simulation results of improved DDCC-based defuzzification circuit for two input signals (V_{i1}, 20 MHz; V_{i2}, 5 MHz; $V_{\mu 1}$= $V_{\mu 2}$=0.5 V; V_Σ=1.0 V)

IV. CONCLUSION

In this study, improved DDCC-based defuzzification circuit for high frequency operating is presented. The circuit has high-speed operation and high accuracy due to differential difference current conveyor's features. The defuzzification circuit is composed of DDCC-based multiplier and divider circuits. The behaviour of the defuzzification circuit has been verified with PSPICE using the models for 0.5 μm MIETEC CMOS process parameters. The simulation results have been confirmed with theoretical results. Therefore, the proposed circuit is suitable for high-speed fuzzy logic controllers using COG defuzzification method.

REFERENCES

1. A. Rodriguez-Vazques, R. Navas, Delgado-Restituto, M., And Vidal-Verdu, F., 'A Modular Programmable CMOS Analog Fuzzy Controller Chip', *IEEE Trans. on Circuits and Systems-II*, 46, No.3, 251-265, 1999.
2. M. Tokmakçı, M. Alçı, R. Kılıç, A CMOS-Based Membership Function Circuit', *Int. Jour. Of Analog Integrated Circuits and Signal Processing*, Vol. 32, No.1, pp. 83-88, July 2002.
3. A.S. Sedra, K.C. Smith, The Current Conveyor: history, progress and new results, *IEE Proc.*, Vol.137, Pt.6, No.2, pp. 78-87, April 1990.
4. S. I. Liu, D. S. Wu, H. W. Tsau, J. Wu, J. I.I. Tsay, Nonlinear Circuit Applications with Current Conveyors, IEE Proc.G., 140, 1-6, 1993
5. E. Sackinger, W. Guggenbuhl, A Versalite Building Block: The CMOS Differential Difference Amplifier, IEEE J., SC. 22., 287-294, 1987
6. W. Chiu, S. I. Liu, H. W. Tsao, J. J. Chen, CMOS Differential Difference Current Conveyors and Their Applications, IEE Proc. 143, 91-96, 1996
7. S. C. Huang, M. Ismail, Design and Applications of a CMOS Analog Multiplier Cell Using Differential Difference Amplifier, Analog Integrated Circuits and Signal Processing, 6, 209-217, 1994.
8. B.D. Liu, C.Y. Huang, H.Y. Wu, Modular current-mode defuzzification circuit for fuzzy logic controllers, *Electron. Lett*., 30, (16),1287-1288, 1994.
9. J.B. Kuo, H.J. Huang, S.S. Chen, and C.S. Chiang, BiCMOS dynamic defuzzifying circuit for fuzzy logic controllers, *Electron. Lett*., 29, (1), 67-68, 1993.
10. M. Tartagni, and P. Perona, Computing centroids in current-mode technique, *Electron. Lett*., 29, (1), pp.1811-1813, 1993.
11. M. Tokmakçı, M. Alçı, E. Uzunhisarcıklı, CCII-Based Defuzzification Circuit For Fuzzy Logic Controllers, IFSA 2003-International Fuzzy Systems Association World Congress, 29 june-02 july 2003.
12. A. Duruk, H. Kuntman, A. Toker, O. Çiçekoğlu, New Improved CMOS Implementation of Differential Difference Current Conveyor, Proc. Of. Int. Conference on Electrical and Electronics Eng. ELECO'99. Electronics 90-94, Bursa, Turkey, 1-5 December 1999.