MOS-C Realization of KHN Biquad Using Inverting Current Feedback Operational Amplifiers

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Abstract

Kerwin-Huelsman-Newcomb (KHN) biquad topology using the active element called inverting current feedback operational amplifier (ICFOA) is presented. The circuit provides second order lowpass, highpass and bandpass filtering functions simultaneously. The resistors in the filter are realized with MOS transistors by making use of opposite potentials at the input terminals of ICFOA. The resulting circuit contains only transistors and capacitors leading to MOS-C realization. To verify the theoretical analysis, PSPICE simulation results, which are obtained by using CMOS realizations of ICFOA, are included.

1. Introduction

The second generation current conveyor (CCII) has been widely used in the field of analog signal processing since its discovery. Many CCII based configurations synthesizing voltage mode and current mode filtering functions have been presented in the literature [1–3]. Due to its high-impedance output terminal, CCII is more convenient for current mode filters although it has also found applications in voltage mode circuits. Afterwards, another output terminal has been added to this element which is obtained by voltage buffering the high-impedance output terminal. The resulting active element has been called current feedback operational amplifier (CFOA). The CFOA has also found many applications [4] and it has been manufactured commercially (e.g. Analog Devices' AD844). It can also be used as a classical operational amplifier with the advantage of constant gain-bandwidth product. Its low-impedance output terminal gives the possibility to cascade voltage mode circuits.

On the other hand, the inverting second generation current conveyor (ICCII) has been introduced to give further possibilities to the analog designers [5]. Its only difference from CCII is that the input terminals are at opposite potentials. This feature can especially be useful in the synthesis of allpass and notch filters. Some applications of ICCII have been reported in the literature [6–8]. As with CCII, it is not very suitable for voltage mode circuits due to the absence of low-impedance output terminal.

In this paper, we present an active building block called inverting current feedback operational amplifier (ICFOA). It is obtained by adding another output terminal to the ICCII with voltage buffering the high-impedance output terminal as it is done for the classical CFOA. It has been seen that this active element is especially useful in the MOSFET-C realization of voltage mode circuits. Kerwin-Huelsman-Newcomb (KHN) biquad has been given as the application example of this element. The resistors in the circuit are realized using MOSFETs with non-linearity cancellation. The resulting circuit contains only transistors and capacitors leading to MOS-C realization.

2. Description of ICFOA and Its CMOS Realizations

The circuit symbol of ICFOA is given in Figure 1. Its port relations are defined by the following set of equations.

$$\begin{aligned} I_y &= 0 \\ V_x &= -V_y \\ I_z &= \pm I_x \\ V_w &= V_z \end{aligned} \tag{1}$$

where the positive sign in $I_z = \pm I_x$ indicates the positive type inverting current feedback operational amplifier (ICFOA+) and the negative sign indicates the negative type inverting current feedback operational amplifier (ICFOA–).

A CMOS realization of ICFOA+ is shown in Figure 2. It is obtained by cascading the DDCC in [9] (with grounded Y_1 and Y_3 terminals) with the voltage follower in [10]. The circuit is simulated using PSPICE program with 0.35μm CMOS process parameters. The supply voltages are taken as ±2.5V. PSPICE simulation results given in Figures 3, 4, and 5 show the DC characteristics of $V_X - V_Y$, $I_Z - I_X$, and $V_W - V_Z$, respectively, confirming that the CMOS ICFOA+ works properly. Simulation results also give that the port resistances are R_X=63Ω, R_Y=220MΩ, R_Z=200MΩ, and R_W=180Ω.

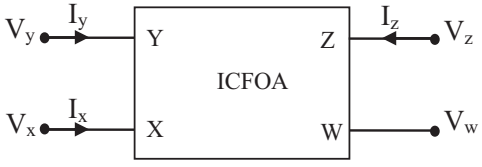

Fig. 1. Circuit symbol of ICFOA

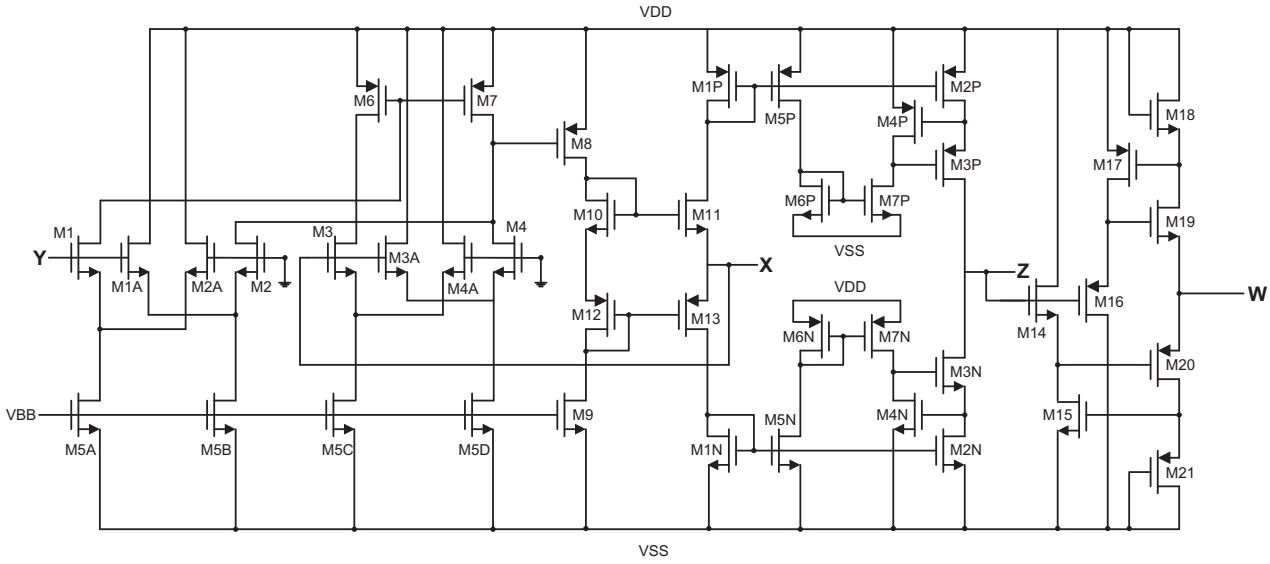

Fig. 2. A CMOS realization of ICFOA+

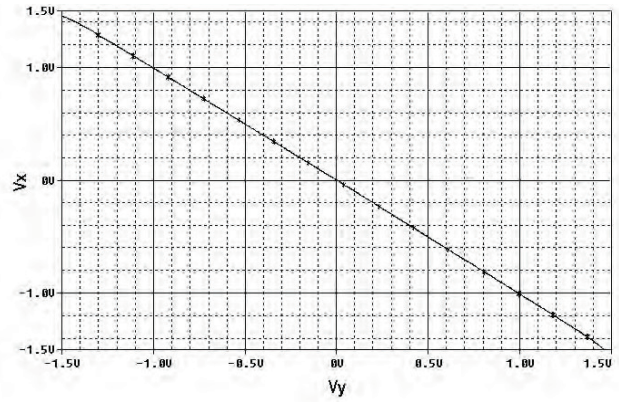

Fig. 3. DC characteristic between V_X and V_Y of the CMOS ICFOA+

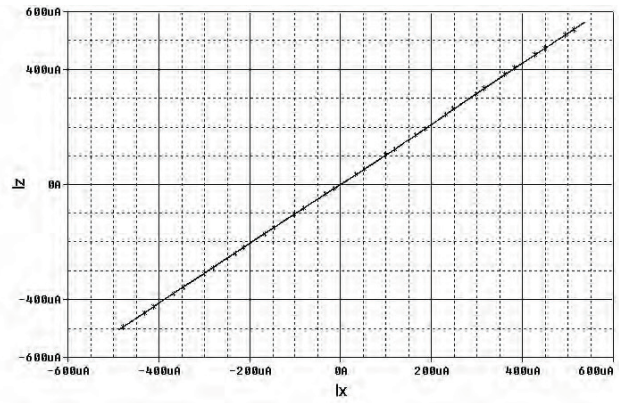

Fig. 4. DC characteristic between I_Z and I_X of the CMOS ICFOA+

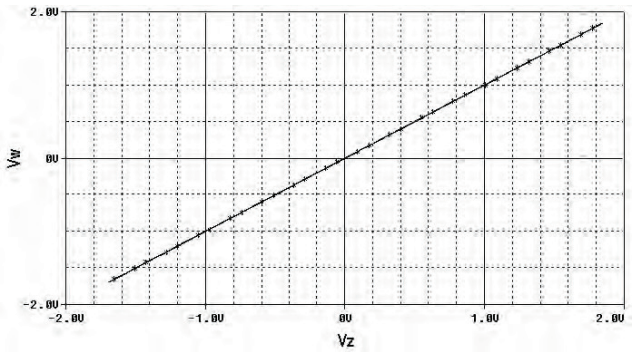

Fig. 5. DC characteristic between V_W and V_Z of the CMOS ICFOA+

A CMOS realization of ICFOA– is shown in Figure 6. It is obtained by cascading the ICCII– in [11] with the voltage buffer in [10]. It is also simulated using PSPICE with the same process parameters and supply voltages. Figure 7 depicts the PSPICE simulation result confirming the I_Z=–I_X relation. The other characteristics for CMOS ICFOA– are similar to those obtained for ICFOA+ which are depicted in Figures 3 and 5.

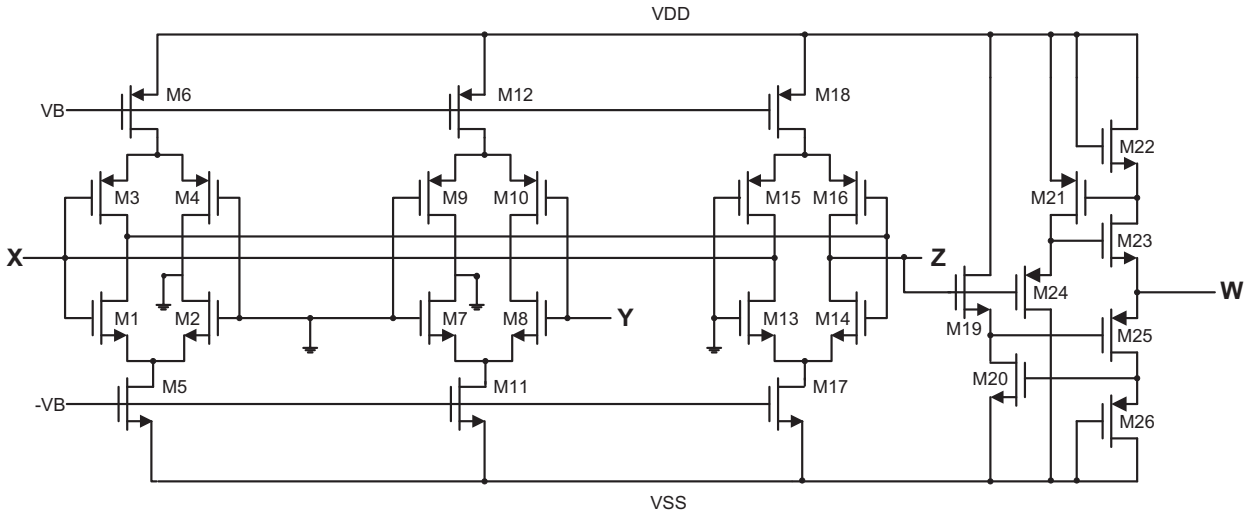

Fig. 6. A CMOS realization of ICFOA–

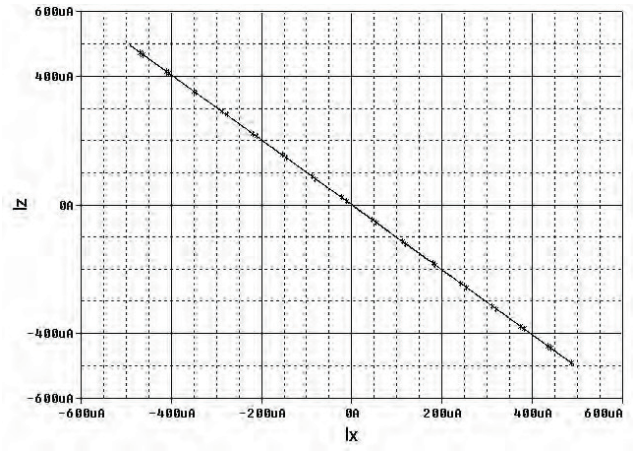

Fig. 7. DC characteristic between I_Z and I_X of the CMOS ICFOA–

3. Kerwin-Huelsman-Newcomb (KHN) Biquad Using ICFOA

Tsividis, et. al. [12] give a technique for the realization of MOS-C based circuits. In this method, a resistor whose terminals connected to the same positive and negative voltage can easily be implemented using a MOS transistor with non-linearity cancellation [12] as shown in Figure 8. ICFOA element introduced in this paper is a good candidate for such type of MOS-C realization since its input terminals are at opposite potentials.

Another method for cancelling nonlinearities was proposed in [13]. A linear resistor has been realized by using parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in Figure 9. The circuit requires depletion mode devices to keep the M_1 transistor on.

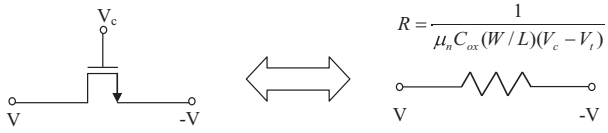

Fig. 8. MOSFET realization of the resistor connected across opposite potentials

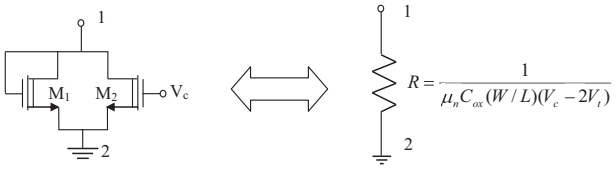

Fig. 9. Parallel connected depletion type MOSFETs realizing the grounded resistor

MOS-C realization of ICFOA based KHN biquad is shown in Figure 10. The transfer functions of lowpass, bandpass and highpass responses of the KHN filter are respectively given by

$$\frac{V_{LP}}{V_{in}} = -\frac{\frac{8R_6}{C_1C_2R_1R_2R_3}}{s^2 + s\frac{4R_6}{C_1R_2R_5} + \frac{8R_6}{C_1C_2R_2R_3R_4}} \quad (2)$$

$$\frac{V_{BP}}{V_{in}} = \frac{s\frac{4R_6}{C_1R_1R_2}}{s^2 + s\frac{4R_6}{C_1R_2R_5} + \frac{8R_6}{C_1C_2R_2R_3R_4}} \quad (3)$$

$$\frac{V_{HP}}{V_{in}} = -\frac{s^2\frac{2R_6}{R_1}}{s^2 + s\frac{4R_6}{C_1R_2R_5} + \frac{8R_6}{C_1C_2R_2R_3R_4}} \quad (4)$$

The natural angular frequency and quality factor can be given by

$$\omega_0 = \sqrt{\frac{8R_6}{C_1C_2R_2R_3R_4}} \tag{5}$$

$$Q = R_5\sqrt{\frac{C_1R_2}{2C_2R_3R_4R_6}} \tag{6}$$

It is clear from the above equations that the circuit simultaneously provides three basic filtering functions, namely lowpass, highpass and bandpass filters. Besides, the gain, quality factor and natural frequency of the filters are independently controllable.

In the simulations, we use the CMOS realizations of ICFOA+ and ICFOA– given in Figures 2 and 6, respectively, together with 0.35μm CMOS process parameters and ±2.5V supply voltages. Also, we take W=4.5μm and L=1.5μm for all transistors realizing the resistors except R_6. We also take V_c=1.65V. Therefore, the resistor values are equal to 2.8 kΩ. R_6 uses depletion type transistors and W=12μm, L=10μm, V_c=10V are selected. So, the resistor value corresponds to 1.38kΩ. The capacitor values are taken as C_1=C_2=100pF. From these values, the theoretical natural frequency is found as 1.13 MHz. The simulated gain responses of second order lowpass, highpass and bandpass filters are given in Figure 11. The simulated natural frequency is equal to 1.11 MHz, which is very close to the theoretical one.

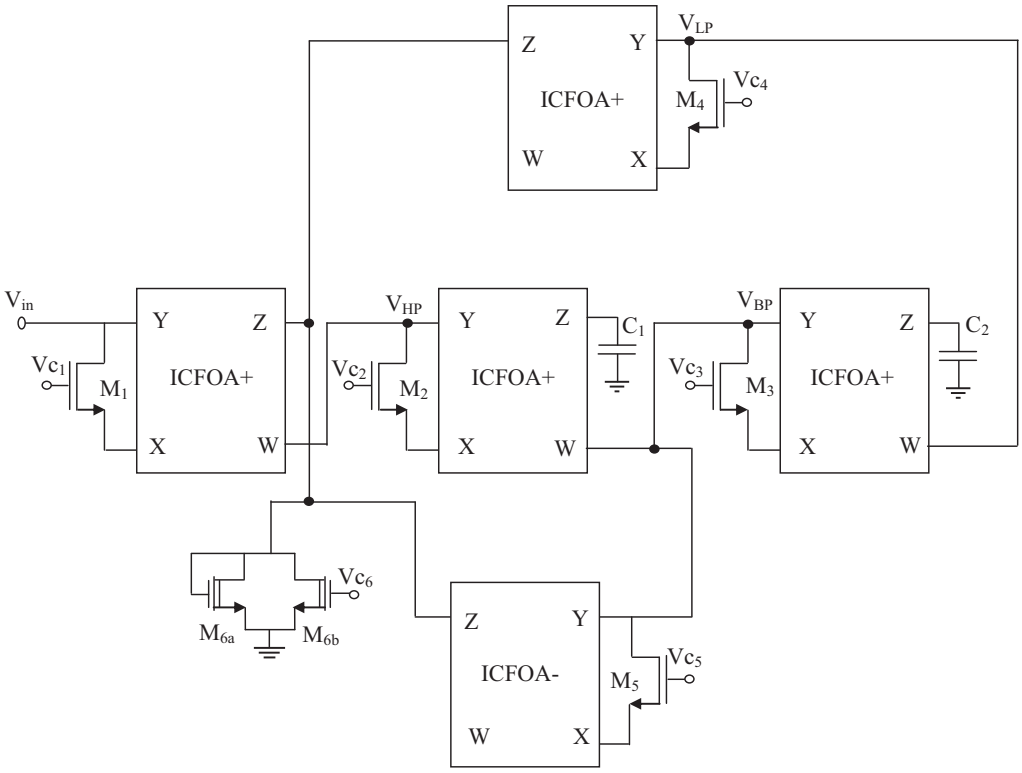

Fig. 10. MOS-C realization of KHN biquad

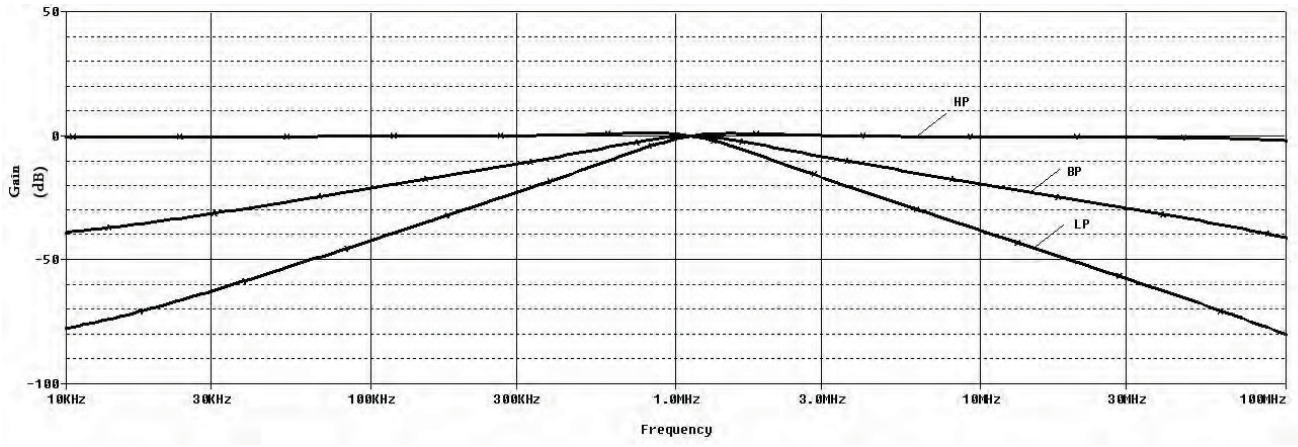

Fig. 11. Simulated gain responses of KHN biquad

4. Conclusion

MOS-C realization of second order lowpass, highpass, bandpass filters using the presented active building block, ICFOA, are given. The circuits can be made fully integrated based on MOS-C realization by making use of inverting voltage copying inputs of ICFOA. One of the output terminals of ICFOA is characterized by low-impedance leading to voltage mode circuits to be cascaded without additional buffers. PSPICE simulation results, which are obtained by using CMOS realizations of ICFOA, verifying the theoretical analysis are included.

5. References

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