NEW HIGH PERFORMANCE CMOS DIFFERENTIAL CURRENT CONVEYOR REALIZATION

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ABSTRACT

New CMOS realization of high performance differential current conveyor (DCCII) is presented. Presented high performance differential current conveyor is a useful analog building block with the advantage of wide bandwidth. It can be directly used with MOS transistors operating in the ohmic region to implement some essential analog functions. As the applications of the presented DCCII, a four quadrant current multiplier and a mixed mode second order bandpass filter are presented. SPICE simulations show that the performance of the DCCII and the multiplier/bandpass-filter are in good agreement with theoretical results.

I. INTRODUCTION

The first generation current conveyor (CCI) was presented by Sedra and Smith in 1968. They presented the second generation current conveyor in 1970. However, a certain work to show that the current conveyor was a more advantageous device than the operational amplifier, couldn't be done during following ten years. So, the current conveyor had been a conceptual device until early 1980s. After innovations in integrated circuit (IC) technology it was seen that the current conveyor can be realized in ICs simply. In the result of these works, it was understood that the circuits which are implemented by using CCIIs have important advantages. Really, many circuit blocks can be implemented by using CCIIs easier than using Op-Amps.

The differential current conveyor (DCCII) is a powerful current-mode building block with properties that make it very suitable for designing all-MOS analog circuits which can be integrated on a single chip. The presented analog block is an extension to the second generation current conveyor presented by Sedra and Smith [1]. Although the CCII can be used to realize many analog functions, the circuits employing the CCII often rely on floating resistors and capacitors which, when integrated on the chip, bring many problems associated with parasitics, area consumption, temperature dependency, etc. The presented differential current conveyor, on the other hand, can be used with MOS transistors operating in the ohmic region to implement the required analog functions where the even and -in some cases- the odd nonlinearities associated with the transistors operating in this mode can be cancelled out.

In this paper, after briefly recalling the basic properties of the differential current conveyor, a new high performance CMOS realization of the suggested block is proposed. Application examples are also supplied, which are four quadrant multiplier cells and mixed mode MOSFET-C continuous time filters.

II. DIFFERENTIAL CURRENT CONVEYOR

The differential current conveyor is a four-terminal analog building block as shown in Figure 1. Describing matrix of the DCCII is given in equation (1).

The MOS realization of the DCCII is shown in Figure 2. All transistors are assumed to be operating in the saturation region.

As shown in Figure 2, the input currents I_{X1} and I_{X2} are applied to the drain of transistors M_{12} and M_{14}, respectively. The Y terminal voltage is applied to the gate of transistors M_2 and M_5. Because of M_1, M_2, M_5 and M_6 are matched transistors, the voltage at Y terminal is conveyed to the terminals X_1 and X_2.

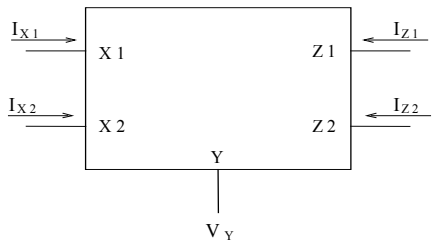

Fig. 1 DCCII symbol

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_{Z1} \\ I_{Z2} \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \\ V_Y \end{bmatrix} \quad (1)$$

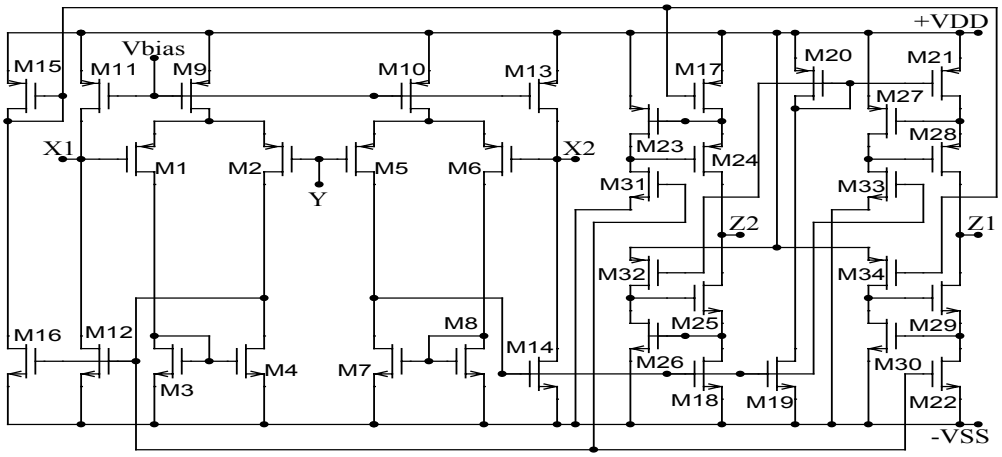

Figure 2 Proposed CMOS DCCII Realization.

The difference between the X_1 and X_2 currents is conveyed to the Z terminals by the mirroring action of transistors M_{15}-M_{18} and M_{19}-M_{22}.

M23-M34 transistors form the accurate active-feedback CMOS cascode current mirrors of the output stages. Active-feedback CMOS cascode current mirrors have very accurate current reflection ratio, while achieving high output impedance. Thus they can be used in high precision analogue integrated circuits, especially in structures where current mode techniques are used [8].

PSPICE simulations have been carried out on the circuit of Figure 2 using MIETEC 0.5µm CMOS process parameters. The supply voltages used are $V_{DD} = V_{SS} = 2.5$ V and the biasing current is adjusted to 50µA. The transistors aspect ratios are given in Table 1. Figure 3 shows the linear relation $I_{Z1} = I_{X1} - I_{X2}$ and $I_{Z2} = I_{X2} - I_{X1}$ between the output current and the input currents. Figure 4 and Figure 5 show the frequency response of differential current conveying property and voltage conveying property of the presented CMOS DCCII shown in Figure 2, respectively.

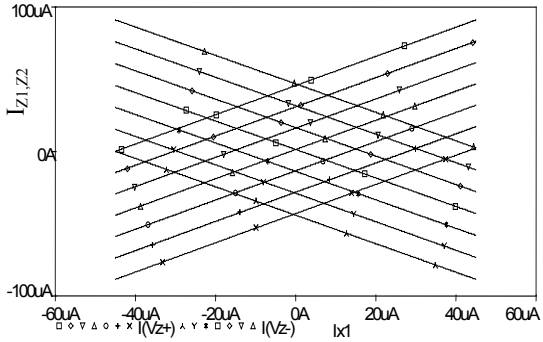

Figure 3 Differential current conveying property of the DCCII**.**

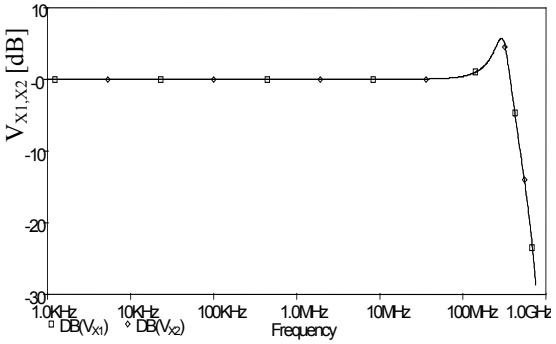

Figure 4 Frequency response of voltage conveying property of the DCCII.

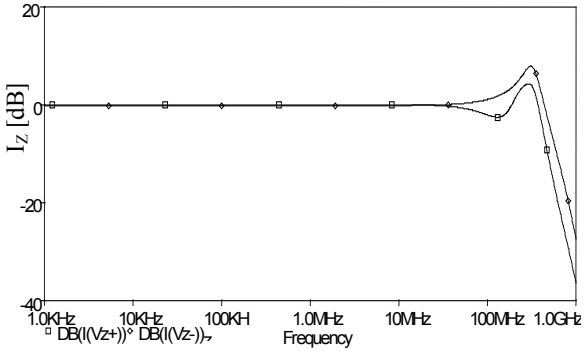

Figure 5 Frequency response of differential current conveying property of the DCCII.

III. APPLICATION EXAMPLES AND SIMULATION RESULTS

FOUR QUADRANT MULTIPLIER CELLS

Multipliers are important circuits for implementing various non-linear functions in analog signal processing. A wide range of analog signal processing applications use analog multipliers and dividers such as adaptive filtering, modulation detection, frequency translation and automatic gain controlling and neural networks [2].

Some multipliers use the quadratic relation between drain current and gate-source voltage of the MOS transistors in the saturation region and others use the MOS transistors in the ohmic region [2].

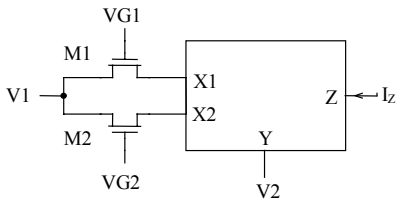

Figure 6 A four quadrant multiplier using the DCCII.

The presented DCCII can be used to realize multiplier/transconductance cells as shown in Figure 6. The transconductance multiplying action is achieved by the transistors M1 and M2 which are operating in the ohmic region [3, 4]. The configuration shown cancels both the even and the odd nonlinearities as discussed next.

The current in the ohmic region is given by:

$$I = K(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_S^2) + a_2(V_D^3 - V_S^3) + ... \quad (2)$$

Since transistors M1 and M2 have equal drain and equal source voltages by the action of the DCCII therefore the output current $I_Z = I_{X1} - I_{X2}$ is given by:

$$I_Z = K(V_{G1} - V_{G2})(V_1 - V_2) \quad (3)$$

Thus the cells can be used as a four quadrant multiplier/transconductance. Figure 7 represents the multiplier output current when the voltage V1 is scanned for different values of the differential gate voltage. An amplitude modulation example is supplied in Figure 8 where the modulating signal is a sine-wave with f = 50 kHz and the carrier is a sine-wave with f = 1MHz.

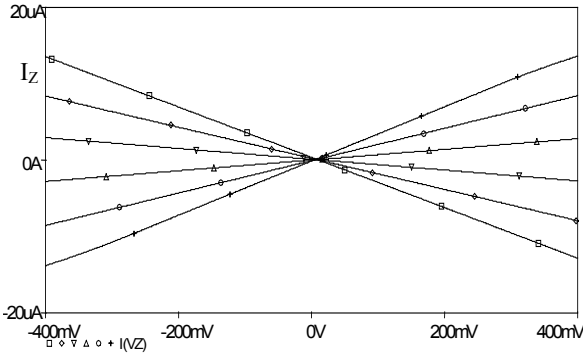

Figure 7 PSPICE simulation of the multiplier.

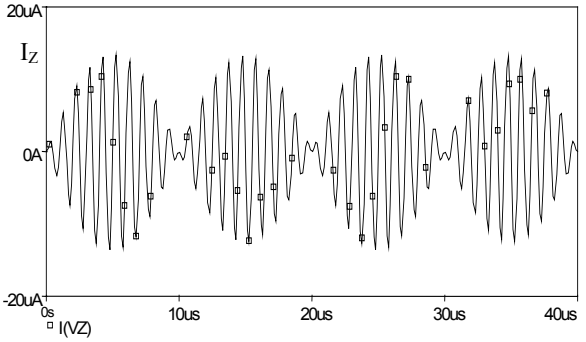

Figure 8 Amplitude modulation example with DCCII based analogue multiplier

MIXED MODE MOSFET-C CONTINUOUS TIME FILTERS

Integrated continuous time filters are now widely accepted in industry [5, 6] where they are used in applications involving direct signal processing especially for medium dynamic range applications in cases where high speed and/or low power dissipation are needed. The DCCII is a suitable building block for the realization of MOSFET-C current mode filters. Although MOSFET-C filters can be implemented in the voltage mode using op-amps, they usually suffer from the finite gain-bandwidth product of the op-amps which limit the frequency range.

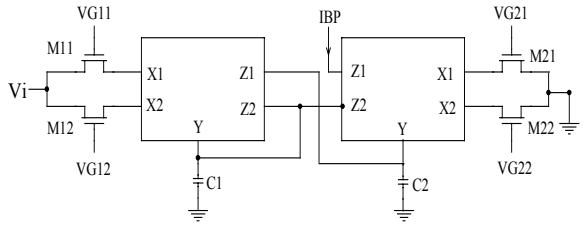

Figure 9 A mixed mode second order band-pass filter.

The circuit shown in Figure 9 represents a mixed mode second order bandpass filter based on the DCCII. Transistors M11, M12, M21 and M22 are operating in the ohmic region with their nonlinearities canceled out as shown in the previous section. The input to this filter section is a voltage while the output is a current and the transfer function is given by:

$$\frac{I_{BP}}{V_i} = \frac{s\frac{G_1G_2}{C_2}}{s^2 + s\frac{G_1}{C_1} + \frac{G_1G_2}{C_1C_2}} \tag{4}$$

where

$$G_1 = K_1 (V_{G11} - V_{G12}) \tag{5}$$

$$G_2 = K_2 (V_{G21} - V_{G22}) \tag{6}$$

The bandpass response of the above filter is shown in Fig. 10 with C1 = C2 = 10pF, $V_{G11} = V_{G21} = 2V$, $V_{G12} = V_{G22} = 1V$.

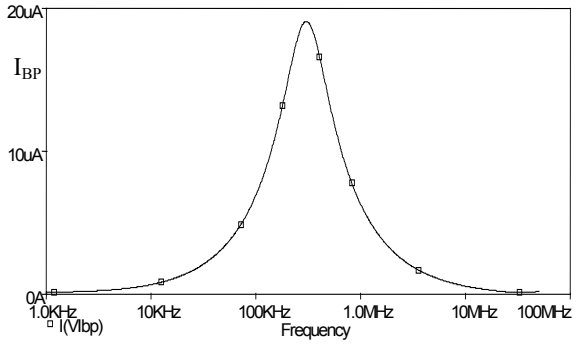

Figure 10 Frequency response of the band-pass filter.

Table1 Aspects of the MOSFETs in the proposed DCCII

Transistor	Aspect Ratio (W/L)
M1, M2, M5, M6	25μm/1μm
M3, M4, M7, M8	5μm /1μm
Other PMOS	50μm /1μm
Other NMOS	10μm /1μm

IV. CONLUSION

A new current mode analog building block is presented. CMOS circuit realization of the block is given. It is then shown the properties of the block are suitable for designing current mode circuits using CMOS technology. SPICE simulations show that the performance of the DCCII and the multiplier and/or bandpass-filter are in good agreement with theoretical results.

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