SIMPLE AND ACCURATE NON-LINEAR MACROMODEL FOR FOUR TERMINAL FLOATING NULLOR (FTFN)

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ABSTRACT

This paper presents a simple and accurate non-linear four terminal floating nullor (FTFN) macromodel. The FTFN characteristics are simulated by using new macromodel and compared with the simulation results obtained by SPICE device models. The results show that the proposed FTFN macromodel represents the CMOS FTFN approximately with the same accuracy of semiconductor SPICE device models but with a significantly reduced computer time.

1.INTRODUCTION

Integrated circuit simulators have proven to be useful tool for IC design engineers. Since any analysis is only as accurate as the model used, modelling of semiconductor devices and IC building blocks is an important factor in circuit simulation. With the increasing popularity of VLSI systems, the demand for simplified but still accurate models which handle analogue subsystems is continuously growing. Analogue IC designer ask for models that allow to combine as much accuracy as possible with a maximum simulation speedup. Resorting to macromodels instead of device model is a widely used strategy which allows the designer to reduce the high computation time required when simulating complex systems. A good macromodel must fulfil two basic requirements: namely, it must be as simple as possible and at the same time simulate circuits with maximum possible accuracy [1-3]. On the other hand, the four terminal floating nullor (FTFN) has been also receiving considerable attention recently as it has been shown that an FTFN is the very flexible and versatile building block in active network synthesis. This leads to growing attention in design of amplifiers, gyrators, inductance simulators, oscillators and filters which use FTFN as an active element [4-11]. Up to now, several op-amp, OTA and CCII macromodels have been proposed [1-3]. Hovewer, there is no any macromodel in the literature to represent FTFN non-idealities and to provide the advantages explained above using the macromodels. The purpose of the study is to introduce a simple and accurate non-linear FTFN macromodel which is suitable for simulation of FTTN-based analogue signal processing circuits.

2. THE FOUR TERMINAL FLOATING NULLOR

The circuit symbol of the FTFN is shown in Figure 1. Circuit example for CMOS realisation of the FTFN is illustrated in Figure 2 [12]. The behaviour of the ideal FTFN is characterised by the following port relations;

$$\begin{aligned} V_x &= V_y \\ I_x &= I_y = 0 \\ I_z &= I_w \end{aligned} \qquad (1)$$

Taking into consideration the FTFN non-idealities the port relations in equation (1) can be expressed as follows;

$$\begin{aligned} V_x &= \beta V_y \\ I_z &= \alpha I_w \end{aligned} \qquad (2)$$

where $\beta = 1 - \varepsilon_V$, and ε_v denotes voltage tracking error and $\alpha = 1 - \varepsilon_i$, ε_i denotes current tracking error of the FTFN. The FTFN is ideally a transconductance amplifier featuring infinite gain and two output currents. The basic equation describing its operation $I_w=I_z=G_m.(V_x-V_y)$. For a finite open loop transconductance gain G_m, the difference between two differential voltages increases as G_m decreases.

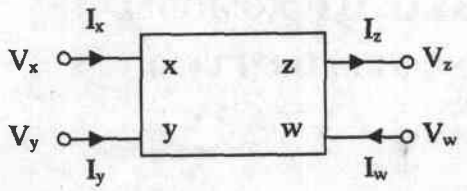


Figure 1: Circuit symbol of the FTFN

3.MACROMODEL DEVELOPMENT

The proposed macromodel for the FTFN structure is shown in Figure 3. With the suitable choise of parameters and elements, the configuration models the circuit behaviour for non-linear DC, AC and large signal transient reponses accurately. The proposed macromodel is subdivided into three stages, namely the input stage, the inter-stage and the output stage

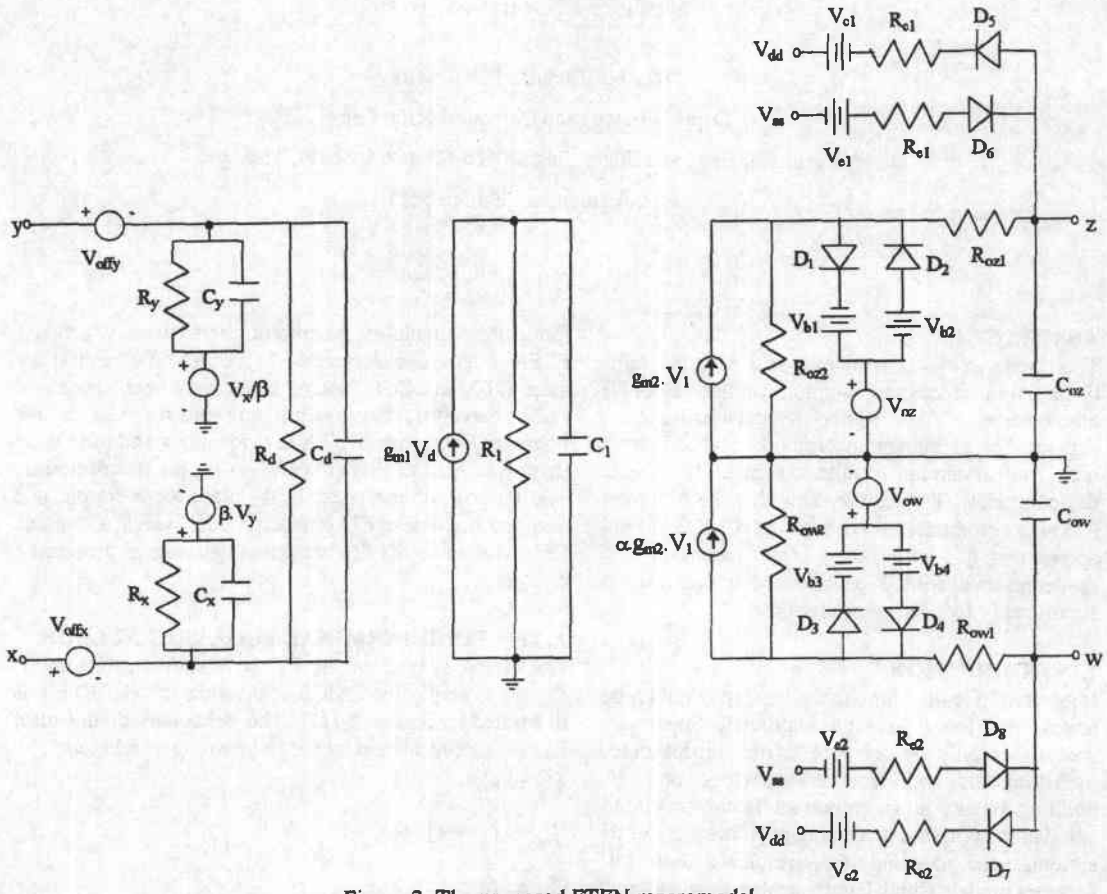


Figure 3: The proposed FTFN macromodel

Table 1: Model parameters of derived FTFN macromodel

Parameter	Value	Parameter	Value	Parameter	Value
V_{offx}	1mV	β	1	R_{c1}	1KΩ
V_{offy}	1mV	R_1	1Ω	R_{c2}	1KΩ
V_{b1}	5.6V	C_1	100p	R_{e1}	1KΩ
V_{b2}	5.6V	R_d	10^{12}Ω	R_{e2}	1KΩ
V_{b3}	5.6V	C_d	1pF	g_{m1}	1 A/V
V_{b4}	5.6V	R_x	10^{12}Ω	g_{m2}	180 mA/V
V_{c1}	1.2V	C_x	1p	R_{oz1}	18KΩ
V_{c2}	1.2V	R_y	10^{12}Ω	R_{oz2}	2KΩ
V_{e1}	[illegible]	C_y	1pF	R_{ow1}	18KΩ
V_{e2}	1.6V	C_{oz}	0.1pF	R_{ow2}	2KΩ
α	1	C_{ow}	0.1pF		

The input stage produces the necessary linear and no-linear differential mode input characteristics and consist of capacitors C_x , C_y C_d , resistors R_x ,R_y R_d, independent voltage source V_{offx}, V_{offy} and voltage-controlled voltage sources V_x , V_y .The voltage source V_{os} is introduced for modelling of input voltage offset voltage. β represents voltage tracking error of the FTFN. C_x , C_y , C_d and R_x ,R_y R_d represent input capacitances and resistances of FTFN respectively. Since the input resistance of the FTFN can be assumed practically infinite, R_x ,R_y and R_d are fixed $10^{12}\Omega$ to prevent numerical problem in simulation. The inter-stage contains a unity gain connection and introduced for high frequency dominant pole. To introduce this pole into the frequency response the resistance R_1 is chosen as $1/g_{m1}$. The output stage consist of two current controlled current sources, output capacitances and output resistances. The ratio of transconducante of current controlled current source represents current tracking error of the FTFN as α. The non-linearity of the FTFN caused by voltage and current limiting at the terminal z and w modelled by introducing additional elements. The voltage swings at z ant w terminal are limited by voltage source-resistor-diode combinations V_{C1}, D_5, R_{C1} - V_{E1}, D_6, R_{E1} and V_{C2}, D_7, R_{C2} - V_{E2}, D_8, R_{E2} .To represent current limiting voltage dependent voltage source-diode-voltage source combinations V_z, V_{b1},V_{b2}, D_1, D_2 and V_w, V_{b3},V_{b4}, D_3, D_4 are incorporated to the circuit. The resistors R_{C1}, R_{E1}, R_{C2} and R_{E2} are introduced resistive elements to the circuit model which adjust the slope of the DC voltage transfer characteristic $V_z=V_z(V_{in})$, $V_z=V_z(V_{in})$ at the boundaries of the linear operation region by using piecewise linear approximation as used before in OTA and CCII models in reference [2-3]. Model parameters of derived FTFN macromodel are given in Table 1.

4.COMPRASION WITH SEMICONDUCTOR DEVICE MODELS

The accuracy of the FTFN macromodel is demonstrated by comparing the simulated FTFN characteristics with simulation result obtained from semiconductor device model. The CMOS FTFN shown in Figure 2 was chosen for demonstration[12]. The macromodel parameters of the derived macromodel were determined from SPICE simulations using device models and given in Table 1. The supply voltages were taken as V_{DD}=5V V_{SS}=-5V. MOS transistor aspect ratio is given in Table 2. Device model parameters used for SPICE simulations are taken from TUBITAK YITAL 3μm CMOS process.

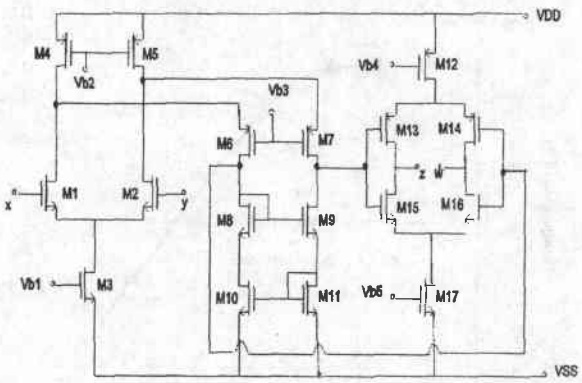


Figure 2: Circuit schematic of the CMOS FTFN

To demonstrate the accurate representation of non-linear behaviour of the CMOS FTFN, the voltage and current DC transfer characteristics obtained SPICE simulation using device models and newly introduced macromodel are illustrated in Figure 4. The frequency responses of the FTFN versus voltage-gain and transconductance are shown in Figure 5. It can be easily observed from Figures 4-5 that non-linear DC transfer characteristics and the frequency responses obtained from SPICE simulation by using device models and newly introduced FTFN macromodel are in good agreement with each other.

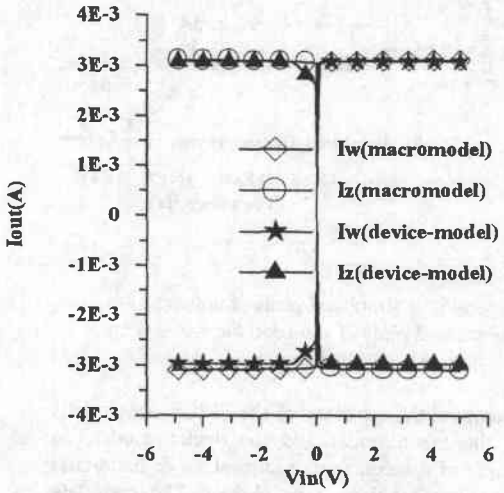
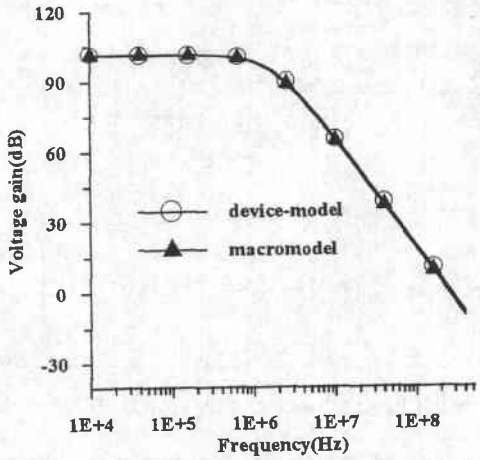
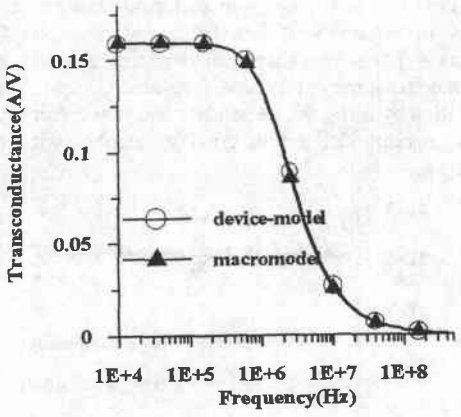


Figure 4:Simulated plots of DC current curves



(a)



(b)

Figure 5: a)simulated plots of voltage gain b) simulated plots of transconductance, versus frequency

To compare the accuracy of the SPICE simulations with the macromodel and the device model, an example of a second-order current-mode band-pass active filter topology was chosen. The complete filter circuit is shown in Figure 6. Passive components were chosen as $C_1=C_4=0.5nF$, $R_1=3K\Omega$, $R_2=1K\Omega$ which result in 104kHz center frequency. SPICE simulations for AC and transient analysis were performed using device models and macromodels. Simulations to obtain the frequency and transient responses of the current-mode band-pass filter were performed by using both corresponding macromodel and the CMOS FTFN on a Pentium-II Celeron 300A computer, and resulting computer times are given in Table 3. The frequency response of the filter obtained from SPICE simulations with device model and macromodel is shown in Figure 7. It is obvious from the Table 3 that the computer time needed for SPICE simulation was reduced considerably by the use of proposed macromodel.

Table 2: Dimensions of MOS devices for proposed circuits

Transistor	W(μm)	L(μm)
M1	24	3
M2	24	3
M3	100	3
M4	100	3
M5	100	3
M6	100	3
M7	100	3
M8	100	3
M9	100	3
M10	100	3
M11	100	3
M12	300	3
M13	100	3
M14	100	3
M15	100	3
M16	100	3
M17	300	3

Table 3: Computer times in seconds needed for SPICE simulations

Analysis type	AC	Transient
Macromodel	6.54	11.03
Device model	12.35	29.11

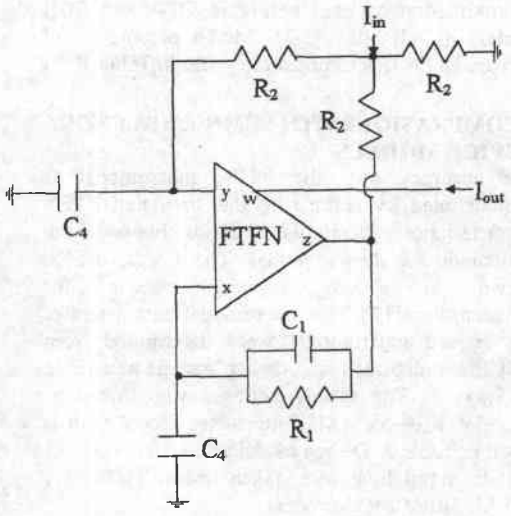


Figure 6: The current-mode band-pass filter

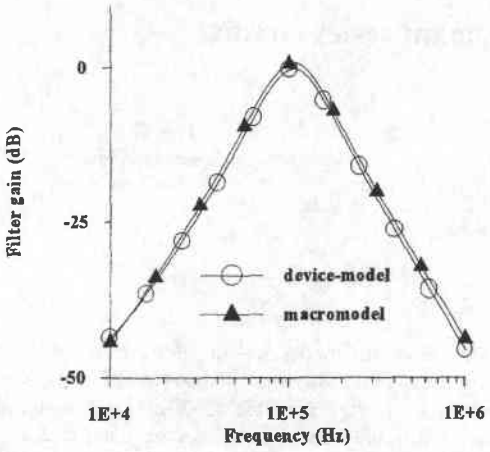


Figure 7: Frequency response of the filter

5.CONCLUSIONS

A simple and accurate non-linear macromodel is proposed in this paper. The derived macromodel is especially suitable for SPICE simulation of FTFN-based analogue signal processing circuit. The FTFN characteristics are simulated by using new macromodel and compared with the simulation results obtained by SPICE device models. The results show that the proposed FTFN macromodel represents the FTFN approximately with the same accuracy of semiconductor SPICE device models but with a significantly reduced approximately %50 computer time .

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