# An 8-bit 50-MS/s CMOS DIGITAL-ANALOG CONVERTER

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*Abstract-* **In this paper a new 8-bit 50-Msample/s CMOS digital-to-analog converter (DAC) is presented. The circuit employs 9 operational transconductance amplifiers (OTAs) and CMOS transistors as switching circuit. The proposed DAC is simulated using SPICE simulation program with 3μm CMOS technology. Simulation results shows verify good performance of the circuit.**

## I. INTRODUCTION

The ability to convert digital signals to analog is very important in applications such as direct digital synthesis (DDS) techniques.

On the other hand, there are several observations worthy of discussion regarding the behavior of OTA-based circuits in comparing with their equivalent op amp-based counterparts.

In the case of op amp building blocks, specific voltage gains or transfer functions are realized by surrounding the op amp with large amounts of external negative feedback in order to significantly desensitize the closed-loop performance to the characteristics of the open-loop op amp. In fact, for ideal operation, the closed loop performance of these circuits is independent of the op amp's open-loop behavior; determined only by the external passive components in the feedback network. In the words, the open-loop gain of the op amp is a second-order effect in these circuits. Moreover, the feedback guarantees linear operation over a wide range of conditions, in spite of the op amp's very high open-loop gain. In contrast, OTA building blocks use no external feedback and their transfer functions depend directly on the transconductance parameter ($g_m$) of the OTA. The strategy for OTA-based circuits and systems places far greater emphasis on custom design, optimization, and control of the OTA-parameters [1].

Although a number of CMOS DACs have been published [2-4], they have complex circuit structure.

In this paper, a simple 8-bit OTA-based DAC configuration is presented. The proposed circuit uses only active elements and is quite suitable for integration.

## II. OTA MODEL

The symbol used for the OTA is shown in Fig. 1, along with the ideal small signal equivalent circuit. An ideal OTA is an infinite bandwidth voltage-controlled current source, with an infinite input and output impedance. The port relation of an OTA can be characterized by

$$I_o = g_m (V^+ - V^-) \tag{1}$$

Note that $g_m$ (transconductance gain) is a function of amplifier bias current, $I_B$. For the case of OTAs using MOS transistors in saturation the $g_m$s are proportional to $\sqrt{I_B}$ ; for MOS transistors operating in weak inversion or bipolar transistors the $g_m$s are directly proportional to $I_B$.
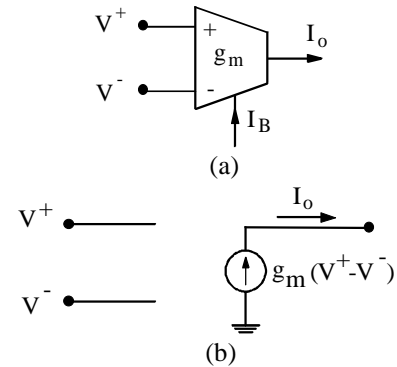


Fig. 1. (a). The OTA symbol. (b). Ideal model.

As shown in the model, the input and output impedances in the model assume ideal value of infinity. However the actual model of the OTA is more complex as shown in Fig. 2.
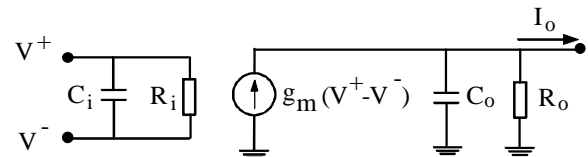
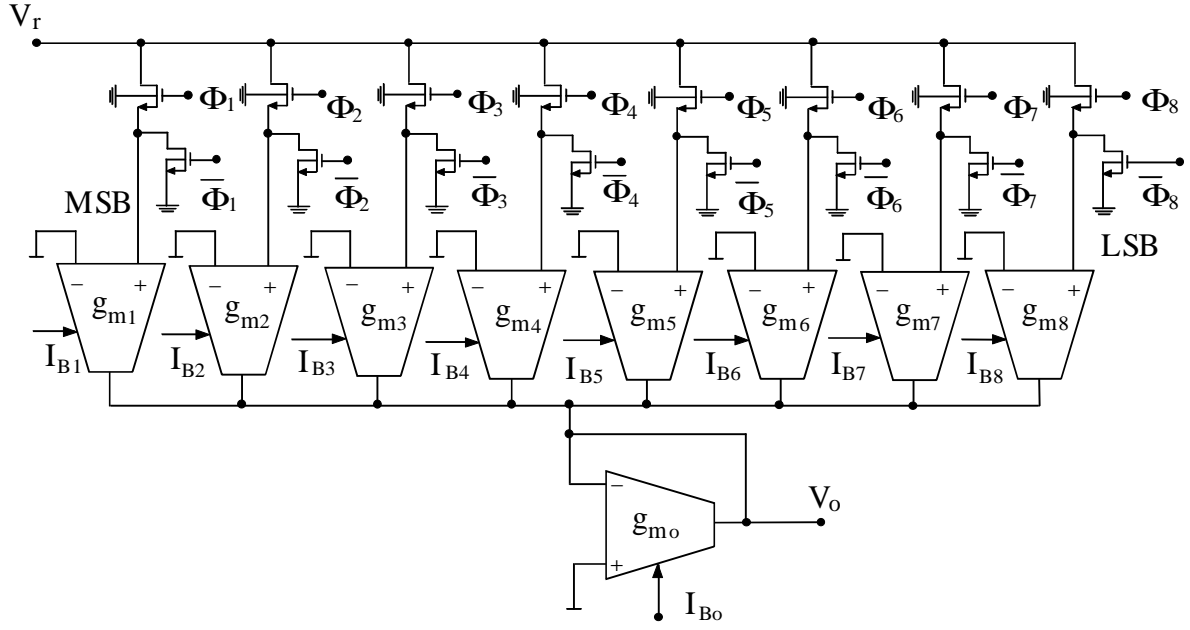

Fig. 2. Non-ideal model of the OTA.

Fig. 3. The proposed 8-bit DAC.

## III. PROPOSED DAC

The proposed 8-bit DAC is shown in Fig. 3. The circuit is composed of 9 OTAs and a set of MOS transistors for. The MOS transistors at the input of the OTAs operate as binary switches. The inputs are a digital word of 8 bits ($\Phi_1$, $\Phi_2$, $\Phi_3$, $\Phi_4$, $\Phi_5$, $\Phi_6$, $\Phi_7$, $\Phi_8$) and a reference voltage $V_r$. The invert of the input code ($\overline{\Phi}_i$, I=1,2…8) along with parallel MOS transistors force the parasitic capacitors of the OTAs to be discharged when the serial MOS transistors are tuned off.

The output voltage of a DAC must be in form of

$$V_{out} = K V_r D \qquad (2)$$

where K is a scaling factor and the digital word D (input word) is given as

$$D = \Phi_1 2^{-1} + \Phi_2 2^{-2} + \Phi_3 2^{-3} + \cdots + \Phi_8 2^{-8} \quad (3)$$

Routine analysis of the proposed 8-bit DAC yields

$$V_{out} = \sum_{i=1}^{8} \frac{g_{mi}}{g_{mo}} \Phi_i V_r \qquad (4)$$

By selecting

$$g_{mi} = \frac{g_{mo}}{2^i}, \qquad (i=1,2…8) \qquad (5)$$

where $g_{mo}$ is the transconductance of the output OTA, the output voltage of the circuit will be in form of equation (2).

## IV. SIMULATION RESULTS

The performance of the circuit is verified using SPICE simulation program. The OTAs are designed using the symmetrical CMOS OTA structure shown in Fig. 3 [5]. The supply voltages were chosen as $V_{DD} = 5V$ and $-V_{SS} = -5V$. The aspect ratios of the MOS transistors are given in Table 1. The MOS transistors were simulated using standard 3µ model parameters [1] given in Table 2.

The transconductance of this OTA is given by [1]

$$g_m = B \sqrt{2 K'_n . I_B . \left( \frac{W}{L} \right)_1} \qquad (6)$$

in which $(W/L)_1$ is the aspect ratio of the input transistors; $K'_n$ is the transconductance parameter for an $n$ MOS in saturation. The parameter B is the current multiplication factor of the OTA. Different values for the bias current ($I_B$) and parameter B of the OTAs are selected so that results in the transconductance values ($g_m$s) given in Table 3. The transconductance of the output OTA ($g_{mo}$) is selected as $g_{mo}$=7mS. The transient analysis of the proposed DAC is performed using SPICE simulation program. The output voltage of the proposed 8-bit DAC sampling a 390.625kHz digital ramp waveform input signal at rate of 50Msample/s. The input code differs from 00000000 to 11111111 regularly. Figure 5 shows the LSB (least significant bit), MSB (most significant bit) and analog output of the DAC. It is observed that the analog output changes from 0 to 5 volts and agrees quite well with theoretical analysis. The settling time of the converter is less than 10nS.
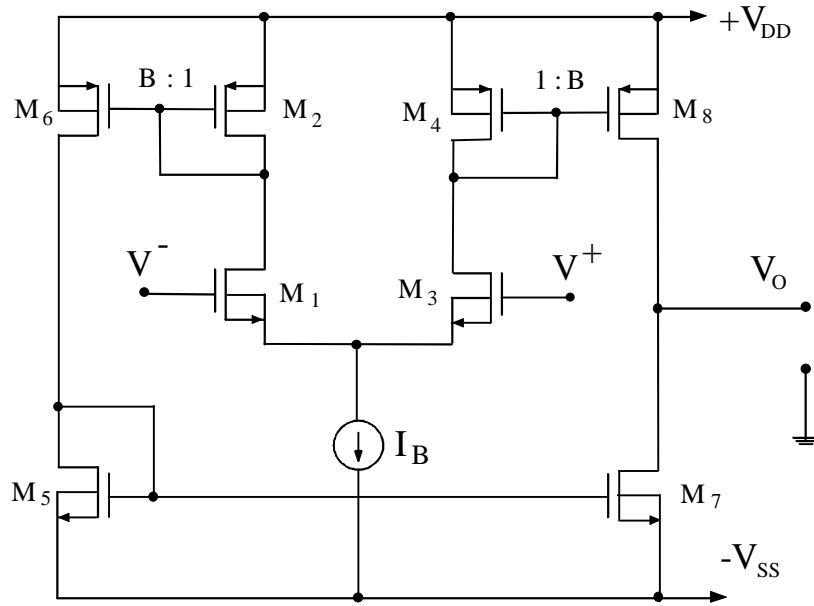
Fig. 4. Symmetrical CMOS OTA structure used in SPICE simulation.

Table 1. Dimensions of MOS transistors used in CMOS OTA for SPICE simulation.

| Transistor | $W$ (μm) | $L$ (μm) |
|------------|----------|----------|
| M1 | 30 | 3 |
| M2 | 12 | 3 |
| M3 | 30 | 3 |
| M4 | 12 | 3 |
| M5 | 12 | 3 |
| M6 | 36 | 3 |
| M7 | 12 | 3 |
| M8 | 36 | 3 |
| M9 | 45 | 3 |

Table 2. The model parameters of standard 3μm CMOS technology used for SPICE simulation.

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.MODEL NM NMOS LEVEL 2 VTO=0.9 KP=50E-6 GAMMA=0.30 PHI=0.70 CGSO=1.76E-10
+ CGDO=1.76E-10 CJ=0.7E-4 MJ=0.5 CJSW=3.9E-10 MJSW=0.33 JS=1E-3 TOX=42.5N
+ NFS=1E11 LD=0 UCRIT=1E4 RSH=25 LAMBDA=0.019

.MODEL PM PMOS LEVEL 2 VTO=-0.9 KP=17E-6 GAMMA=0.50 PHI=0.69 CGSO=2.8E-10
+ CGDO=2.8E-10 CJ=3.3E-4 MJ=0.5 CJSW=4.4E-10 MJSW=0.33 JS=1E-3 TOX=42.5N
+ NFS=1E11 LD=0 UCRIT=1E4 RSH=25 LAMBDA=0.005

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Table 3. Transconductance values of the OTAs

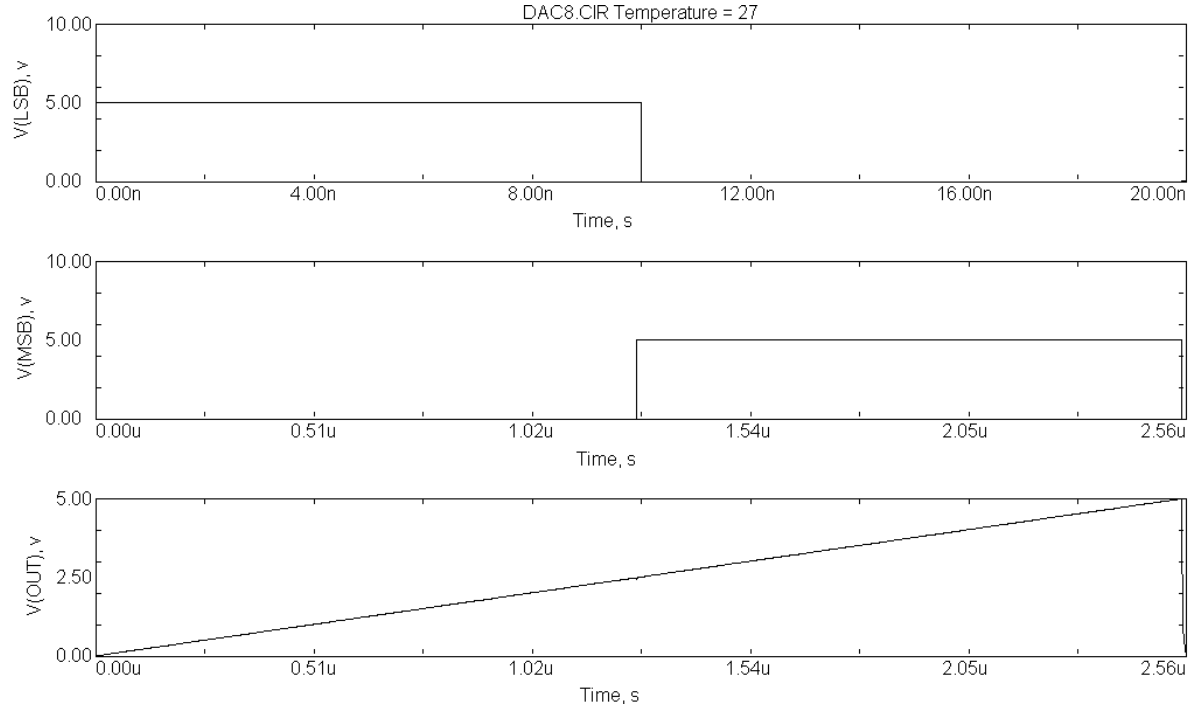| $g_{mi}$ | Value (mS) | $g_{mi}$ | Value (mS) |
|----------|------------|----------|------------|
| $g_{m1}$ | 3.5 | $g_{m5}$ | 0.218 |
| $g_{m2}$ | 1.75 | $g_{m6}$ | 0.109 |
| $g_{m3}$ | 0.875 | $g_{m7}$ | $5.45\times10^{-2}$ |
| $g_{m4}$ | 0.4375 | $g_{m8}$ | $2.72\times10^{-2}$ |

DAC8.CIR Temperature = 27

Fig. 5. Digital input (LSB, MSB) and analog output waveforms of the proposed DAC.

## V. CONCLUSIONS

In this paper a new 8-bit CMOS DAC has been presented. The presented DAC is constructed using only active elements, which makes it suitable for integration. The performance of the DAC is tested using SPICE simulation program. The conversion rate of the proposed DAC is 50 Msample/s with settling time less than 10ns.

## REFERENCES

[1]     K. R. Laker, and W.M.C. Sansen, Design of Analog Integrated Circuits and Systems: McGraw-Hill, 1994.

[2]     T. Miki, Y. Nakamura, Y. Nishikawa, K. Okada, and Y. Horiba, " A 10bit 50-MS/s CMOS D/A converter with 2.7 power supply," in Proc. *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 1992, pp. 92−93.

[3]     D. Reynolds, " A 320MHz CMOS triple 8 bit DAC with on-chip PLL and hardware cursor," *IEEE J. Solid-state Circuits*, vol. 29, pp. 1545−1551, Dec. 1994.

[4]     L. S. Y. Wong, C. Y. Kwok, and G. A. Rigby, " A 1-V CMOS D/A converter with multi-input floating-gate MOSFET," *IEEE J. Solid-state Circuits*, vol. 34, pp. 1386−1390, Oct. 1999.

[5]     C. Acar, F. Anday, and H. Kuntman, " On the realization of OTA-C filters," *International Journal of Circuit Theory and Applications*, vol. 21, pp. 331−341, 1993.