A New LVI Assisted PSPWM DC-DC Converter

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Abstract

In this study, a new Phase Shifted Pulse Width Modulated (PSPWM) full bridge isolated DC-DC converter is proposed. In the proposed converter, the resonant inductor is replaced with Linear Variable Inductor (LVI), and controlled with output current. The new converter has many advantages over recently developed PSPWM DC-DC converters in terms of control simplicity and efficiency. The soft switching operation range is wide and dependency of ZVS operation to the load current is low. At low current levels the required energy for ZVS operation is obtained easily because the value of LVI is large enough. The value of LVI decreases linearly with increasing current. At high current levels parasitic resonance and duty cycle loss are decreased. By selecting the range of the LVI properly, dead time control between gate drive signals of the IGBTs in the same leg is not required. A single phase 160A inverter arc welding machine is implemented with the proposed converter. The experimental results taken from the converter shows the feasibility of the proposed method.

Keywords : DC-DC Converters, Soft Switching, ZVS, PSPWM Converter, Linear Variable Inductor (LVI).

1. Introduction

It is required to use soft switching techniques in order to reduce switching losses, current and voltage stresses; consequently, increasing circuit efficiency, power density and decreasing electromagnetic interference in dc-dc converters [1-4]. In the full bridge (FB) isolated dc-dc converters, the switching losses and the parasitic resonances between the parasitic capacitance of the power switches and the transformer leakage inductance reach very high values. In these converters, by means of phase shifting (PS) method, a quasi-resonance is created between the parasitic capacitance of the power switch, and the leakage inductance of the transformer. The parasitic capacitance energy is discharged by the leakage inductance and the IGBT turns on with ZVT. It is possible to encounter many studies in the literature about these converters and solving the problems of them [5-14].

The required energy for discharging the parallel capacitor is supplied from the load current at the leading leg of the PSPWM converter. But, at the lagging lag, soft switching is not achieved at no-load and at light load conditions. Most of the recent researches on PSPWM converters are mainly concentrated to solve the problems of the lagging lag [11-14].

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In this study, a new method is proposed to solve the problems at the lagging lag. The resonant inductor in the PSPWM converter is replaced with linear variable inductor (LVI), and controlled with output current. The proposed converter has many advantages over recently developed PSPWM DC-DC converters in terms of control simplicity and efficiency. The soft switching operation range is extended and dependency of ZVS operation to the load current is decreased. At low current levels the required energy for ZVS operation is obtained easily because of the high value of LVI. Parasitic resonances and duty cycle loss that occur at high current levels are reduced. By selecting the range of the LVI properly, dead time control between gate drive signals of the IGBTs in the same leg is not required. A single phase 160A inverter arc welding machine is implemented with the proposed converter. The experimental results taken from the converter shows the feasibility of the proposed method.

2. Proposed PSPWM Converter

The proposed PSPWM converter is shown in Fig.1. The converter consists of four IGBTs (Q1-Q4) with reverse diodes (D1-D4), parallel snubber capacitors (C1-C4), high frequency transformer, dc blocking capacitor (Cs), resonance inductor (Ls, LVI), two output rectifier diodes (Do1 and Do2) and output filter (Lo). In order to decrease turn off losses of the IGBTs, high valued parallel snubber capacitors (C1=C2=10 nF) are used in the converter. The maximum and minimum values of the LVI are determined in order to discharge snubber capacitors at minimum and maximum output currents, respectively.

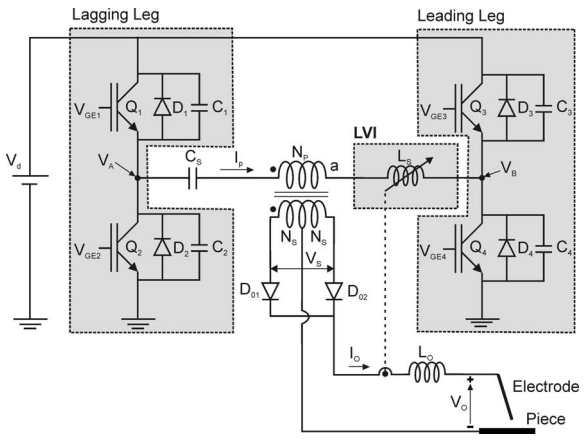

Fig.1. LVI controlled PSPWM DC-DC converter for arc welding applications.

Lagging lag transition in the PSPWM converter shown in Fig.2 consists of two intervals. In the first interval, parallel

capacitor voltage v_{Cp} reaches from zero to V_d and I_p falls from I_{p0} to I_{p1} in t_{ZVS} duration. V_{GE2} is applied after t_{ZVS} duration. t_{ZVS} and I_{p1} are obtained as

$$C_P = C_1 // C_2 \quad (1)$$

$$t_{ZVS} = \sqrt{L_s C_p}\, \arcsin \frac{V_d}{I_{p0}} \sqrt{\frac{C_p}{L_s}} \quad (2)$$

$$\frac{1}{2} L_s (I_{p0}^2 - I_{p1}^2) = \frac{1}{2} C_p V_d^2 . \quad (3)$$

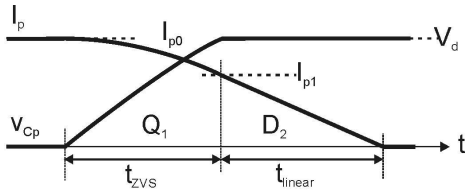

Fig. 2. Lagging leg transition intervals

In the second interval, negative voltage is applied to L_s and current falls to zero linearly. This duration is given as

$$t_{linear} = L_s \frac{I_{p1}}{V_d} . \quad (4)$$

The change of the primary current from I_{p0} to 0 occurs in t_{P0} duration. The dead-time t_{d12}, required for Q_1 and Q_2 IGBTs should provide

$$t_{ZVS} < t_{d12} < t_{P0} \quad (5)$$

$$t_{P0} = t_{ZVS} + t_{linear} . \quad (6)$$

If $t_{d12} > t_{P0}$, then current changes direction, reverse resonance starts and Q_2 turns on with hard switching. The energy of the snubber capacitor is dissipated on the transistor. The minimum current level I_{pmin} for ZVS is calculated as,

$$I_{pmin} = V_d \sqrt{\frac{C_p}{L_s}} . \quad (7)$$

Before lagging leg transition Q1 and D3 conducts. Lagging leg transition starts when the drive signal V_{GE1} is removed. Equivalent parallel capacitor C_p is charged from zero to V_d and the current is commutated to D_2 if there is enough energy in the LVI. For the complete charge/discharge of parallel capacitor, primary current should be larger than I_{Pmin}. The maximum resonance duration is calculated as

$$t_{ZVSmax} = \frac{\pi}{2} \sqrt{L_s C_p} . \quad (8)$$

The characteristics of the new converter is obtained with simulation in MATLAB and given in Fig.3. For high frequency operation dead time interval is kept small. It is accepted that LVI is changed as shown in Fig.3, depending on the output current ($I_P = I_o / a$). Very high values of L_s is not simulated because it increases conduction losses. With proper selection of minimum and maximum values of LVI, nearly constant dead time (≈1μs) is obtained in the converter.

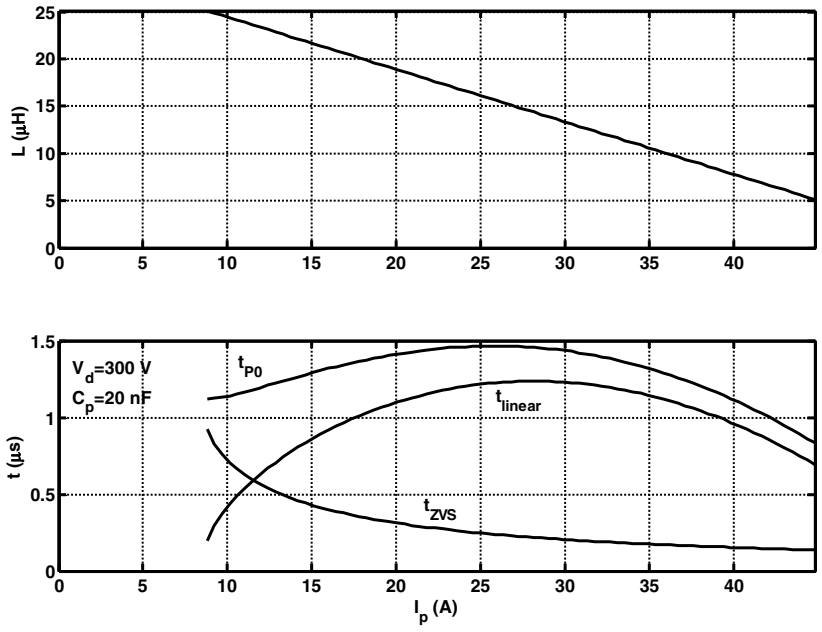

Fig. 3. Lagging leg transition durations according to the LVI variation.

3. Experimental Results

To implement the LVI characteristics shown in Fig.3, two identical cores are used. The parameters of the core are given in Table 1.

Table 1. Core Properties

l	*Magnetic length*	$19{,}2.10^{-2}$ cm
A	*Core area*	$4{,}34.10^{-4}$ cm^2
μ	*Core permeability*	1290

Basic structure of the LVI is shown in Fig.4. Without a control current in the control winding, the inductance of the primary winding is twice of a single winding. Maximum inductance value of the LVI is obtained with proper number of primary turns. Control winding turns are determined experimentally until the required inductance characteristics are obtained.

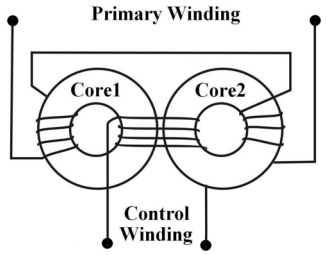

Fig.4. Basic structure of the LVI.

To measure the inductance of the realized LVI an experimental circuit is built. Voltage pulses with short durations are applied to the LVI prototype. Current and voltage waveforms are recorded with a digital oscilloscope and inductance value is calculated from waveforms. The test procedure is repeated for different control currents (I_o) and results are shown in Fig.5. The inductance value of the implemented LVI prototype decreases approximately linearly with increasing control current. The developed LVI is replaced with resonant inductor in the PSPWM converter.

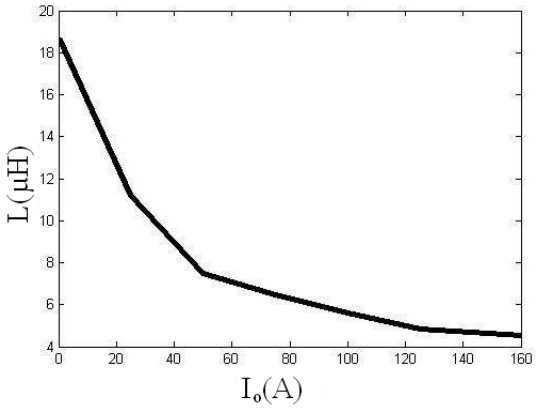

Fig.5. Experimental variation of inductance with output current.

The key components used in the PSPWM converter are given in Table 2. The control of the converter is realized with UC3879.

Table 2. The components used in the converter

S1 - S4	IXGH60N60C2D1
C1 - C4	10 nF-630 V
Cs	2.2 μF 630 V
Transformer	2xE65-N87 a=5:1
Do1, Do2	DSEI 2x121-02A
Lo	30 μH (160A)

Experimental results taken from the converter are given in Fig.6. It is seen that primary current changes direction in less than 1.5μs, because linear inductor value decreases with output current. Also, duty cycle loss and output voltage ringing is quite low.

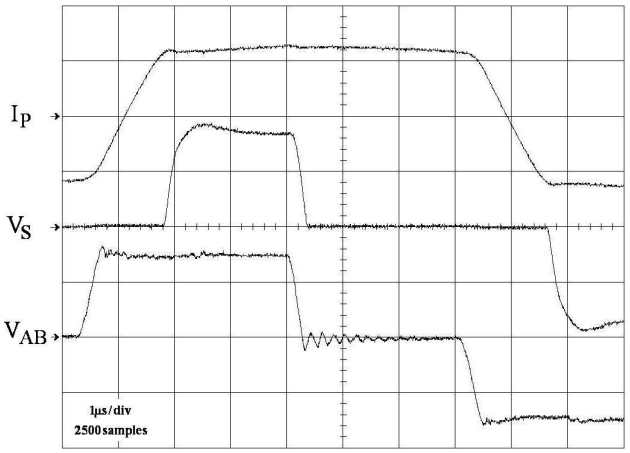

Fig 6. I_P (25A/div), V_S (100V/div) and V_{AB} (200V/div) waveforms for I_o = 140 A respectively.

6. Conclusions

In this study, a new Phase Shifted Pulse Width Modulated (PSPWM) full bridge isolated DC-DC converter is proposed. In the proposed converter, resonant inductor is replaced with linear variable inductor (LVI), and controlled with output current. The new converter has many advantages over recently developed PSPWM DC-DC converters. By selecting the range of the LVI properly, dead time control requirement between gate drive signals of the IGBTs in the same leg is removed. A single phase 160A inverter arc welding machine is implemented with the proposed converter. The experimental results taken from the converter shows the feasibility of the proposed method. The proposed converter is particularly suitable for high current applications such as welding machines.

7. References

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