A 12 bit, 80 Msamples/s, Pipeline Analog to Digital Converter

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ABSTRACT

In this paper, a 12 bit 80-MSample/s pipeline analog to digital converter has been designed and simulated. Circuit techniques used include a dynamic comparator, differential operational amplifier and digital correction. A switched capacitor (SC) circuit is instantiated in each of the pipelined stages. 0.35um standard CMOS was used to simulate designed ADC. Results comprehend a peak SNDR and ENOB of 70.2 dB and 11.34 bit, respectively with a full-scale sinusoidal input at 4.6875 MHz. Total power dissipation is 360 mW from 3.3 V.

I. INTRODUCTION

IN mixed-mode analog-to-digital (A/D) interfaces, there are many applications where a video-rate A/D converter (ADC) is integrated with complex digital signal-processing (DSP) blocks in a compatible, low-cost technology particularly CMOS. Such applications include camcorders, wireless local area-network transceivers, and digital set-top boxes. Advances in CMOS technology, however, are driving the operating voltage of integrated circuits increasingly lower.

Pipeline ADCs implemented in modern CMOS processes achieve high conversion speeds. It is a very attractive choice for high-speed high resolution communication applications due to its good compromise between conversion rate (up to 100 MS/s) and performance. However, their resolution depends on the accuracy of interstage gain, which in turn is determined by open-loop gain of operational transconductance amplifiers (OTAs) in pipeline stages. As it becomes increasingly difficult to design high-gain OTAs, calibration algorithms that can increase ADC resolution by estimating and correcting interstage gain errors become important.

The 1.5 bit-per-stage pipeline ADC architecture is the norm in industry because it lends itself to simple digital correction of the sample-and-hold amplifier (SHA) gain and offset errors, and facilitates the use of dynamic comparators with large input offset. However, it is not the optimal choice from a power consumption perspective primarily because of the higher amplifier count and the fact that amplifier power consumption in switched-capacitor (SC) circuits actually increases (rather than decrease) at low supply voltages [1]. About 31 mW is one of the lowest reported power consumption for a 1.8 V 10-bit 1.5 bit-per-stage pipeline ADC [2] (a much lower value of 16 mW was achieved for a 1.5 V 10-bit 30 MS/s implementation in [3] but with the use of a pseudo-differential architecture for the amplifiers and the advantage of Vsupply > 2.5Vth). On the other hand, multi-bit pipeline stages have been used for implementations that consume slightly lower power dissipation (about 28 mW among the lowest reported [4]). However, the challenge is the higher complexity involved in achieving good linearity in a multi-bit realization at low supply voltages (Vsupply < 2.5Vth). This difficulty is also pertinent to the 1.5 bit-per-stage implementation.

Current CMOS process limits the resolution of pipeline architecture in high speed applications up to10-12 bits. This drawback can be overcome using a calibration scheme which measures the errors in the system and reduces its effects leading to higher effective resolution. The measurement process can be performed with or without interruption of conversion (foreground [5]-[6] and background [7]-[9] calibration, respectively).

This paper describes a 3.3-V, 12-bit, 80-MS/s, pipeline ADC that avoids reliability problems. It was also simulated with CMOS technology with standard threshold voltages.

II. 1.5-BIT/STAGE PIPELINE ADC ARCHITECTURE

A 1.5 bit/stage pipeline ADC is composed of N-cascaded stages that output 2 bits/stage as shown in Figure 1. These digital output bits are aligned in time and processed to form a higher resolution digital representation of the input signal. The extra half-bit of information enables error correction due to sub-ADC offsets. Therefore, the requirements on the components in each stage are relaxed. Specifically, the comparators in each stage's sub-ADC can tolerate offset error as large as Vref/4, and allows for relaxed constraints on op-amp DC gain (finite gain).
A typical stage of the pipeline has a sample and hold, ADC, DAC, a subtraction function and a 2x gain stage as seen in Figure 2. 11 stages are required to obtain 12

effective bits from 22 digital outputs. The first stage has a 1x SHA at its input and the last stage of the pipeline is a full 2 bit switched capacitor flash ADC. If the last stage is implemented as a typical stage (1.5-bits), the last code will be missing, but this is generally not a problem.

The sub-ADC of each stage has 2 comparators with thresholds at -Vref/4 and +Vref/4. The input signal range is +Vref to -Vref. It is followed by a DAC that outputs one of three values (-Vref, 0, or +Vref) based upon the decisions of the sub-ADC. This value is subtracted from the stages input to form a residue for processing by subsequent stages. The subtraction and input sample and hold functions are implemented with a switched capacitor gain stage of 2 at each stage of the pipeline to ensure that the LSB size remains constant at each stage.

This design utilizes switched capacitor techniques to realize the complete sub-ADC as opposed to standard flash sections. This approach contributes to lowering the overall power consumption of the pipeline.

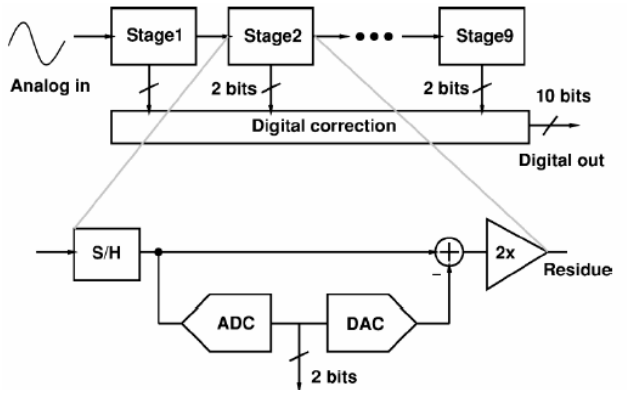

Figure 1. A system level diagram of the 1.5-bit/stage pipeline architecture.

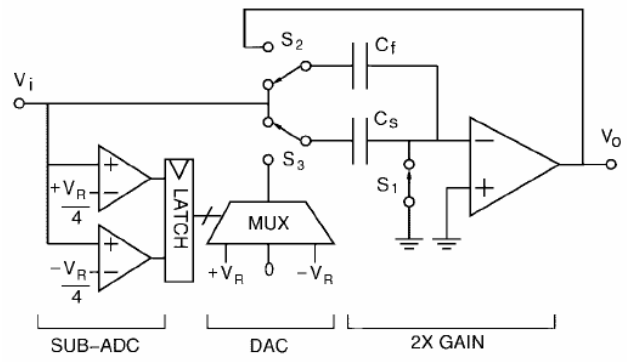

Figure 2. A typical stage in the pipeline.

III. CIRCUIT DESIGN AND OPERATION

The ADC in this paper requires a sample conversion rate of 100 Ms/s which corresponds to a 10ns clock period. The pipeline operations are dictated by two non-overlapping clocks, Φ1 and Φ2 that allocate time for non-ideal rise/fall times and a 1ns delay between clock edges. A clock diagram is shown in Figure 3. As previously stated, the first stage is implemented as a typical stage with an up-front sample and hold. This is optional because the sub-ADC performs a sample and hold function that's aligned in time with the sampled input used to create the residue at the first stage. If the1x SHA is not incorporated, power consumption is reduced and high speed precision comparators can be used to counteract aperture errors.

During the first phase, odd stage DAC outputs are valid and residues are generated that are sampled by the sub-ADC's and2x SHA's at even stages. In the middle of this phase, the even stage sub-ADC's make decisions that are latched and presented to their corresponding DAC's. Concurrently, odd stages have reference values applied to capacitors within the sub-ADCs to generate thresholds of +Vref/4 for the next phase. The second phase operates in a similar fashion, but with even and odd stages reversing roles. Since any given stage samples the residue of the previous stage and provides a valid residue to the following stage by the start of the next phase, the latency through the pipeline is reduced by a factor of 50%.

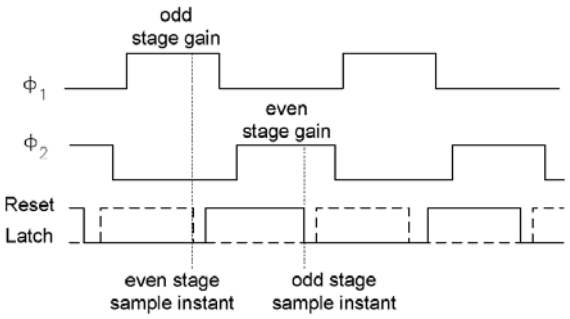

Figure 3. Clock diagram used in the design

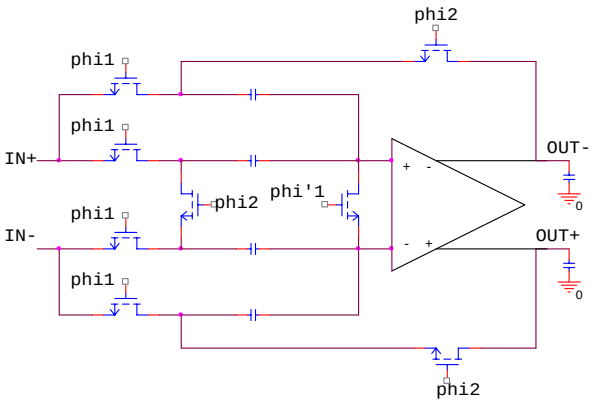

Figure 4. The 2x SHA used in the design

The sub-ADC of each stage was implemented entirely with switched-capacitor circuitry and is fully differential. As indicated in Figure 4, its operation is controlled by two sets of non-overlapping clocks, Φ1/Φ2 and reset/latch.

During phase2, the full (differential) reference value is applied to C, and the capacitors are differentially shorted. In the next phase, *Vin* is imposed to an effective capacitance of 2C (both capacitors) resulting in a differential value of Vin-Vref/4 across the inputs of the comparator. The comparator waits until the middle of phase 2 to sample the input and latch it to the output. The latched outputs are sent a digital block that suppresses bubbles/sparkles, generates proper MSB/LSB's and controls the DAC output. To obtain the reference threshold of -Vref/4, the positive and negative reference inputs are simply reversed. The offset is dominated by the input pair. Under nominal conditions, simulations revealed an offset of less than 3 mV. During the reset phase, the output nodes are pulled to VDD, which prevents the latch from changing states. The outputs of the input pair are shorted together, which sets the seed for the first regeneration phase. This initial regeneration phase helps reduces the time constant of the comparator. In the latching phase, the output nodes are decoupled from VDD, and the latch switch begins conducting. This initializes the full regenerative effect provided by the cross-coupled inverters. The differential output nodes drive the inputs of an S-R latch (not shown in Figure 5), which provide full CMOS logic levels at its output. Finally, when the latching phase ends, the output nodes get pulled back to VDD to hold the state.

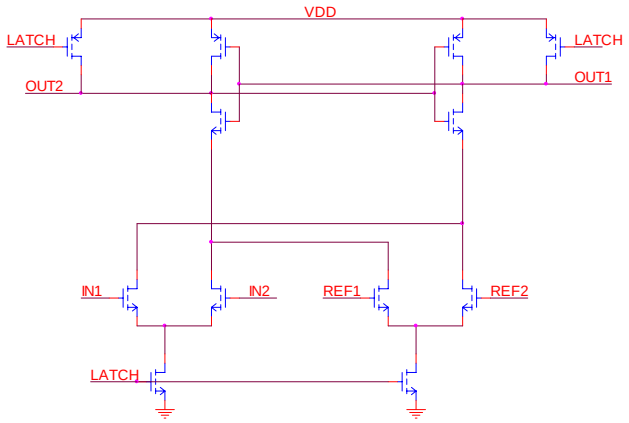

Figure 5. High-speed comparator.

In each stage, an operational amplifier is needed to provide gain and ensure signal integrity down the pipeline. As sampling rates increase, the amplifier has less time to provide an accurate output. The amplifier settling time (or time constant), is proportional to the unity gain frequency and the feedback factor. The accuracy of the settled output, however, is proportional to the open-loop amplifier gain. These conditions provide for a challenging design, since gain and bandwidth are a fundamental tradeoff. Bandwidth can be improved with larger bias current levels since the gain is proportional to device transconductance. However, this reduces the output resistance. These conditions motivated the use of a gain-boosted amplifier topology Figure 6. This topology features four auxiliary amplifiers which increase the overall open-loop gain by their own gain. The top ones are NMOS input and the bottom are PMOS. The additional amplifiers were carefully designed such that the poles introduced into the main amplifier were non-dominant. Table1 shows each amplifier's AC characteristics.

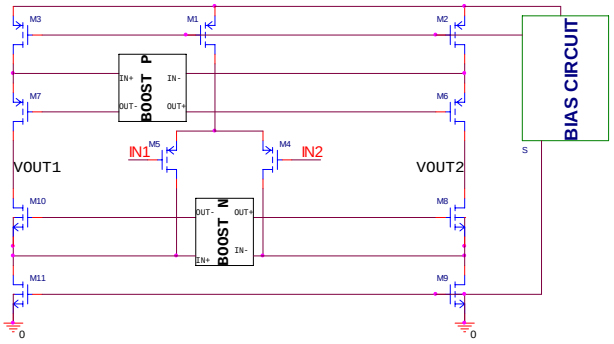

Figure 6. Gain-boosted folded cascade op-amp

Table 1.Opamp performance summery

	DC Gain	UGF	ΦM
PMOS booting amp	41dB	510Mhz	82
NMOS booting Amp	45dB	560Mhz	73
Main Op-Amp	85dB	480Mhz	70

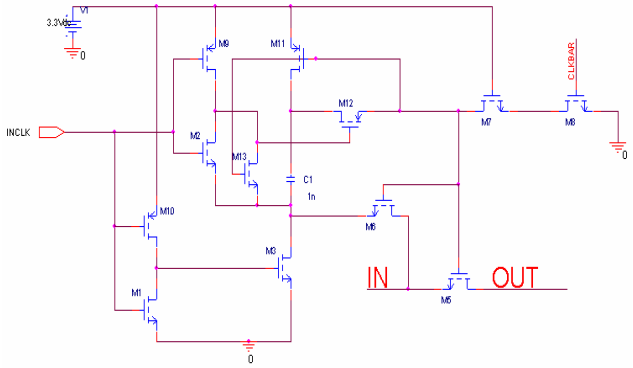

Figure 7. Proposed bootstrapped switch

IV. RESULTS AND DISCUSSION

The proposed ADC has been designed based on TSMC 0.35µm standard CMOS process and simulated using Hspice simulator. The bootstrapped switches showed in Figure 7 have been used in this design. The threshold voltages of this technology for NMOS and PMOS transistors are 0.6V and -0.63V, respectively. Figure 10, shows the ADC linearity simulation for full range of input. In Figure 8, the transient behavior and Figure 9, Fast Fourier Transform (FFT) of the proposed ADC at frequency of 4.6875 MHz has been shown. Table2

summarizes the simulated ADC performance and Table 3 illustrates comparison with other ADCs.

Table 2. Overall ADC performance

INL	0.45LSB
DNL	0.74LSB
ENOB	11.34bit
SNDR	70.2dB
THD	75.23dB

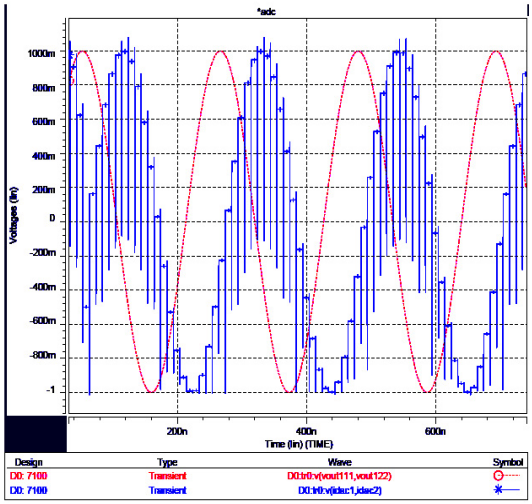

Figure 8. Transient response of ADC

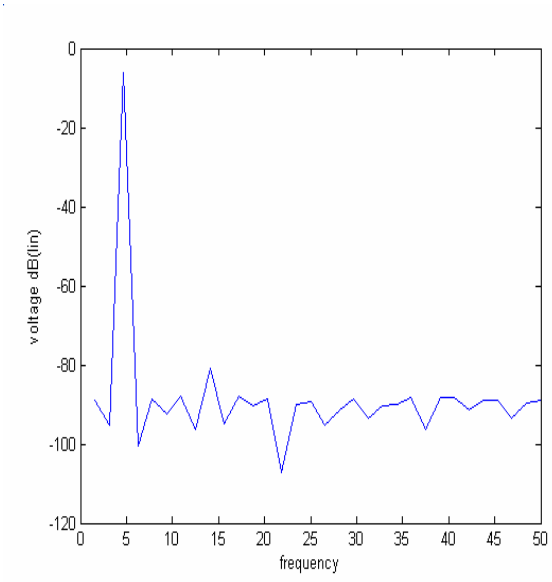

Figure 9. FFT response of output

Table 3. Comparison with other 12 bit ADCs.

ADC	Fs(Msps)	ENOB(bit)	Power(mW)
AD9226	65	11.3	475
AD9235	65	11.4	320
AD9430	70	10.5	1250
AD9433	125	10.6	1350
AD9432	105	10.8	850
This work	80	11.3	360

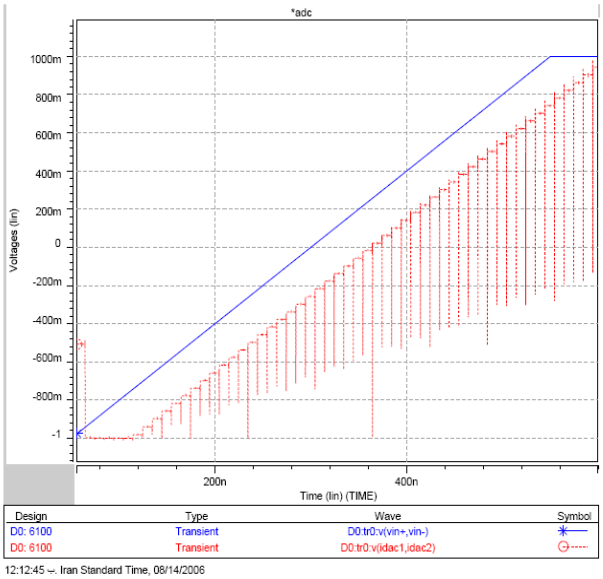

Figure 10. Linearity test of ADC for all codes.

V. CONCLUSION

A 12 bit 80 MS/s pipeline ADC has been presented in 0.35 µm CMOS process. The designed ADC system consumes 360 mW from a single 3.3 V supply with INL and DNL values are less than ±0.5 LSB and ±0.8 LSB respectively. The 1.5bit/stage pipeline architecture with added comparator redundancy and digital correction is very popular, since it allows large comparator offsets and relaxes gain requirements. This architecture has been adapted to allow an arbitrary value of interstage gain.

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