Reconfigurable Implementations of PWL-Based Multiscroll Chaos Generator

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Abstract

In this paper, versatile implementations of PWL-based multiscroll chaos generator have been comprehensively examined in the scope of programmable solutions, both analog and digital, and discrete component realization. To this end, PWL-based multiscroll chaos generator has been implemented using FPAA/FPGA devices and generally known discrete component realizations have been investigated. After that, these implementations have been compared under the terms of implementation easiness, design flexibility, power consumption, dynamic range, area consumption and frequency range.

1. Introduction

Multiscroll chaos generators, which have possible application fields such as broadband signal generators, CNN (Cellular Neural Networks) structures, secure communications and random number generators, exhibit richer dynamics than single-band and double-band chaotic attractors [1]-[5]. Therefore, since first multiscroll model proposed by Suykens and Vandewalle using quasilinear function approach [6], multiscroll chaotic attractors have been a widely researched field of study. In these studies, various multiscroll structures have been developed by using different nonlinear functions other than quasilinear function [7-17]. Among these functions, the most common one is a modified form of the three-segment PWL (piecewise linear) function used in Chua's circuit. Analog realizations of PWL-based multiscroll chaos generators require too many components, thus they are hard to implement. Furthermore, as the scroll number increase, the circuit to be realized is also getting more complicated and necessity for a new prototype occurs for each model. This situation is both time consuming and costly. Moreover, increase in the scroll number means increase in the dynamic range of the circuit to be realized. Therefore maximum scroll number that can be achieved in this type of implementations is limited to the saturation levels of the active components in the circuit.

Today, with their programmability and reconfigurability features, FPGAs (Field Programmable Gate Array) and FPAAs (Field Programmable Analog Array) provide an alternative to discrete analog and digital hardware implementations. FPAAs are electrically reprogrammable integrated circuits, which contain basic analog components in their structure, and they are used in implementations of analog and mixed circuits by providing high stability, accuracy and rapid prototyping techniques. FPGAs are reconfigurable integrated circuits, which consists of programmable digital blocks and programmable interconnections between them. Unlike standard digital microprocessors, FPGAs provide massive parallelism in digital implementations. With these features, FPAA and FPGA devices can be used to overcome the problems observed in discrete implementations of multiscroll chaos generators and to provide an alternative hardware solution. In this context, to meet the requirements mentioned above we aimed to prepare a comprehensive study consisting of both FPAA and FPGA based multiscroll implementations and to give comparative discussions on analog and digital design and implementation issues of multiscroll structures. In frame of comparative discussions about FPAA/FPGA implementations of multiscroll generators, we tried to present a perspective on "which implementation is better for PWL-based multiscroll generators".

This paper is organized as follows: In section 2, a theoretical background and the results of numerical analysis of PWL-based multiscroll chaos generator are presented. FPAA and FPGA based programmable realizations of this model are given in section 3. Finally, discussion and conclusion parts are given in section 4 and section 5, respectively.

2. PWL Function Based Multiscroll Chaos Generator

There are various PWL function based multiscroll chaos generators as mentioned in introduction. The considered PWL function based multiscroll chaos generator is modified version of generalized Chua's circuit and proposed by Suykens, Huang and Chua in [18]. This system is defined as follows:

$$\begin{aligned} \dot{x} &= \alpha\left[y - h(x)\right] \\ \dot{y} &= x - y + z \\ \dot{z} &= -\beta y \end{aligned} \tag{1}$$

Nonlinear transfer function in Eq.1 is described by following equation:

$$h(x) = m_{2q-1}x + \frac{1}{2}\sum_{i=1}^{2q-1}\left(m_{i-1} - m_i\right)\left(\left|x + c_i\right| - \left|x - c_i\right|\right) \tag{2}$$

Eq.2 includes multiple breakpoints expressed with q, ($q \epsilon N^{+}$). For generating n-scroll attractors, the system parameters must be adjusted as in Table 1 [8]. In addition these parameter values, and are chosen 9 and 14, 87 respectively for all n-scroll attractors. The numerical simulation results of PWL function based 5-scroll chaotic attractor and its transfer function are illustrated in Fig. 1.

A discrete hardware implementation example of PWL based multiscroll generator is demonstrated in Fig.2 [8]. Nonlinearity of the given circuit is satisfied by voltage-controlled voltage source realized by op-amps, which permits independent adjustment of both breakpoints and slopes in nonlinearity. The slope of each piece of nonlinear characteristic is obtained by inverting/noninverting amplifiers and voltage branches separately.

Table 1. Parameter values of PWL function based multiscroll chaos generator.

Number Of Scrolls	Parameter Values
n=3	$q=2$ $m=[+0.9/7 \quad -3/7 \quad +3.5/7 \quad -2.4/7]$ $c=[1 \quad 2.15 \quad 4]$
n=4	$q=2$ $m=[-1/7 \quad +2/7 \quad -4/7 \quad +2/7]$ $c=[1 \quad 2.15 \quad 3.6]$
n=5	$q=3$ $m=[+0.9/7 \quad -3/7 \quad +3.5/7 \quad -2.7/7 \quad +4/7 \quad -2.4/7]$ $c=[1 \quad 2.15 \quad 3.6 \quad 6.2 \quad 9]$
n=6	$q=3$ $m=[-1/7 \quad +2/7 \quad -4/7 \quad +2/7 \quad -4/7 \quad +2/7]$ $c=[1 \quad 2.15 \quad 3.6 \quad 8.2 \quad 13]$
n=7	$q=3$ $m=[+0.9/7 \quad -3/7 \quad +3.5/7 \quad -2.4/7 \quad +2.52/7 \quad -1.68/7 \quad +2.52/7 \quad -1.68/7]$ $c=[1 \quad 2.15 \quad 3.6 \quad 6.2 \quad 9 \quad 14 \quad 25]$

Breakpoints are set by gains of inverting and noninverting amplifiers. As shown in discrete circuit scheme, this realization requires many active elements and analog building blocks. This realization is capable of generating 5 scroll attractor and to increase the number of the scroll, additional building blocks should be added to this scheme yielding more complex circuitry.

3. FPAA/FPGA Based Implementations of PWL-Based Multiscroll Generator

FPAA and FPGA offer very important programmable design possibilities for multiscroll chaos generator design such as reducing the complexity of design, real-time modification or completely new design possibility, flexible software control and adjustment within the system.

FPAA device used in this study is AN231E04, which enables flexible and rapid prototyping of analog circuits by programmable blocks called CABs (Configurable Analog Blocks) [19]. This device includes four CABs. A CAB consists of op-amps, an array of switches and a capacitor bank. Switched-capacitor technology is used for implementing various analog functions in a CAB. Different circuit configurations are obtained via adjustment of switches between various components inside CABs.

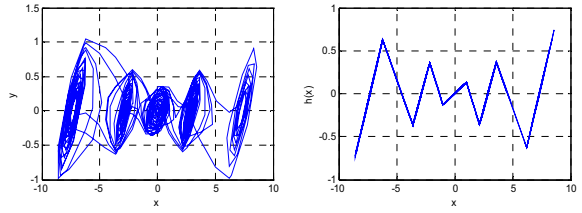


Fig. 1. Numerical simulations of PWL function based 5-scroll attractors (a) phase portrait, b) PWL characteristic.

In FPAA design process, firstly the system is tested via numerical tools before FPAA modeling, because saturation level (±3V) of FPAA devices mostly prohibits a direct implementation of most systems. If any exceeding value is observed, the model must be rescaled according to simulation results and saturation levels. Then, the system model formed on FPAA software tool is downloaded to the FPAA device via a serial interface port. Afterwards, obtained experimental results are compared with numerical simulations. If the results are matching then the implementation process is completed, else the model is modified [20].

FPGA device used in implementations of these multiscroll generators is CycloneIII (EP3C16F484C6) IC available on Altera DE0 educational board [21]. CycloneIII has 15408 digital blocks called logic elements and 112 9-bit embedded multipliers, which will be effectively used in our designs. Also, Altera DE0 board has various peripherals, control and display units. Yet, it can be considered as a simple board compared to its counterparts.

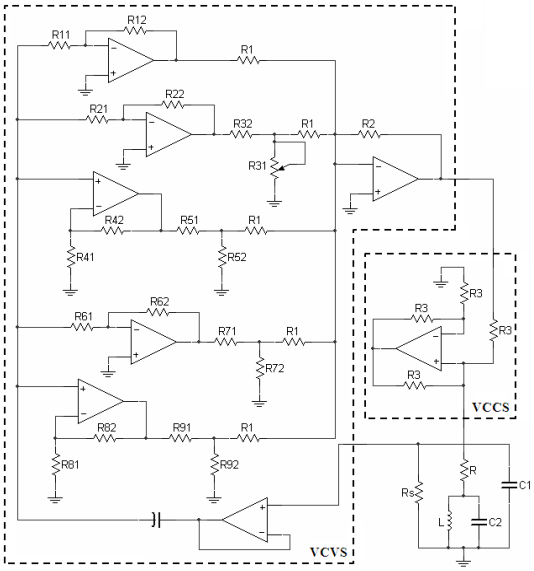


Fig.2. A discrete hardware implementation example of PWL function based multiscroll chaos generator [8].

Since we aim here to implement these multiscroll chaos generators on FPGAs as practical as possible instead of complex discrete hardware realizations, this device selection is ideal to show how compactly multiscroll generators can be realized even on a simple programmable hardware. For the same reasons, digital outputs are fed to 8-bit DACs, while higher resolution DACs offer much more efficiency. To provide practicality in these implementations, a modular design method in which a multiscroll structure is realized as small different parts that can be also used in other multiscroll generator designs is followed. These parts are realized with VHDL (Very High Speed Integrated Circuit Hardware Description Language) codes on QuartusII software using 32-bit fixed point numerical notation. When it is possible, we tried to form a whole design that consists of different generators on same implementation where those parts behave different characteristics for desired operation. When it is not, we tried to form a general design scheme that can be applied to different generator implementations where some of those modular system parts are used repeatedly for different systems. Synthesis results of these implementations are given for comparison in following sections.

3.1. FPAA Implementation

To implement PWL function based multiscroll chaos generator on FPAA, the continuous time equations defined by Eq.1 is used. When the numerical simulation result in Fig.1 is scrutinized, it is seen that state variables have exceeded saturation level (±3V). To eliminate the saturation problem, system is rescaled. Then rescaled equations are modified with respect to SUMFILTER block design aspects. As a result of these operations, the modified system definitions which will be essential to FPAA modeling of PWL function based multiscroll chaos generator are given in Eq.3 and Eq.4.

$$\begin{aligned} \dot{x} &= ax + by - ch(r_s x) \\ \dot{y} &= dx + ez \\ \dot{z} &= z - fy \end{aligned} \tag{3}$$

$$h(r_s x) = m_{2q-1} r_s x + \frac{1}{2}\sum_{i=1}^{2q-1}(m_{i-1} - m_i)(|\, r_s x + c_i\,| - |\, r_s x - c_i\,|) \tag{4}$$

Here, the values m_{2q-1} and c_i are taken same as the numerical analysis done before for 3 to 7 scrolls. To observe experimentally PWL function based multiscroll chaotic attractors from 3-scroll to 7-scroll on FPAA, parameter values are set as in Table 2.

Table 2. Parameter values of PWL function based multiscroll chaos generator on FPAA.

Number Of Scrolls	Experimental Setup Parameters
n=3	a=0.8, b=4.15, c=3.15, d=3, e=3, f=4.76, r_s=3.
n=4	a=1, b=1.87, c=4.2075, d=5, e=7, f=2.04, r_s=5.
n=5	a=1, b=1.8, c=1.8, d=5, e=6, f=2.04, r_s=5.
n=6	a=1, b=1.93, c=2.895, d=5, e=5, f=2.856, r_s=20.
n=7	a=1, b=0.955, c=1.719, d=10, e=12, f=1.19, r_s=10.

The FPAA implementation scheme of PWL based multi-scroll chaos generator circuit is shown in Fig.3. The state-variables x, y, and z are constituted at the outputs of SUMFILTER blocks. Circuit gains providing system parameters in Table 2 are realized by adjusting input coefficients of SUMFILTER blocks. And the nonlinear PWL function is realized with a user-defined TRANSFER FUNCTION block.

Each n-scroll structure (from 3 to 7) is constructed in FPAA software tool separately according to PWL function and parameter values in Table 2. After modeling circuit implementation in FPAA software tool, each model is downloaded to the FPAA development board via serial interface. Experimental measurements are obtained from I/O connections of the FPAA board. Multiscroll attractor and nonlinear transfer function characteristic belong to 5-scroll structure are shown in Fig.4. As shown in this table, for each FPAA implementation it is sufficient to use only one FPAA board consisting of four CABs.

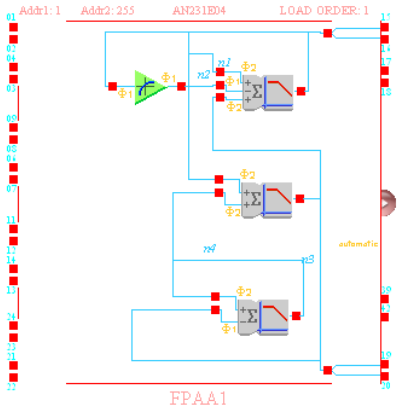


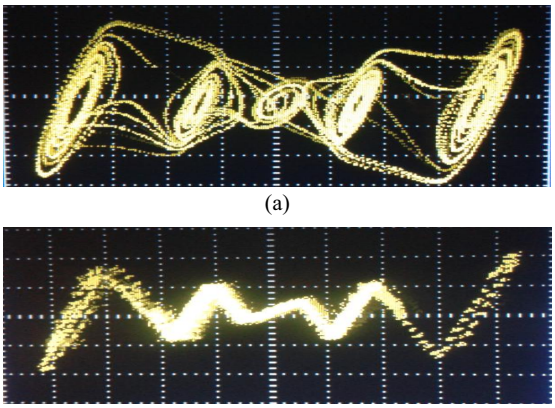
Fig.3. FPAA implementation scheme of multiscroll chaos generator circuits.

3.2. FPGA Implementation

To implement PWL based multiscroll chaos generators on FPGA, continuous time equations defined by Eq.1 is discretized using Euler discretization method by taking discretization constant as 0.01. Derived equations are as follows:

$$\begin{aligned} x_{n+1} &= x_n + \alpha[y_n - h(x_n)]\Delta k \\ y_{n+1} &= y_n + (x_n - y_n + z_n)\Delta k \\ z_{n+1} &= z_n - \beta y_n \Delta k \end{aligned} \tag{5}$$

$$h(x_n) = m_{2q-1} x_n + \frac{1}{2}\sum_{i=1}^{2q-1}(m_{i-1} - m_i)(|x_n + c_i| - |x_n - c_i|) \tag{6}$$



(a)

(b)

Fig.4. 5-scroll attractor and nonlinear transfer function of PWL function based multiscroll chaos generator implemented on FPAA for; (a) n=5, x-y plane x= .2 Volts/Div, y= .2 Volts/Div; (b) n=5 x-h(x) plane x= .2 Volts/Div, y=.2 Volts/Div.

The parameters of these equations are taken same as the numerical analysis done before for 3 to 7 scrolls. When these equations are examined it is seen that the main Chua's system in Eq.5 will be same for each multiscroll implementation with different transfer functions.

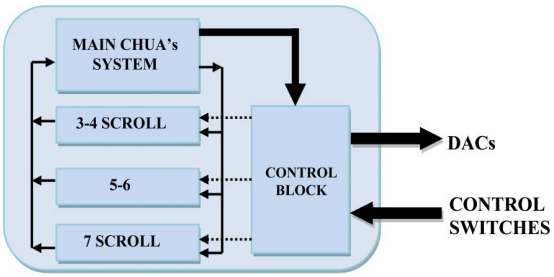
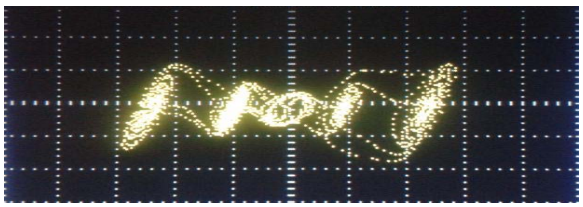
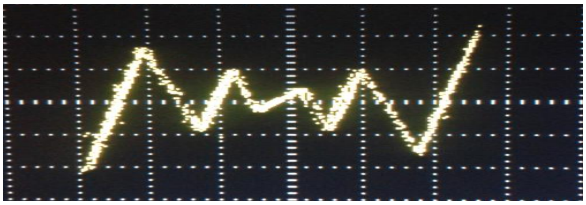


Fig.5. The FPGA design scheme of PWL function based multiscroll chaos generator implementation.

Not only that but also it is seen even the number of the mathematical operations in transfer functions of 3-4 and 5-6 scroll systems are exactly the same. This gives a good idea to implement them using same hardware on FPGA without consuming too much logic blocks. Besides its area efficiency, this kind of implementation is much more practical to observe different n-scroll generators simultaneously just by changing assigned control switches on the FPGA board without reprogramming the device. The general FPGA scheme designed with this approach is described in Fig.5.



(a)



(b)

Fig.6. 5-scroll attractor and nonlinear transfer function of PWL function based multiscroll chaos generator implemented on FPGA for; (a) n=5, x-y plane x= 1 Volts/Div, y= 2 Volts/Div; (b) n=5, x-h(x) plane x= 1 Volts/Div, tf= 1 Volts/Div.

As seen in this figure, the first step of the design is to form the main Chua's system in Eq.5 using VHDL without its transfer function part. Then using the same way transfer functions are formed and connected to this main circuit separately. However, for 3-4 and 5-6 scroll systems, same transfer function hardware is formed with switch controlled parameters, i.e., 3-4 scroll hardware acts as a 3 or 4 scroll transfer function for predefined conditions of the control switches. In this way, only operand parameters are changed thus the number of the operational blocks (adder, multiplier, etc.) on hardware remain the same. In this scheme, control block organizes whole design. According to applied switch position, control block activates the requested transfer function's block, and sends the proper signal telling this activated block which parameters will be used. After that, activated transfer function block handles all mathematical operations for given value of x_n sent from main Chua's system and sends the calculated $h(x_n)$ value back to it within a clock cycle.

In this way, main Chua's system calculates x_{n+1} value and for each clock cycle this process is repeated. Another task that control block handle is scaling and sending the right outputs to the DACs, which are requested by user through control switches. For that reason main Chua's system outputs x_n, y_n, z_n and $h(x_n)$ are sent to control block before transferring to DACs. Here control block scales them to 8 bit values and sends chosen two of them to DACs. This allows users to be able to observe both attractor and transfer function characteristics on an oscilloscope like display unit again just by changing a control switch. Obtained results of this design implementation are given in Fig.6. In this design, all embedded multipliers are used in the implementation process and these results as extra area consumption on FPGA. Nevertheless, %68 area consumption for this comprehensive design implemented on a simple educational board is very acceptable.

4. Conclusions

As for PWL based implementation, studies showed that discrete circuit realization becomes more complicated as scroll number increases. But for FPAA and FPGA based realizations PWL function can be easily expressed via software tools. Hence, while FPAA and FPGA implementations of PWL functions show very good performance, the discrete circuit implementation is expressed as an ineffective way of implementing PWL function. The programmability and reconfigurability features of FPAA and FPGA devices provide flexible design possibilities such as reducing the complexity of design, real-time modification, software control and adjustment within the system. The programmable and reconfigurable devices are more practical than the discrete circuits and they provide rapid prototyping facilities to the user. For these reasons, FPAA and FPGA based multiscroll implementations using PWL nonlinear functions have been evaluated as high acceptability in terms of design flexibility parameter.

Power consumption is accepted as another comparison parameter. For multiscroll chaos generator implementations, while FPAA's power consumption ranges between 60-140 mW, FPGA's power consumption is calculated approximately 85 mW. Discrete circuit implementation designs' power consumptions for three multiscroll generators are calculated approximately 500 mW for PWL based multiscroll generator.

Among these three design procedures, the widest dynamic range belongs to discrete circuit implementations because of the highest supply voltages. While FPAA need to rescale of system parameters and naturally this process gives constrict to the dynamic range of this IC, the dynamic range in FPGA depends on the bit length of the numerical notation in use instead of supply voltages. In the conversion of digital FPGA outputs to analog, this dynamic range can be adjusted via amplifier stage of the DAC unit. As a result of this comparison, the multiscroll structure based on FPGA and discrete circuits are evaluated as high acceptability.

The area consumptions of the two programmable IC's have been also presented in the related section in the paper. Area consumptions in these tables represent the usage percentage of the IC resources. As shown these tables, only one FPAA or FPGA IC device is sufficient to implement referred multiscroll generators. Naturally the discrete circuit implementations did not take part in this comparison.

From the point of view of the frequency range, the manufacturer data shows that FPGA offers a wide range of 500 MHz. In contrast to this, the default operating frequency in FPAAs is chosen as 2 MHz and can be extended to 8 MHz. Multiscroll chaos generators based on discrete implementation are able to capable to generate chaotic signals in MHz levels. For this purpose, current-mode active elements should be used in the circuit configuration.

By using design techniques presented here, prototypes of other similar multiscroll chaos generators can be constructed rapidly and the testing and verifying process can be executed on this programmable platforms. In future works, besides individual FPAA or FPGA based system implementations of chaos and multiscroll chaos generators, in order to benefit the advantages of both devices we will deal with mixed hardware solutions using both FPAA and FPGA devices together simultaneously.

ACKNOWLEDGMENT

This work has been supported by "Office of Scientific Research Projects of Erciyes University" under FBA-11-3548 grant number

5. References

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