ALL-SİLİCON OPTİCAL TECHNOLOGY FOR CONTACTLESS TESTİNG OF INTEGRATED CİRCUİTS

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ABSTRACT

This paper demonstrates an all-silicon contactless testing approach using a modified microscope system and a novel silicon LED fabricated on the "device under test". This cost effective approach utilizes optical signals and avoids known problems associated with the large number of mechanical probes required for wafer testing of advanced silicon ICs.

I. INTRODUCTION

With increasing chip densities, the conventional mechanical probing approach for internal fault detection and functional testing has become obsolete. Mechanical probes have limitations because of their large size and their inherent parasitic effects. The SIA National Technology Roadmap for Semiconductors (1997) predicts that the ASIC's will need over 3000 I/O pads in the first years of new century, with a peripheral pitch distance of 50 μm [1]. The reliability of testing, with an ever-increasing number of mechanical probes in direct contact with the chip periphery is also becoming a major concern in testing.

"Design for Testability" approaches can enhance test-vector coverage through circuit-level design strategies. Such techniques have extended the usefulness of mechanical test approaches, but cannot ameliorate the fundamental limitations associated with the simultaneous, mechanical probing of large numbers of small pads. New approaches will be required as the roadmap suggests.

Contactless testing resolves many of the challenges associated with conventional mechanical wafer testing. A number of contactless techniques have been investigated since 1980's, but none have yet found acceptance as a routine testing tool. Electron-beam testing has been used in a variety of ways for many years, and techniques such as photoemissive probing, electro-optic sampling, charge density probing, and photoexcitation techniques have also been investigated. These contactless techniques can provide access to determine the logic state of internal nodes of a device under test. These contactless technologies also have a collection of major disadvantages, including such factors as high equipment costs, complex test set-ups, complex measurement chamber requirements (often high-vacuum), crosstalk, incompatibility with conventional wafer probing systems, and the risk of DUT damage [2].

The work reported here describes a new test methodology without the above limitations. This new approach is completely compatible with silicon IC technology, and can be implemented simultaneously with conventional mechanical probes using standard equipment.

A fully optical contactless testing technique is presented utilizing the integration on the DUT of a silicon light emitter, or LED (for sending data out optically) and a silicon photodiode (for receiving data). In addition the DUT would contain a driver circuit for the LED, and an amplifier and comparator circuit to amplify the signal from the photodiode and reconstruct a logic compatible digital signal (Figure 1). The chip area required for these circuits has been calculated to approximate that required for a bond-pad and associated drive or input buffer circuitry. The selected "output" electrical signals are converted to optical signals by on-chip silicon-based LEDs or electroluminescent photon sources [3].

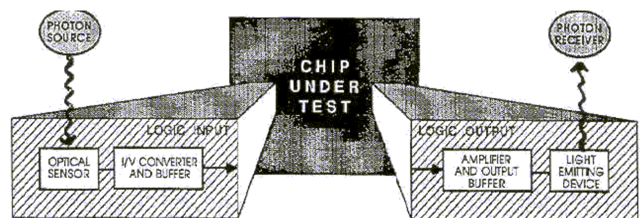


Figure 1. All-silicon contactless testing approach

Silicon is a generally poor material for light emission, though it is reasonably good as a photo-detector. The use of an optimized silicon light-emitting diode structure as an

electroluminescent source allows the entire approach to be fully compatible with current silicon technology [4].

II. EXPERIMENTAL SET-UP

The equipment required to implement this concept at wafer probe consisted of an optical lens system (much like a microscope) and an optical test head that is fully compatible with mechanical probes. In fact, mechanical probes will be used for power, ground, and certain test vectors. The optical test head can simultaneously monitor the logic state of additional test nodes, both at the die periphery and internal to the chip (Figure 2).

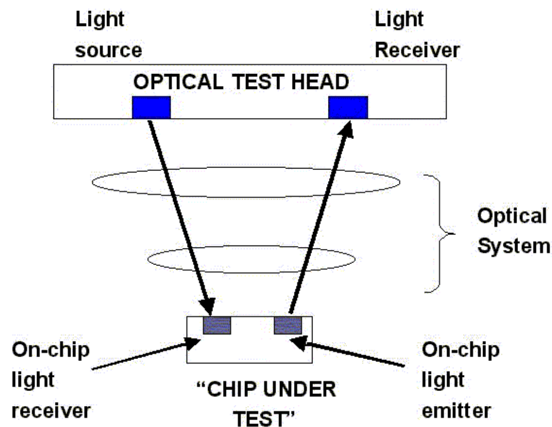


Figure 2. Optical Set-Up

In order to demonstrate an all-silicon optical test approach, breadboards using a hybrid approach were utilized. Figure 3 shows the complete picture of the optical system that has been designed for the experiments.

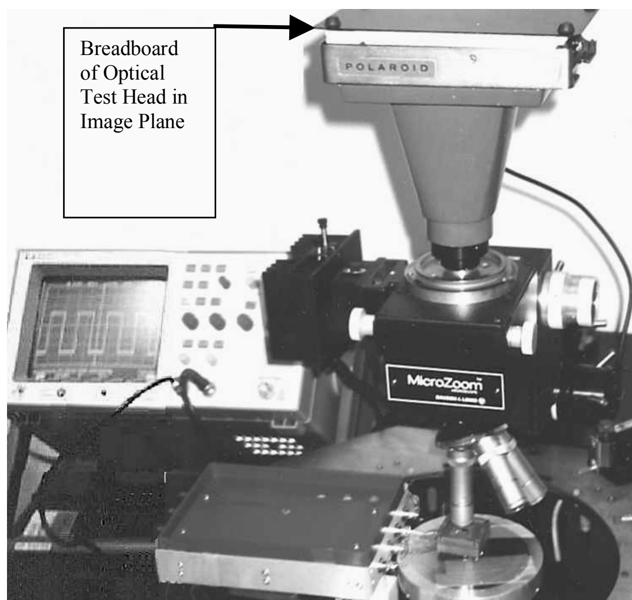


Figure 3. The experimental optical system, with the hybrid breadboard component .

As can be seen in this figure, a Polaroid camera and a B&L microscope optics system has been fit together to make the optical testing system possible.

In the experiments, "Silicon Light Emitter" chip was fabricated for use in this project, and has been utilized as "chip under test". This chip includes many silicon light emitting and detecting structures, such as Schottky photodiodes (Figure 4).

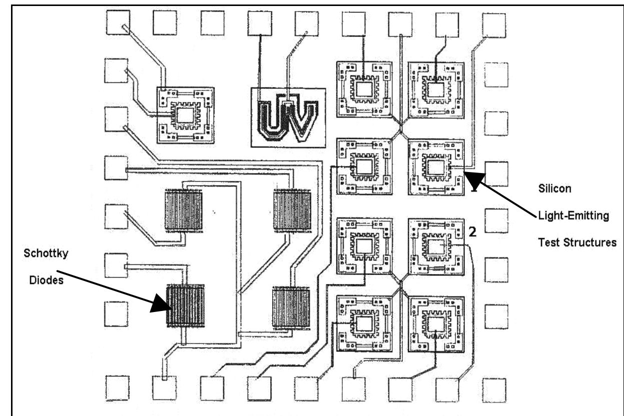


Figure 4. The specially designed experimental DUT

Due to fabrication difficulties, the Schottky diodes on this chip indicated a high dark current which limited their sensitivity. Because of that, in the experiments, the silicon "postage-stamp" test structures have also been utilized as silicon photodiodes. Their usage as photodiodes has become possible by the proper adjustment of their corresponding bias voltages.

II. EXPERIMENTS

TRANSMISSION OF INPUT STIMULUS FROM OPTICAL TEST HEAD TO CHIP (DUT) FOR DATA ENCODING

Two spatially separated optical input signals were simultaneously applied to the DUT to establish the simultaneous transmission of multiple input signals. Figure 5 illustrates the experimental set-up, with two GaAs LEDs serving as pulsed light sources. A circuit board located on the image plane of the Polaroid attachment encloses the LED's (see Figure 3). The LEDs are positioned at locations on the image plane corresponding to silicon photodiodes on the DUT. In general a source array will be designed specifically for each DUT. The location of sources corresponds to the imaged location of internal nodes to be tested, and is, therefore, particular to the optical test head configuration used for test. The whole image of the "chip-under-test" appears on the image plane when the proper lens combination has been used, and therefore proper location

of the LEDs straightforward. In the experiment, an 8X objective has been utilized.

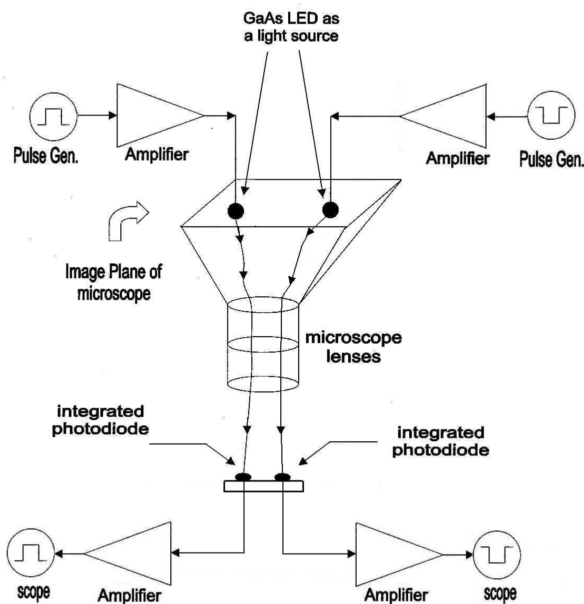


Figure 5. Schematic of transmission of stimulus data from optical test head to chip

For this experiment, adjacent photodiodes were chosen to represent internal circuit test nodes. This choice maximizes the probability of cross-talk between the two photodiodes, which are separated by 520 μm. The square-wave modulation signals for these LED's were set 180º out of phase.

The photodiode outputs are connected to transimpedance amplifiers housed in a shielded breadboard arrangement. The transimpedance amplifer converts the photodiode current to an output voltage. The minimum transimpedance required to obtain detectable signal depends on the test head's optical output power and the attenuation of the particular optical setup. However, it was calculated for nominal values that a transimpedance of 20Kohms would provide adequate signal for the comparator. The integration of such a transimpedance amplifier on a silicon chip has been demonstrated feasible in CMOS [5]**.** The signal is then processed by a comparator circuit with its threshold set near the middle of the voltage swings from the amplifier, to restore proper logic levels. The schematic drawing of the transimpedance amplifer used in the the hybrid breadboard is shown in Figure 6. The hybrid comparator circuit utilizes a CA3290 in a standard comparator configuration. Figure 7 shows the output waveforms for the two optical encoding signals. Figure 7a shows the left, and 7b shows the right side of the light transmission path of Figure 5.

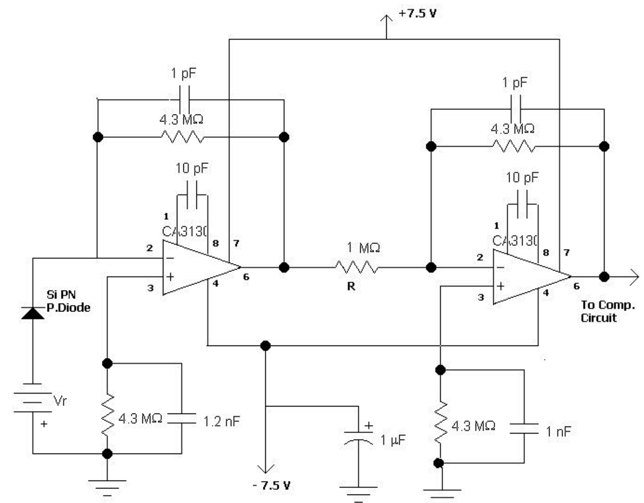
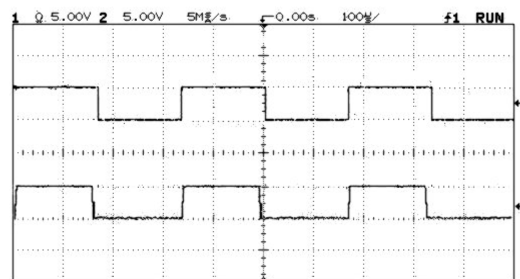


Figure 6. The hybrid transimpedance photodiode amplifier schematic drawing.

These results clearly indicate that it is possible to transmit multiple input optical signals simultaneously to chip with negligible cross-talk.



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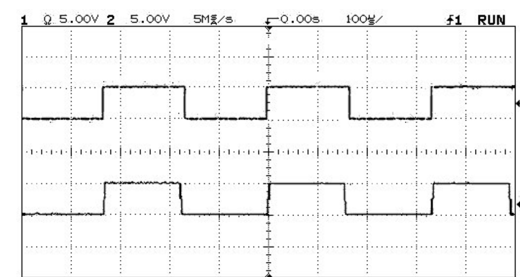

7b

Figure 7. The comparison of each output signal to its original input signal. Upper waveforms show the original signals, and lower ones show the outputs.

TRANSMISSION OF CHIP OUTPUTS FROM DUT TO OPTICAL TEST HEAD FOR EXTRACTION

The simultaneous transmission of output signals from the chip to the optical test-head for detection is also required for the success of the proposed method. This transmission is a greater challenge than the input signal transmission,

because of the relatively weak on-chip silicon emitter. The light generating test structures were fabricated by standard silicon processing techniques and resulted in a silicon p-n junctions that emit visible light when operated in avalanche breakdown. Figure 8 shows the "postage-stamp" test structure. Despite its low quantum efficiency, sufficient light is generated for applications involving contactless testing.

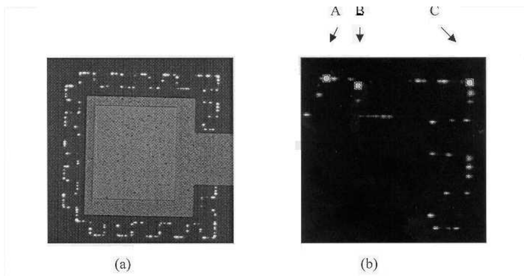

Figure 8. Silicon light-generating test structure

The experimental set-up for the output extraction is shown in Figure 9. A pulse generator drives an amplifier that drives the silicon light-emitting structure. Emitted light is focused through the microscope and detected by a detector placed at the proper location in the image plane of the microscope. Either a photo-multiplier tube or an avalanche photodiode with amplifier circuitry can be used as the detector; this experiment utilized the Hamamatsu avalanche photodiode module C5460-0, which has a gain of -1.5E8 V/A. The resulting waveform at the detector output can then be compared with the original waveform driving the silicon light-emitter on the DUT.

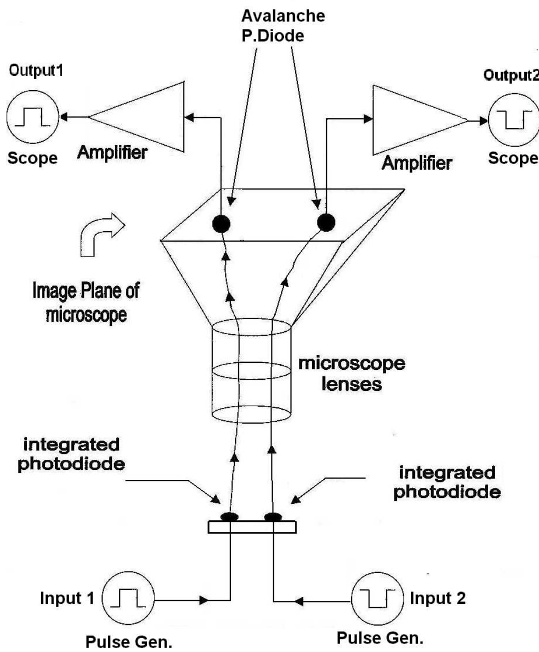

Figure 9. Simultaneous transmission of output signals for extraction.

Two output optical signals from the DUT were sent simultaneously to the optical test head to characterize the extraction of multiple output signals. Two adjacent silicon light emitting structures on the DUT (Figure 4) were modulated at 10 kHz for transmission. This frequency was the upper frequency limit of the available detection instrumentation, however the time response of hot-carrier luminescence in silicon LED's has been shown to be in the range of several picoseconds [6,7]. This would suggest testing frequencies above a gigahertz are possible. The silicon light emitters were modulated at 180º phase difference. Figure 10 and 11 compares the resulting output waveforms to the original waveforms for each transmission path In this figures, the output signal image on the oscilloscope screen has been inverted to account for the negative amplifier gain. The excellent correspondence between these signals demonstrates that multiple output signals can be simultaneously extracted with negligible interference.

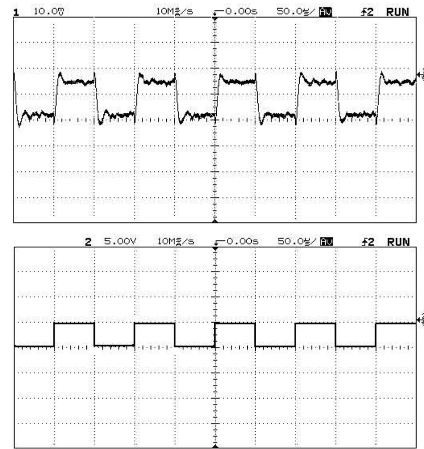

Figure 10. Signal waveform at the detector output (upper) versus input signal applied to Si LED (lower) - "the left transmission path"

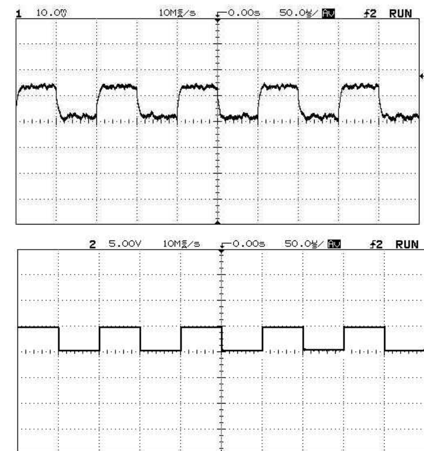

Figure 11. Signal waveform at the detector output (upper) versus input signal applied to Si LED (lower) - "the right transmission part".

THE SIMULTANEOUS TRANSMISSION OF DATA IN BOTH DIRECTIONS

This experiment was performed to examine the possibility of sending and receiving data from the chip simultaneously. Figure 12 shows such an arrangement in which data is transmitted to a DUT optically, converted to logic signals, processed by the chip, and the output data transmitted back to the test head optically.

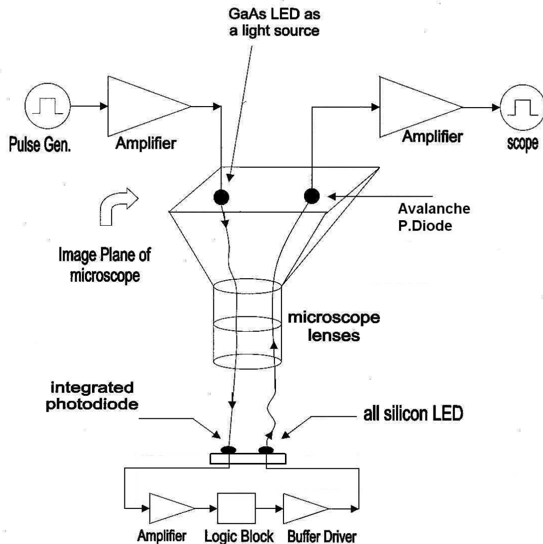

Figure 12. The experimental set-up for simultaneous encoding and extraction of test data.

In this experiment, both an avalanche photodiode and a GaAs LED are placed at specific separate locations on the image plane of the microscope, corresponding to the light-emitter and photodetector on the DUT, respectively. The test vectors are encoded and extracted using the processes described before. It was found that when light pulses were simultaneously sent from the optical test head, and from the DUT, reflections in the microscope from the strong GaAs LED signal created cross-talk and blocked out the weak Si LED signal.This problem can be easily avoided by special design of the test procedure, and is not considered to be a major limitation of the contactless testing method. The timing of the test process can be arranged such that the chip output is observed at a different time than the test input data.

IV. RESULTS AND DISCUSSION

Experimental results demonstrate that multiple optical test vectors can be input on the periphery or within the core of a DUT with negligible crosstalk using this technique. Thus, optical signals can be simultaneously supplied to a silicon chip for data encoding through multiple test vectors. Multiple simultaneous output signals have also successfully been extracted with negligible crosstalk indicating the possibility of high observability and coverage with the technique. Optical input and output for test vectors offers significant reductions in the mechanical complexity and reliability of chip-level testing relative to mechanical contact probe techniques.

The limitations of the technique have not yet been fully explored. Measurement speed will be limited by the switching speed of Si LEDs. Based on hot carrier luminescence work of Kash and Tsang (previously referenced) which report that switching speeds exceeding 10 GHz can be measured using hot carrier luminescence, the switching time for Si LEDs is expected to be on the order of picoseconds.

Frequency limitation on the performance of the breadboards used in this experiment is due to limitations of the electronic instrumentation system, and not representative of more sophisticated implementations of the approach. Further study is required to determine the ultimate measurement bandwidth of the proposed testing approach.

V. CONCLUSION

This work demonstrates the feasibility of an all-silicon contactless testing approach. Experimental data illustrate that multiple, simultaneous optical signals can be simultaneously input to or output from a silicon chip.

A contactless optical testing approach can address challenges associated with increases in the number of physical test probes require to test increasingly complex Silicon ICs. The proposed method appears economically practical, given the availability and low cost of required system components. The method should have implementation costs significantly lower than other contactless methods.

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