MOS-Only Third Order Butterworth Filter with DTMOS Tuning Technique for High Frequency Applications

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Abstract

In this paper, a new low-voltage, MOS-only, third order low-pass filter is proposed. The core circuit consists of only three MOSFETs and their parasitic gate to source capacitances as passive elements. Using TSMC 0.18µm technology parameters, the circuit with all biasing elements included consumes just 0.69mW for a cut-off frequency higher than 200MHz under a single supply of 1.8V. Non-ideal effects have been investigated and dynamic threshold voltage MOS (DTMOS) tuning technique has been developed for the filter circuit to suppress the non-idealities. Resulting circuit is capable of operation at high frequencies with low power consumption due to the usage of significantly less number of transistors than conventional active block-based filtering circuits.

1. Introduction

When designing an electronic circuit, it is usually considered that there are parasitic properties of the components, effects of which should be reduced by reducing their relative effect on the output. One instance of such parasitic properties is to be found in MOS transistors as the capacitances between transistors' terminals. In common design procedure, these effects are tried to be minimized.

Another electronic design aspect is the usage of passive elements such as resistances and capacitors. These elements have rather high tolerances and occupy more space than transistors in ICs. Minimizing the usage of these passive elements is a desired design specification.

Utilizing the parasitic capacitances and the transconductance of MOS transistors as capacitances and resistance offers a solution to the above mentioned concerns. Briefly, this approach turns disadvantages into advantages.

Using a minimum number of transistors is another desired design specification. As the number of transistors in a circuit increases, high frequency performance of the circuit decreases because of the capacitive properties of the transistors. So, for a good high frequency performance, the number of transistors should be minimized. Moreover, the minimization of the number of transistor also decreases the required supply voltage value of the circuit.

A common approach in the design of analog filters is using active elements such as current conveyors or other building blocks. But, as mentioned above, the large number of transistors in these building blocks reduces high frequency performance of the design and the required supply voltage is increased. In the literature, there has been an increasing amount of interest on circuit design using MOSFETs because of the aforementioned specifications [1-2].

On the other hand, some filter circuits that are recently presented in [3-5] use a different approach called as "MOS-Only". Beside their simplicity, MOS-only circuits both eliminate the necessity of connection of additional passive resistor and capacitor elements. Transconductance gain of MOSFETs in saturation region is used instead of passive resistance. The C_{gs} capacitance of these MOSFETs is used instead of passive capacitor. Therefore, high frequency operation is an inherent feature of this design methodology. A MOS-Only first order all-pass filter is presented in [3]. Furthermore, using only nine MOSFETs, a second order current mode MOS-Only circuit presented in [4] that has single input and triple output such as band-pass, low-pass and high-pass. The biquad low-pass/band-pass dual output current mode MOS-Only circuit in [5] employs only eight MOSFETs.

In this study a third order MOS-Only Butterworth filter circuit is presented. In the literature several Butterworth filter circuits are presented such as [6]. For example, a third-order current-mode high frequency Butterworth low-pass filter has been proposed with using OTAs in gm-C configuration [6]. The filter cut-off frequency was 200MHz with a power consumption of 16.77mW. However, this topology requires relatively large number of transistors to realize the OTA elements and additional passive capacitances [6]. Instead of conventional gm-C technique as exemplified in the study [6], it is possible to get similar results with employing less number of transistors, without using additional passive elements and significantly lower power consumption when MOS-only technique is used in the design of third-order current-mode high frequency Butterworth low-pass filters.

In this study, in addition to first order [3] and second order [4-5] filters in the literature, a third order Butterworth current-

mode filter is presented. Our approach of utilizing the parasitic capacitances of MOS transistors regards gate-to-source capacitances (C_{gs}) as useful, whereas other parasitic capacitances such as drain-to-gate capacitances (C_{gd}) are considered as parasitic. Therefore, the proposed circuits make use of the gate-to-source capacitances and the effect of the other parasitic capacitances is desired to be minimized. The fact that the gate-to-source capacitance of a MOS transistor is usually higher than the other parasitic capacitances is the reason behind this methodology.

We have analyzed the effect of additional transistors to overall transfer function for picking up the output current. Therefore, we have also proposed an enhanced version of MOS-only third order Butterworth filter with an available output current for usage in succeeding stages. A straightforward technique has been utilized to pick up the currents flowing over the MOS transistors by adding additional MOS transistors for this purpose. Their effects on the Butterworth transfer function are also analyzed and an improved version of MOS-only circuit including the effects of these additional transistors is investigated. Moreover, suppressing the effects of non-idealities caused by biasing or other parasitic capacitances, a tuning methodology based on external tuning and Dynamic Threshold MOS (DTMOS) transistor technique is developed. In this tuning technique, bulk terminals of MOS transistors are used to adjust the biasing point of the circuit by changing the threshold voltages of the MOS transistors. This gives the designers more flexibility than conventional tuning methods and allows low voltage operation when several transistors are stacked over each other.

2. The Proposed MOS-Only Circuit

The proposed MOS-only filter circuit is shown in Fig. 1. M2 and M3 are NMOS transistors and M1 is chosen as PMOS. Input current signal is applied to the source terminal of M1 transistor while the output signal is flowing over the drain of M2.

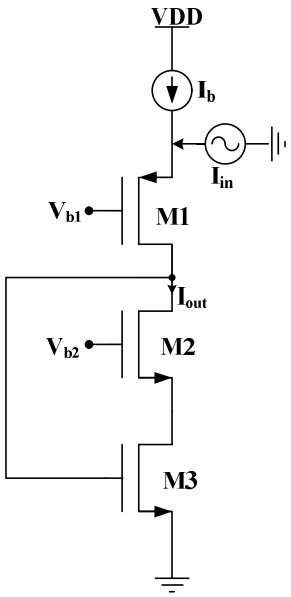

Fig. 1. The proposed MOS-only circuit

AC model of the proposed MOS-only circuit is depicted in Fig.2 where only gate to source capacitances and transconductances of MOS transistors are added to the model for simplicity. When the gate-to-source parasitic capacitances are taken into consideration, but the gate-to-drain capacitances not, then the transfer function of this circuit is given as

$$\frac{i_{out}}{i_{in}} = \frac{g_{m1}g_{m2}g_{m3}}{(g_{m1}+sC_{gs1})(s^2C_{gs3}C_{gs2}+sC_{gs3}g_{m2}+g_{m2}g_{m3})} \quad (1)$$

which can be rewritten as

$$\frac{i_{out}}{i_{in}} = \frac{1}{s^3\frac{C_{gs1}C_{gs2}C_{gs3}}{g_{m1}g_{m2}g_{m3}}+s^2\left(\frac{C_{gs1}C_{gs3}}{g_{m1}g_{m3}}+\frac{C_{gs2}C_{gs3}}{g_{m2}g_{m3}}\right)+s\left(\frac{C_{gs1}}{g_{m1}}+\frac{C_{gs3}}{g_{m3}}\right)+1} \quad (2)$$

The equation in (2) becomes a third order low-pass Butterworth filter transfer function when following equalities are satisfied. Thus, under the conditions in (3), it is possible to get a third order Butterworth filter only using three MOS transistors when the biasing transistors are neglected.

$$\frac{g_{m1}}{C_{gs1}} = \frac{g_{m2}}{C_{gs2}} = \frac{g_{m3}}{C_{gs3}} \quad (3)$$

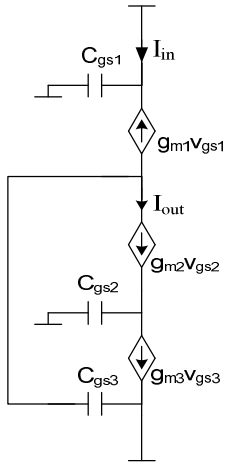

Fig. 2. The AC model of the proposed MOS-only circuit

In this technique, gate to drain capacitances of MOS transistors become undesired parasitic capacitances which deteriorate the ideal transfer function in (2). When their affects are added to the transfer function, it becomes

$$\frac{i_{out}}{i_{in}} = \frac{g_{m1}g_{m2}(g_{m3}-sC_{gd3})}{(g_1+sC_{gs1}).\Delta} \quad (4)$$

where

$$\Delta = s^2(C_{gs2}C_{gs3}+C_{gs2}C_{gd1}+C_{gs2}C_{gd2}+C_{gs2}C_{gd3}+C_{gs3}C_{gd3}+C_{gd3}C_{gd1}+C_{gd3}C_{gd2})+ s(g_{m3}C_{gd3}+g_{m2}C_{gs3}+g_{m2}C_{gd1}+g_{m2}C_{gd2})+g_{m2}g_{m3} \quad (5)$$

When gate to drain capacitances are neglected, the equation reduces to its definition in (2) as expected. The numerator of the non-ideal transfer function in (4) shows that there is a right hand plane zero at

$$f_o = \frac{g_{m3}}{2\pi C_{gd3}} \tag{6}$$

This right hand plane zero adds more phase shift to the Bode plot of the circuit and might be a problem for the stability of the circuit unless it is moved to very high frequencies. This is the chosen method in our design to alleviate its effect by properly adjusting the biasing and transistor aspect ratios which affect the value of gate to drain capacitances. Additional elements might be added to the circuit to move the zero to the left half plane or even to cancel the poles. However, this is not a robust solution and does not guarantee the pole zero cancelation whenever any variation occurs in the circuit such as process variations, temperature, etc. Moreover, the realization of these elements leads to additional parasitics.

$$f_{3dB_{ideal}} = \frac{g_m}{2\pi C_{gs}} \tag{7}$$

The equality of ideal 3dB pole frequency in (7) shows that cut-off frequency is proportional to the transconductances and gate to source capacitances of transistors. High frequency operation is possible when C_{gs} capacitances and transconductances are adjusted accordingly since the topology requires very small number of transistors contrary to a realization based on active analog building blocks such as op-amps, OTAs, etc. It is useful to note that the transconductance of a MOS transistor, as given in (8), is proportional to its width length ratio which also affects gate to source capacitance (9), so the designer should be careful while adjusting their values to determine the circuits both biasing and operation frequency for proper operation. In (9) gate to source capacitance is given when the transistor is in saturation mode of operation where C_{ov} is the overlap capacitance and Cox is the oxide capacitance.

$$g_m = \sqrt{2kI_D \frac{W}{L}} \tag{8}$$

$$C_{gs} = WLC_{ov} + \frac{2}{3}WLC_{ox} \tag{9}$$

One thing should be resolved for the circuit in Fig.1 is that the output current is flowing over the transistor M2. This current should be picked by a mechanism which does not affect the overall Butterworth transfer function. This method additionally should consider proper biasing of overall circuit and it should not deteriorate the frequency behavior of the circuit when high frequency operation is required. Furthermore, parasitics from the additional circuitry should be kept to a minimum. Considering aforementioned specifications, the improved circuit is shown as in Fig.3.

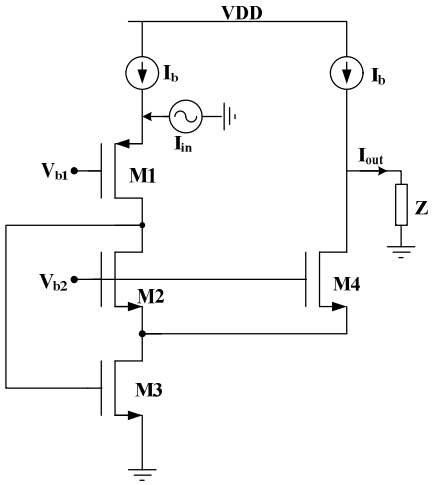

Fig. 3. The proposed overall MOS-only circuit

The transfer function of the improved MOS-only circuit can be given as in (10) when its AC model in Fig.4 is analyzed. The circuit in Fig. 3 satisfies third order Butterworth transfer function with new design equalities given in (14).

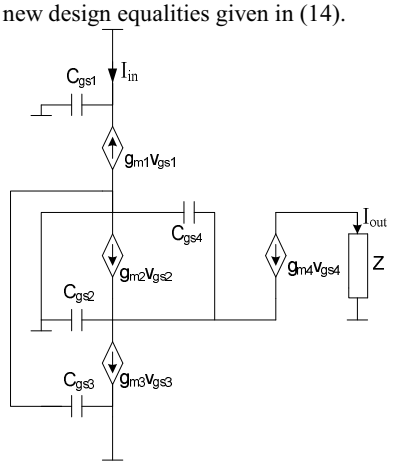

Fig. 4. The AC model of the improved MOS-only circuit

$$\frac{i_{out}}{i_{in}} = -\frac{g_{m1}g_{m3}g_{m4}}{(g_{m1}+sC_{gs1})[s^2C_{gs3}C_T + sC_{gs3}g_{m4}(a+1) + ag_{m4}g_{m3}]} \tag{10}$$

In equation (10), C_T shows the total equivalent gate to source capacitance between the gate and source of M2 and M4 transistors which is equal to $C_{gs2}//C_{gs4}$. The coefficient a, is defined by the ratio of the transconductances of M2 transistor to M4 transistor. Under the same biasing conditions and same transistor same dimensions these two capacitances become approximately same. Additionally, when M2 and M4 transconductances are chosen equal, these two variables, C_T and *a* become

$$C_T = 2C_{gs2} \quad , \quad g_{m2} = g_{m4} \Rightarrow a = 1 \tag{11}$$

After substituting these values into (10), transfer function becomes

$$\frac{i_{out}}{i_{in}} = -\frac{g_{m1}g_{m2}g_{m3}}{(g_{m1}+sC_{gs1})[s^2 2C_{gs2}C_{gs3}+s2C_{gs3}g_{m2}+g_{m2}g_{m3}]} \quad (12)$$

which can be rewritten as

$$\frac{i_{out}}{i_{in}} = -\frac{1}{s^3\frac{2C_{gs1}C_{gs2}C_{gs3}}{g_{m1}g_{m2}g_{m3}}+s^2\left(\frac{2C_{gs1}C_{gs3}}{g_{m1}g_{m3}}+\frac{2C_{gs2}C_{gs3}}{g_{m2}g_{m3}}\right)+s\left(\frac{C_{gs1}}{g_{m1}}+\frac{2C_{gs3}}{g_{m3}}\right)+1} \quad (13)$$

To get a third order Butterworth response, new design equalities should be chosen as in (14)

$$\frac{g_{m1}}{C_{gs1}} = \frac{g_{m2}}{C_{gs2}} = \frac{2g_{m3}}{C_{gs3}}, \quad g_{m2} = g_{m4}, \quad C_{gs2} = C_{gs4} \quad (14)$$

when Cgd capacitances are taken into consideration, non-ideal transfer function becomes

$$\frac{i_{out}}{i_{in}} = \frac{-g_{m1}g_{m2}(g_{m3}-sC_{gd3})}{(g_1+sC_{gs1})(1+sC_{gd4}Z).\Phi} \quad (15)$$

where Z is the load impedance and Φ is given as

$$\Phi = [s^2(2C_{gs3}C_{gs2}+2C_{gd1}C_{gs2}+2C_{gd2}C_{gs2}+C_{gd3}(C_{gs3}+C_{gd1}+C_{gd2}+2C_{gs2}))+ s(2C_{gs3}g_{m2}+2C_{gd1}g_{m2}+2C_{gd2}g_{m2}+C_{gd3}(g_{m2}+g_{m3}))+g_{m2}g_{m3}] \quad (16)$$

3. The Complete MOS-Only Circuit with Off-Chip Tuning

As it is seen from the non-ideal transfer function in (15), there is an additional pole coming from the gate to drain capacitance of M4 transistor and the Z load impedance. Usually the gate to drain capacitances significantly is lower than gate to source capacitances. When their effects are neglected, that is Cgd<< Cgs, the transfer function in (15) reduces to the ideal function. However, another important point to be pointed out that the current sources in circuits are not ideal. Thus, their gate to source capacitances will also affect the circuit. Similarly, the effects coming from transistors forming biasing voltages should also be considered but adding all the secondary effects in hand calculations become tediously complicated. Therefore, following complete circuit in Fig.5 is formed for further investigations in simulations with real current sources and biasing voltages.

In Fig.5, M5 and M6 transistors are diode connected transistors to generate desired biasing voltage at the gate of M2 transistor. M7 and M8 are current sources supplying biasing current over the core MOS-only circuit part. Vtune1 and Vtune2 are off-chip tuning voltages. These are used to compensate the change of the circuit's center frequency due to non-idealities. However, in the topology, four MOS transistors are stacked over which limits the biasing options of designer because of the supply voltage limits of modern low power analog circuits. For proper tuning in the circuit, DTMOS technique [7, 8] based on additional off-chip tuning voltage is utilized.

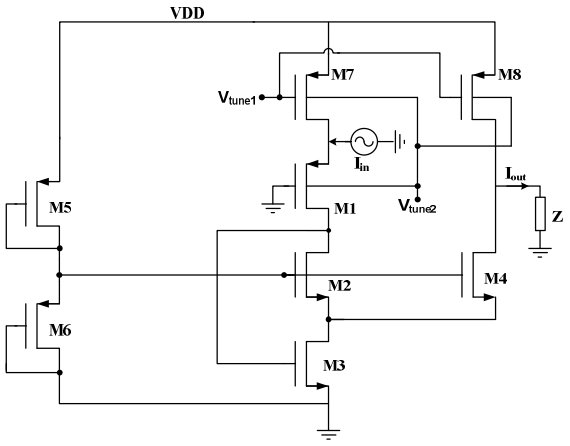

Fig. 5. The proposed, complete MOS-only circuit with DTMOS tuning technique

4. DTMOS Technique

DTMOS (Dynamic Threshold MOS) transistor was introduced by Assederaghi et al, in their paper [7] for digital circuits initially.

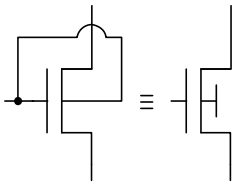

Fig. 6. DTMOS transistor and its commonly used circuit symbol

Connecting gate and body of an ordinary MOS transistor, as shown in Fig.6, is sufficient to generate a DTMOS transistor without requiring additional process steps in standard CMOS technology utilizing the definition of threshold voltage in (17), where ϕ_0 is the total surface band bending, γ body effect factor, V_{TO} is the zero bias threshold voltage. The equation is written for a long channel n-MOS transistor where drain-induced barrier lowering (DIBL) effect is neglected.

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right) \quad (17)$$

In addition to digital circuits, DTMOS transistors are also suitable for analog circuits where low-voltage and low power operation is needed. DTMOS transistors show lower effective threshold voltage under forward body bias. Moreover, under weak inversion regime DTMOS transistors also show better subthreshold slope and higher transconductance comparing to normal MOS transistors [7, 8]. One drawback of these transistors is that the forward body bias is limited to 0.4V~0.5V to prevent excess body currents due to source body, drain body parasitic diodes. To utilize this idea in higher supply voltages, either limiter transistors should be used or DTMOS technique should be employed to fix the maximum forward body bias. For instance, using a DC voltage source to forward bias the VSB voltage in (17) for a PMOS transistor effectively reduces the threshold voltage. When n-well process technology has been used, only PMOS transistor's body is available for connections. Additional terminal in the transistor gives the designers new

possibilities to find new solutions in analog circuit design. For instance, body effect of a MOS transistor can be minimized when a body is forward biased but maximum forward body bias voltage should be limited to prevent very high latch-up currents. This technique is used in the circuit in Fig. 5 to increase the tuning range of V_{tune1} to get closer to the ideal response.

5. Simulations

In simulations, TSMC 0.18µm n-well process technology parameters are used in SPICE program to model the transistors. The dimensions of the transistors in Fig.5 are tabulated in Table 1. These values are determined according to the design equalities in (14) and to satisfy high frequency operation of the proposed circuit. Vtune1 voltage is set to 0.6V while the maximum forward body bias of PMOS transistors M1, M7, M8 is 0.4V to employ DTMOS technique in off-chip tuning methodology.

Table 1. Transistor dimensions

Transistors	Width (µm)	Length (µm)
M1	30	1.5
M2, M4	168	2
M3	238	1.4
M5	4	4
M6, M7, M8	20	2

The power consumption of the circuit is 0.69mW when I_b biasing currents are set to 186.5µA after DTMOS tuning. The ideal cut-off frequency of the filter is found as 228MHz. The ideal and simulated responses of proposed third order Butterworth MOS-only filter are given in Fig. 7 when the output is loaded practically with a 10pF capacitor.

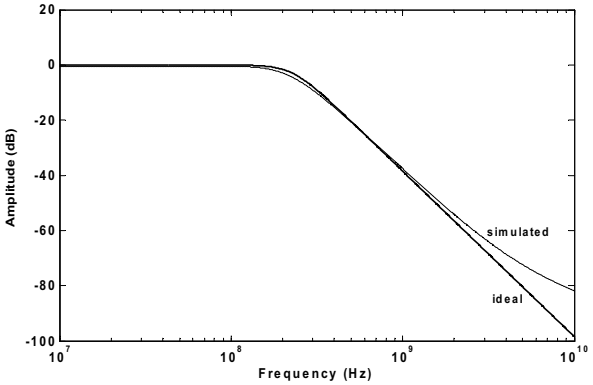

Fig. 7. Ideal and simulated filter magnitude response

Fig. 8 shows the sinusoidal characteristics of the ideal and the simulated responses at 100MHz. Ideal and simulated responses are opposite in phase but direction of the output current is taken inside in order to compare the ideal and simulated characteristics more closely. There is small magnitude loss at the simulated characteristic which is a result of the biasing conditions. These conditions are closely related with the filter results especially when high frequency operation is an aimed specification.

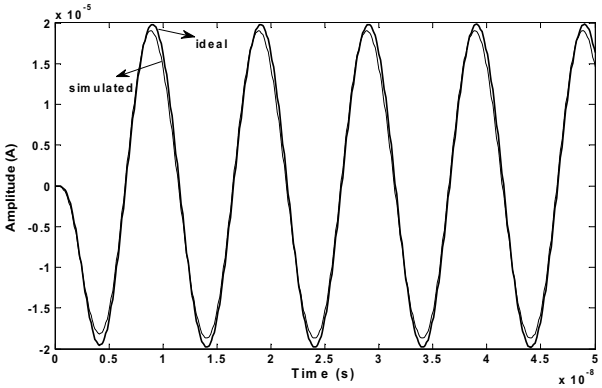

Fig. 8. Ideal and simulated filter sinusoidal response at 100MHz

6. Conclusion

A third order low-pass Butterworth filter for high frequency applications are proposed different from second order MOS-Only circuits in the literature. MOS-only technique has enabled to get a filter circuit with small number of transistors, low power consumption and requiring no additional passive elements. Furthermore, to alleviate the non-idealities caused by parasitics, A DTMOS technique-based tuning methodology is developed. Results show that the proposed circuit is capable of operation at high frequencies with consuming low power. The performance of the filter is confirmed with the program SPICE and theoretical calculations are found in good agreement with simulation results.

7. References

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