Real Time Implementation of Hybrid Sine Wave Reference Generator Based on PLL and DLT

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Abstract

A sine signal synchronous to the power system voltage signal is required in most power electronics based industrial applications. In this study, a phase locked loop (PLL) and direct look-up table (DLT) based hybrid sine oscillator is developed, and sinusoidal signals of the desired frequency that is synchronous to the reference input signal is generated in real time applicaitons carried out with the developed oscillator.

1. Introduction

Sinusoidal oscillators have many important practical applications in several fields of electrical engineering such as communications, instrumentation, music synthesis, and control [1]. Different techniques to generate the sine reference are proposed in the literature. Detailed analysis of these techniques and their relative merits are outside the scope of this paper but the interested reader could find them in [2,3]. Table I of [2] identifies a trade-off between three main criteria, which are fundamental to the reference waveform synthesis problem [3]. They are;

1) waveform quality;
2) run-time efficiency;
3) allocated memory.

Comparing these methods given in [2,3], the DLT method has been shown to provide a good compromise between efficiency and accuracy. Therefore this method is yet by far the most commonly used method for reference waveform generation in inverters, particularly those employing low-cost microcontrollers [3].

In this study, the DLT method was choosen because of its advantages as mentioned above for generating sinusoidal signal. In order for the generated sinusoidal signal to be synchronize to the choosen reference input signal, a PLL circuit was.

2. Direct look-up table method

The DLT method is a simple algorithm, based on reading the memorized samples of the sinusoid from a table. The memorized samples represent values of the sinusoidal function for M angles uniformly spaced around the unit circle, in the range 0 – 360° (0- 2π). They are stored in the table as the information of angle ($k*2\pi/M$) and its sinus value[4] :

$$S(k)=\sin(k*2\pi/M), \quad k = 0,1, ..., M-1 \qquad (1)$$

where k = table index and M = length of table.

The sine-wave signal is generated by accessing the table at a constant rate f_s Hz, in effect, moving counterclockwise around the unit circle and wrapping around the end of the table whenever 2π is exceeded [4].

In classical DLT method each time the table is accessed the index value (k) in Eq.(1) is regularly increased so that it takes values in the internal $[0...M-1]$. However, in this study, k is obtained by reading the instantaneous count value of the counter that is used as frequency divider in PLL circuit.

The generated sampled waveform is only an approximation to the sampled sinusoid. Because of the approximations made in the sine-wave signal generation, some distortion appears. As the table is much longer (N larger), the resolution is much better and consequently, the approximation will be closer [4].

3. Description of Designed Sinus Oscillator

How a sinusoidal signal can be generated by means of classical DLT method was summarized above. In various power electronics based industrial applications, on the other hand, the used sinusoidal waveform signal must be synchronize to the power system voltage signal (or to choosen any reference signal). The functional block diagram of the developed PLL and DLT based hybrid system for the purpose of generating a sinusoidal signal synchronized to the power system voltage signal is shown in Fig. 1. It is possible to divide the developed system into three main parts.

1) Signal conditioning circuit.
2) PLL circuitry.
3) Implementation of the DLT algorithm.

As shown in Fig. 1, by using resistors (R5,R6) of suitable values and INA126 IC a signal conditioning circuit (SCC) was designed so that the power system voltage signal to be used as a reference input signal can be applied to the PLL.

As mentioned before, it is required that the generated sine wave be synchronos to the reference input signal. For this purpose, PLL is used due to its advantages such as ability to work with the distorted signals, ability to track the frequency deviation of the input signal to which it is locked in the specified interval.

The PLL is essentially a digital feedback system where the input frequency f_i and feedback frequency f_{yN} are compared in the phase frequency detector and an analog error signal proportional to the phase difference is generated at the input of the loop filter.

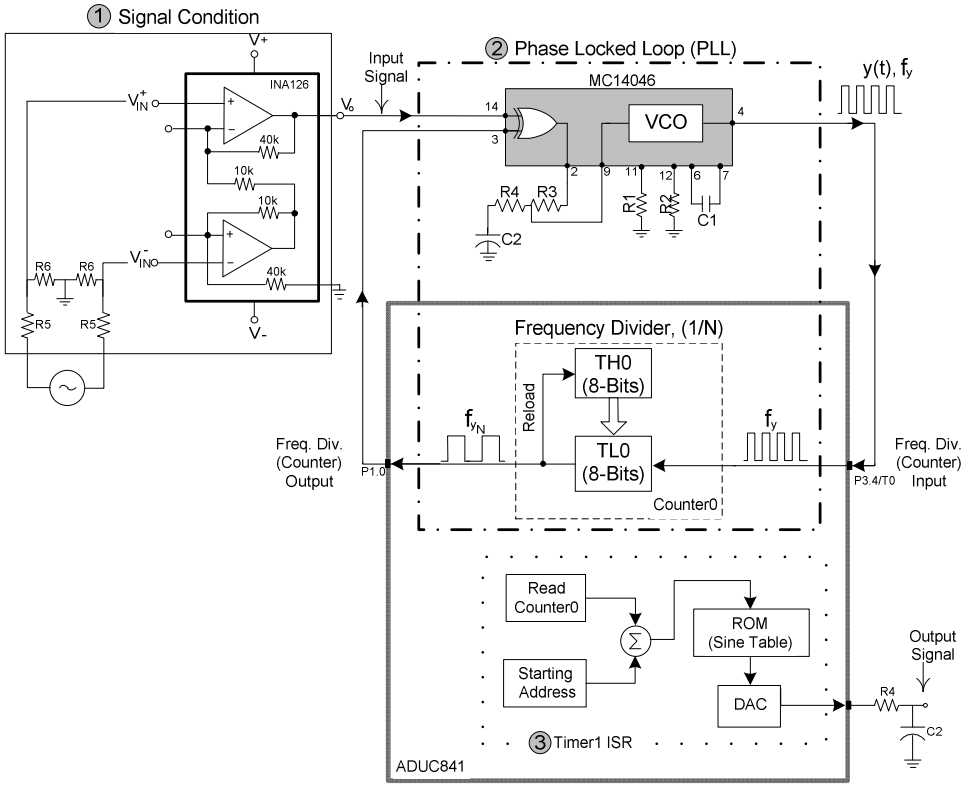


Fig. 1. Functional block diagram of developed hybrid signal oscillator

The error signal drives a voltage-controlled oscillator (VCO) to generate the desired output frequency. If the output wave tends to fall back in phase (or frequency), the error voltage builds up to correct the VCO output such that the input and feedback waves lock together with a small phase error [5]. Once locked, PLL remains in that state for the input frequency range,

$$f_i - \Delta f \le f_i \le f_i + \Delta f \qquad (2)$$

which is a unique feature of it. Thus, synchronization does not break within the above defined interval. Δf is set during the design of PLL.The details of operation and design of PLL circuitry can be found in literature [5].

When the PLL locked on the input signal as described above, the counter produces a series of output numbers ranging from 0 to *N-1*, in a sawtooth pattern as shown in Fig. 2

Once PLL locks to the input, DLT algrithm starts to run in order to produce sinusoidal signals synchronous the input signal, with period $T_s = 1/f_s$ of the internal counter of the peripheral microcontroller in these steps [6];

i) The counter value (*0...N-1*) is read and added to a starting address number and applied to ROM. The ROM contains sine wave data of one cycle *M* words in length.

ii) The pattern is applied to a 12-bit DAC which generates a sampled sine wave output.

iii) The DAC output is applied to a low-pass filter, which passes the desired frequency and rejects the spurious frequencies.To generate a sine wave at an arbitrary frequency, the filter is generally a low-pass filter with a pass band up to the desired frequency, and a reject band starting at some multiple of the desired frequency.

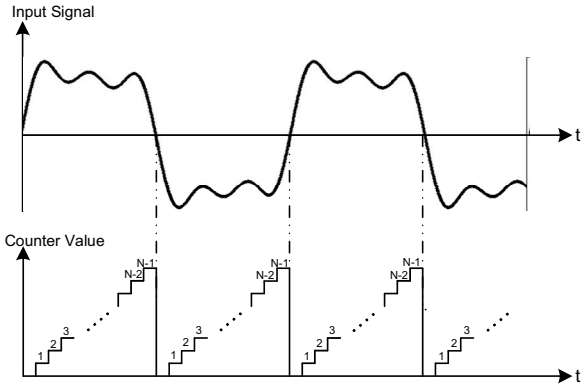


Fig. 2. Input signal and frquency divider value

Differently from the conventional DLT algorithmes, the sine signal frequency generated in this work is not dependent on the operating period T_s and it can be expressed as,

$$f_o = \frac{M}{2N} f_i \qquad (3)$$

where N is frequency division ratio of PLL, M is sine tablelength and f_i is the frequency of the input (reference) signal.

However, T_s of the DLT algorithm should be selected carefully since it defines the accuracy of the generated signal. The impact of various T_s values, $T_{s3}<T_{s2}<T_{s1}$, on the generated sine waveform is shown in Fig.3 and total harmonic distortion (THD) analysis of these sine waveforms is given in Table 1.

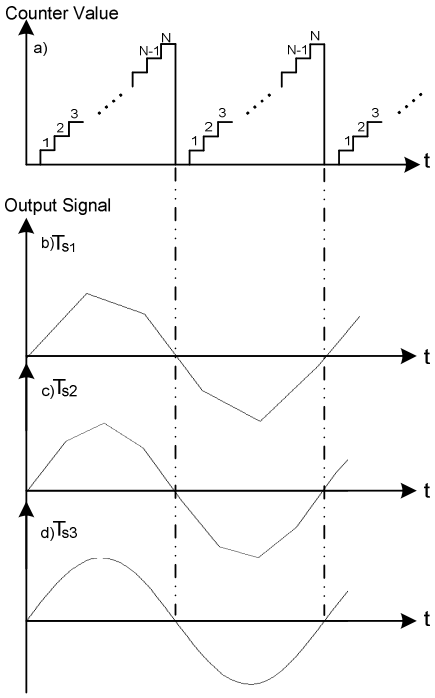


Fig. 3. Sample signal waveforms for different T_s values

Table 1. THD results for different operating period

T_s Value (T_s= 1/f_s)	% THD Value
T_s= T_{s1}=1/300	31.08
T_s= T_{s2}=1/1200	7.57
T_s= T_{s3}=1/9600	0.94

The range of T_s is defined by Nyquist criterion and length of table M as below:

$$\frac{1}{Nf_i} \le T_s < \frac{1}{2f_i} \qquad (4)$$

Fort the large values of T_s the generated sine wave becomes excessively distorted as shown in Fig. 3b and in Table 1. On the other hand T_s values less than $1/Nf_i$ increase microcontroller work with no improvement in the accuracy.

4. Experimental results

In this section it is demonstrated that the developed sine oscillator is capable of generating sinusoidal waveforms in desired frequency and accuracy in synchronous to any reference signal, however distorted it is. The reference (input) signal at f_i=50 Hz is generated by a microcontroller based programmable function generator (PFG) for the experimentation is shown in Fig. 2.

The experimental work done for generating the sinusoidal signal synchronized with the above reference signal and having angular accuracy of 1° is explained below.

1-) A sine table wais prepared with M=360 for the range of [0°-360°] with an angular accuracy of 1°.

2-) The generated signal was desired to be with the same frequency as the reference signal so, from Eq. (2) N=180 was calculated.

3-) For N =180, from MC14046 datasheet and experimentation R1, R2, R3, R4, C1 and C2 were found to be 27k, 270k, 560k, 1nF and 10uF respectively. Using these component values, Δf of (2) for $f_i = 50Hz$ was obtained to be $\Delta f \cong 5.4Hz$

4-) R5 and R6 of SCC were calculated to be 1.2M and 4.7K respectively fort he 220V grid voltage. However, in the experiment R5 and R6 were taken to be 10k since the reference input signal was generated with PFG.

5-) The codes, short and computatively effective, of which flow diagram is provided in Fig. 4 were written in Assembly language and run in ADUC841 microcontroller.

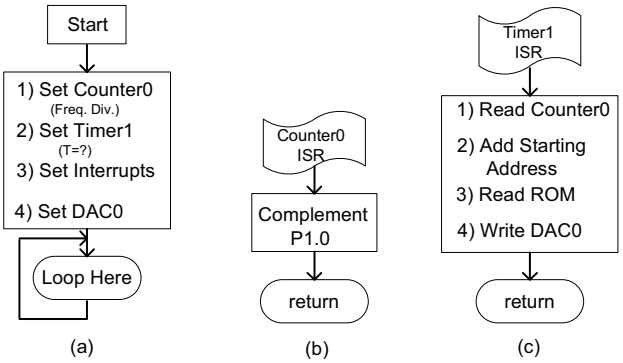
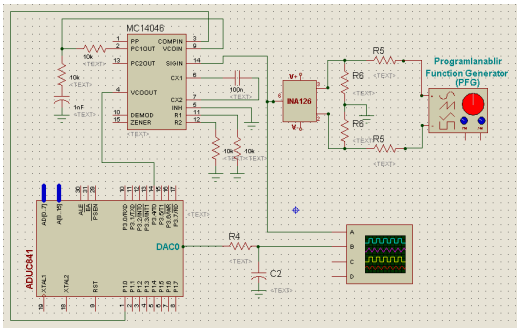


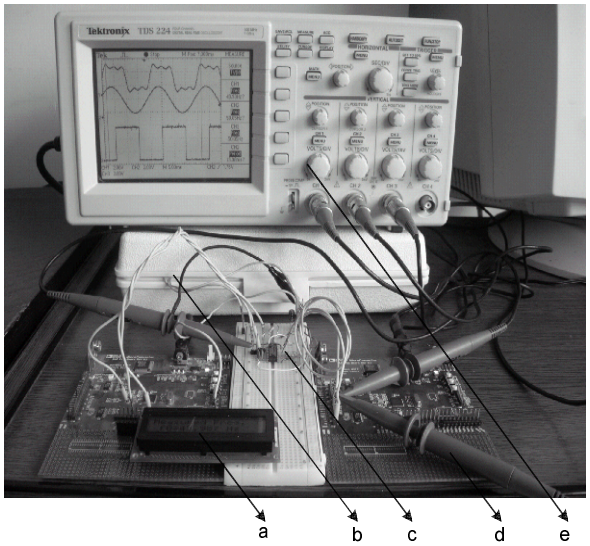
Fig. 4. Flow charts of created programs
a)Main program b)Counter0 ISR c)Timer 1 ISR

Shown in Fig.4a is the main program, in Fig.4b is the Interrupt Service Routine (ISR) for Counter0 and in Fig. 4c is ISR for Timer 1. The schematic of the finally developed signal oscillator is shown in Fig. 5.

The signal oscillator was tested by inputting a distorted voltage signal from the PFG. At the output a signal comprosed of only the fundemental component and synchronized with the input was obtained. A real time picture of the oscillator input and outputs signal is provided in Fig. 6. It should be noted that the frequency of the oscillator output signal is variable by Eq. 2.



(i)



a) Sine wave generator b) Power supply c) Analog PLL circuit d) designed μC based harmonic generator e) Oscilloscope.

(ii)

Fig. 5. (i)Schematic's of designed signal oscillator and (ii) real time experimental setup

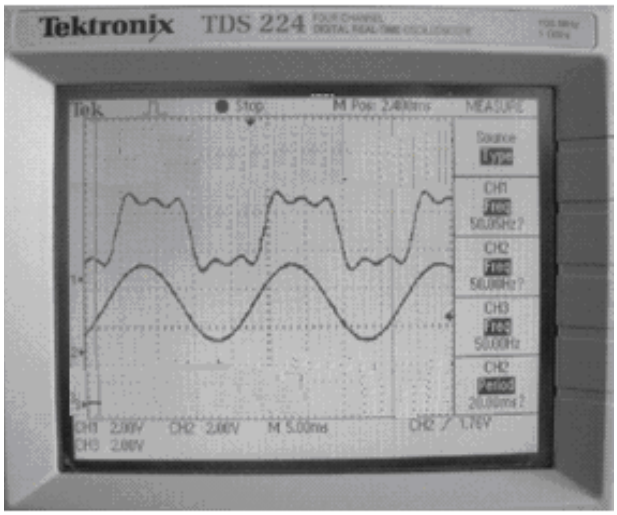


Fig. 6. Oscilloscop screen from real time experiment

5. Conclusions

In this work a hybrid oscillator which generate synchronos signals with the input and able to track input frequency variations in the range of $[f_i - \Delta f, f_i + \Delta f]$,where $f_i = 50Hz$ and $\Delta f = 5.4Hz$, is developed. The oscillator is cheap and reliable and has a compact structure due to the microcontroller architecture comprising many peripherals such as ADC/DAC, PWM, EEROM etc. Besides, the oscillator requires very little calculatory work so lend itself to performing other measurement and control tasks

6. References

[1] M.A. Al-Jarrah, M. Al-Ibrahim and A.I. Abu-El-Haija, "Recursive digital sine wave oscillators using the TMS32010 DSP", *IEEE IMTC' 94 Conf.*, pp. 792-796, 1994.

[2] M. Mirkazemi., T. C. Green and B. W.Williams, "Analysis and comparison of real-time sine-wave generation for PWM circuits", *IEEE Trans. Power Electron.*, vol.8,pp. 46–47, 1991.

[3] T. Abeyasekera, C.M. Johnson, D.J.Atkinson and M.Armstrong, "Elimination of Subharmonics in Direct Look-Up Table (DLT) Sine Wave Reference Generators for Low-Cost Microprocessor-Controlled Inverters", *IEEE Trans. Power Electron*., vol.18(6), pp.1315-1321, 2003.

[4] V.Matic, M.Nedelicki, V.Tadic, "Comparison of digital signal processing methods for sine wave signal generation", *IEEE ITS'98 Symp*, pp.290-295, 1998.

[5] R.E.Best, "Phase-Locked Loops Design Simulation and Applications", *McGraw-Hill*, 2003.

[6] S. Max, "Direct AWG sine wave synthesis with fixed clock frequency", *Measurement*, vol. 31, pp. 209-217, 2002.