A Novel High Integration-Density TFT-CMOS Inverter with Vertical Structure for Low Power Application

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Abstract

In this paper, a novel vertical-like TFT-CMOS inverter with simple process and high integration density is proposed, which is composed of a pseudo-planar CMOS. Two compared devices are also designed for comparison, namely, the vertical complementary metal-oxide-semiconductor (VCMOS) and planar complementary metal-oxide-semiconductor (PCMOS). According to simulation results, the source overlap region is used to obtain a high drain saturation current, the drain underlap region is used to obtain a low I_{off}, and the BOI is used to reduce the drain off-state current. we find out that the proposed approach achieves a 59.5% area reduction and significant shortening of wiring distance between the active devices when compared with existing planar CMOS technology.

1. Introduction

The conventional planar complementary metal–oxide–semiconductor (CMOS) scaling has reached its scaling limits; therefore, new device architectures are needed to continue/maintain the performance gain of the CMOS. A vertical MOSFETs exploit the vertical channel to achieve the higher performances compared with the conventional planar MOSFETs [1], [2]. Owing to its importance in the nano scale regime and challenges in developing technologies, there is a strong need for evaluating circuit performance with a realistic VCMOS architecture including the effects of layout, and device design. In this paper, the scaling performance (of area, speed, and power efficiency) and the behavioral analysis of a VCMOS platform are carried out using SILVACO TCAD simulation, including parasitic effects, and being benchmarked with planar [3] technologies for the same technology node. The results show that the new VCMOS offers significant performance gains and is a viable solution for future CMOS technologies.

In this paper, we demonstrate a new VCMOS inverter as shown in Fig. 1(a), and we compare its preliminary characteristics with those of the conventional PCMOS inverter by using SILVACO TCAD.

2. Device Structure and Fabrication

A new VCMOS inverter processes were simulated by using SILVACO TCAD. The starting substrates were wafers capped with a thick oxide layer for this work as shown in Fig. 2(a). First, the buried oxides (BOI) layer was patterned and etched (40 nm), as shown in Fig. 2(b). Second, a thick poly-Si layer was deposited and planarized by chemical mechanical polishing (CMP), and SiN (50 nm) deposition were formed as hard mask, which are shown in Fig. 2(c).

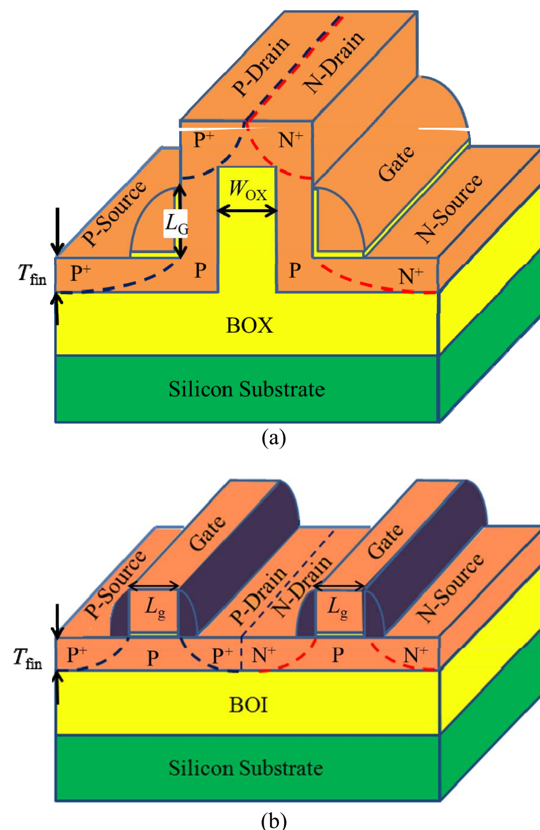


Fig. 1. The two schematic structures of (a) new VCMOS inverter and (b) PCMOS inverter.

In order to form the vertical channel scheme, the SiN and polysilicon were etched as shown in Fig. 2(d). Third, the silicon dioxide was deposited, and dry etched to form the oxide spacer for protecting the channel regions, After defining the S/D pads and channel regions, n-type S/D doping was then performed with arsenic at a tilt angle of 45°, whereas p-type S/D doping was performed with boron at a tilt angle of −45°, respectively, as shown in Fig. 2(e). And then, we used the SiN hard mask to define the vertical island by continuing anisotropic etching, then, the gate oxide was thermally grown for the vertical

sidewall structure. Next, an *in situ* 40 nm thick poly-Si film was doped and deposited simultaneously to form p$^+$ poly-Si gate and then patterned by plasma etching technology, as shown in Fig. 2(f). Finally, the contact formation is performed to form the connection layer.

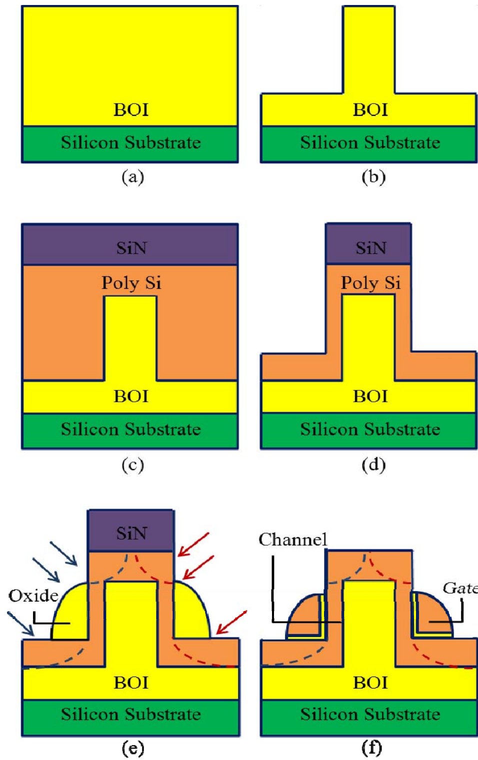


Fig. 2. The main fabrication process of a new VCMOS inverter. (a) wafers capped with a thick oxide layer, (b) etch oxide, (c) poly-Si deposition, CMP, and SiN deposition, (d) etch SiN and poly-Si, (e) S/D formation and (f) gate formation.

3. Results and Discussion

Fig. 3 shows the I_d-V_g characteristics of the two CMOS inverters. It shows the I_d-V_g curves of the two CMOS inverters. It can be observed that the I_{off} and Subthreshold Swing (S.S.) of the VCMOS inverter are improved due to the drain underlap regions, when compared with the PCMOS inverter.

Fig. 4 shows the transfer curves and the static current of the two CMOS inverters. We note that the VCMOS output voltage can reach the full swing. Also, it can be observed that the static power of the VCMOS inverter is lower than that of the PCMOS inverter.

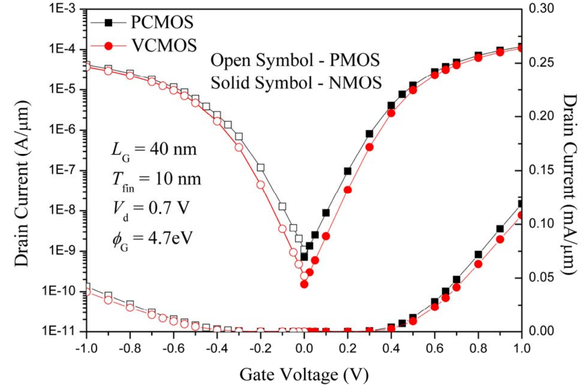
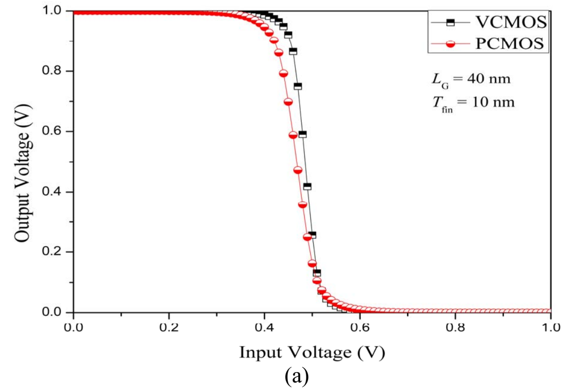


Fig. 3. Simulated I_d-V_g characteristics of VCMOS inverter and PCMOS inverter.



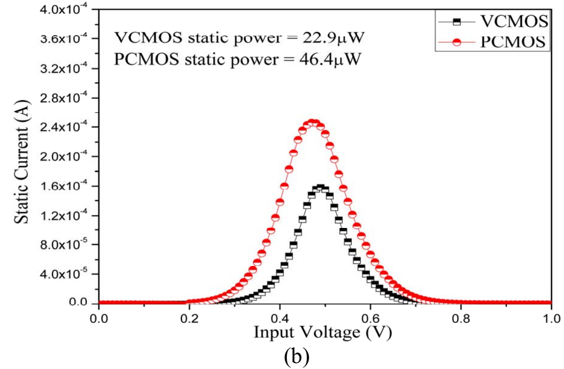
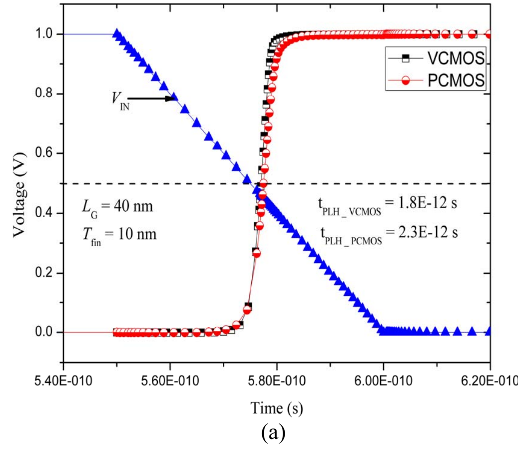
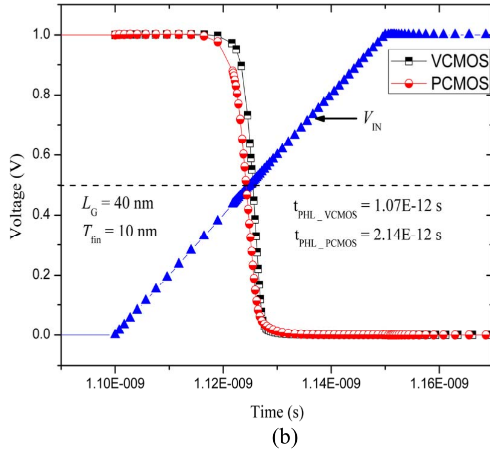


Fig. 4. (a) transfer curves and (b) static current transfer characteristics for the inverters of the new VCMOS inverter and conventional PCMOS inerter.

Fig. 5 compares the t_{pLH} and the t_{pHL} of the two CMOS technologies. The average delay time of the VCMOS exhibits 36% improved compared with a PCMOS. The extracted static power, t_{pLH} and t_{pHL} of them are also shown in Table 1.



(a)



(b)

Fig. 5. Comparison of (a) the t_{pLH} and (b) the t_{pHL} between the VCMOS and PCMOS inverters.

Table 1. Summary of the characteristics of the inverters.

	PCMOS	VCMOS
Static Power (μW)	46.4	22.9
t_{PHL} (ps)	2.14	1.07
t_{PLH} (ps)	1.8	1.3
t_P (ps)	1.97	1.185
FOM (aJ)	91.4	27

Note: The t_P is calculated as, $(t_{PHL} + t_{PLH})/2$, where t_{PLH} and t_{PHL} are propagation delay value of each kind of inverters which are shown in Fig. 5. Note: The Figure of Merit (FOM) is calculated from t_P and static power product.

Fig. 6 shows the voltage transfer characteristics (VTC) for an inverter featuring 40-nm-long transistors. Several V_{DD} values are considered ranging from 0.3 to 1 V. For each supply voltage condition, well-behaved VTC is obtained with a low-to-high output dynamic that reach rail-to-rail supply voltage range. Also, it does not degrade the high and low logic states due to the subthreshold leakage currents of both transistors are sufficiently low.

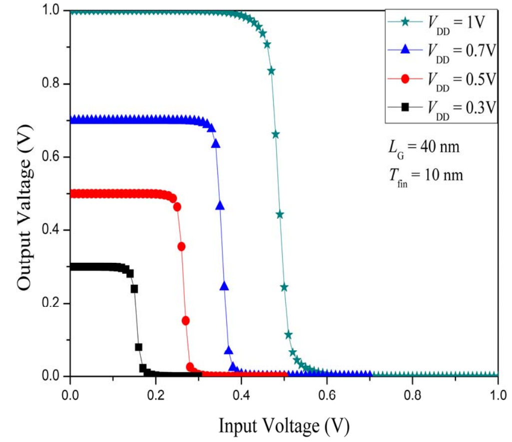


Fig. 6. VTC of a new VCMOS inverter at different V_{DD} ranging from 0.3 to 1 V.

Fig. 7 shows the excellent noise margins of a new VCMOS inverter which is extracted from the graphical illustration, e.g., NM_L = 0.42 V and NM_H = 0.41 V for 1 V of supply voltage. To refine the analysis, by using the maximum product criterion (MPC) [5] to evaluate the static noise margins. The maximum area of the rectangles can be embedded within the VTC loops of the cross-coupled inverters.

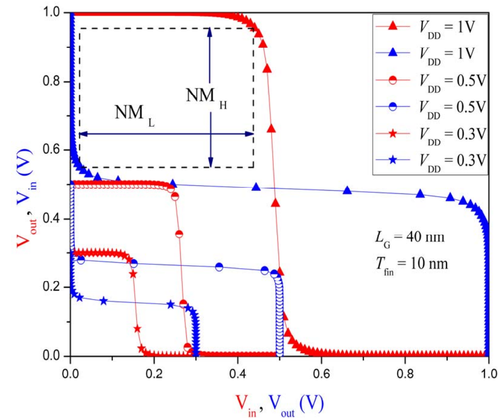
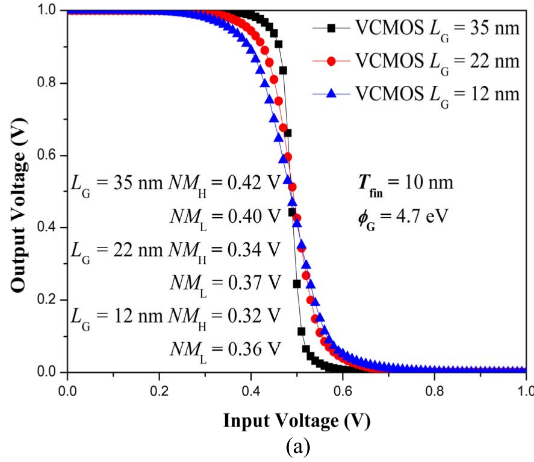
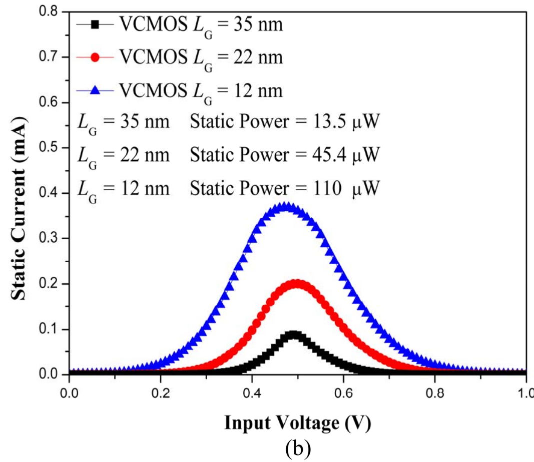


Fig. 7. Transfer static characteristics of the new VCMOS inverter at three different V_{DD} (0.3, 0.5, and 1 V) by plotting V_{in} and V_{out} interchangeably to evaluate the noise margins.

Fig. 8 shows the transfer curves and the static current of the VCMOS inverter with different L_G. We note that the L_G = 35 nm of the VCMOS output voltage can reach the full swing. Also, it can be observed that the static power of the L_G = 35 nm is lower than that of the L_G = 12 nm.



(a)



(b)

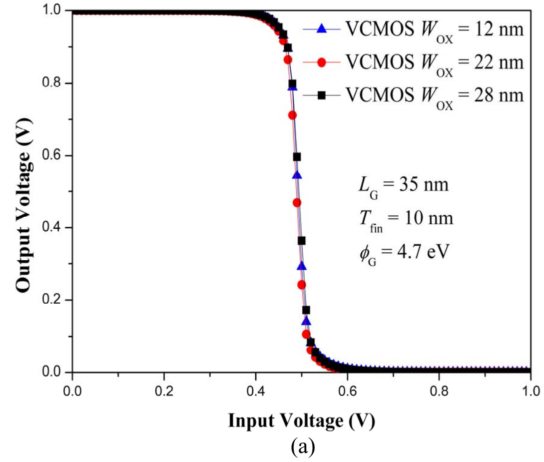
Fig. 8. (a) transfer curves and (b) static current transfer characteristics for the inverters of the new VCMOS inverter with different L_G.

Fig. 5 compares the t_{pLH} and the t_{pHL} of the two CMOS technologies. The average delay time of the VCMOS exhibits 36% improved compared with a PCMOS. The extracted static power, t_{pLH} and t_{pHL} of them are also shown in Table 2.

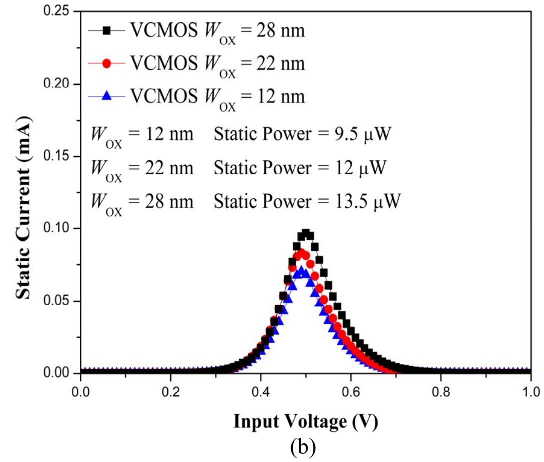
Table 2. Summary of the characteristics of the VCMOS inverter.

L_G (nm)	L_G = 12	L_G = 22	L_G = 35
Static Power (μW)	110	45.4	13.5
t_P (ps)	0.63	0.8	1.475
FOM (aJ)	69.3	36.32	19.9

Fig. 9 shows the transfer curves and the static current of the VCMOS inverter with different W_{OX}. We note that the different W_{OX} of the VCMOS output voltage can reach the full swing. Also, it can be observed that the static power of the W_{OX} = 12 nm is lower than that of the W_{OX} = 28 nm. due to the drain underlap regions small, when compared with the W_{OX} = 28 nm of VCMOS inverter.



(a)



(b)

Fig. 9. (a) transfer curves and (b) static current transfer characteristics for the inverters of the new VCMOS inverter with different W_{OX}.

Fig. 5 compares the t_{pLH} and the t_{pHL} of the two CMOS technologies. The average delay time of the VCMOS exhibits 36% improved compared with a PCMOS. The extracted static power, t_{pLH} and t_{pHL} of them are also shown in Table 3.

Table 3. Summary of the characteristics of the VCMOS inverter.

W_{OX} (nm)	W_{OX} = 12	W_{OX} = 22	W_{OX} = 28
Static Power (μW)	9.5	12	13.5
t_P (ps)	16	16.5	1.475
FOM (aJ)	1.5675	19.2	19.9

Fig. 8 shows the layout of the conventional CMOS inverter and the new VCMOS inverter which have a shared output contact and without gate width modulation. It can effectively reduce the area about 59.5%. Thus, a low cost, extra-high on-off speed, and high packing density VCMOS inverter technology can be easily achieved and applied for use in the future ULSI design.

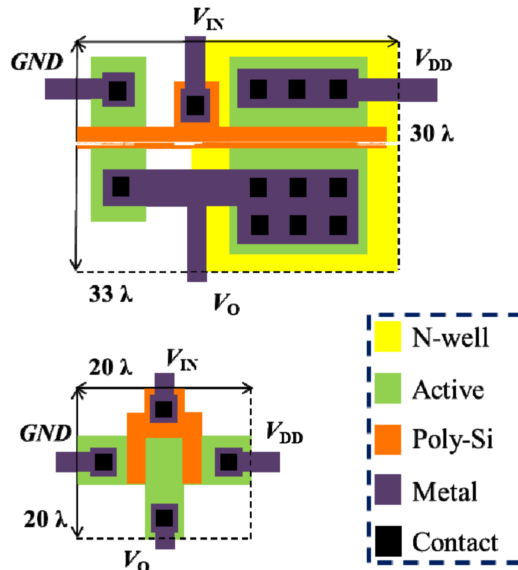


Fig. 8. Comparison of the area penalty of (a) a conventional CMOS inverter and (b) the new VCMOS inverter which have shared output node.

4. Conclusions

In this paper, we have presented a simulation study for ULSI applications of a new VCMOS inverter. According to the simulations, the VCMOS inverter shows better electrical performance than its conventional counterpart. Besides, the new VCMOS shows the excellent noise margins deduced from the graphical illustration. Thus, it is believed that the new VCMOS inverter can become a low power application for high integration density ULSI applications.

5. Acknowledgement

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6. References

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