ANALYSIS AND COMPARISON OF SPACE VECTOR MODULATION SCHEMES FOR INVERTER WITH SINUSOIDAL OUTPUT CURRENT BY USING DSP CONTROLLER

Saffet Altay Sinan Güngör
e-mail: altay@elk.itu.edu.tr *e-mail:* gungor@elk.itu.edu.tr
Istanbul Technical University, Faculty of Electrical & Electronic, Department of Electrical Engineering, 30626, Maslak, Istanbul, Turkey

Key words: Space vector modulation,optimal zero voltage vector selection

ABSTRACT

In this study, the implementation and performance enhancement of the space vector modulation (SVM) schemes has been investigated. SVM has been implemented for the voltage source inverter (VSI) and has been tested for an induction motor. Experimental results have been shown superior performance on the electromagnetic torque. A reverse sequencing scheme has also been proposed to optimize switching losses and total harmonic distortion (THD) of phase voltages and currents for high power applications.

I. INTRODUCTION

In recent decades there has been a rapidly growing demand for high quality power. In light of this fact, this paper presents the theory and implementation of two sequencing schemes of SVM by combining the advantages of digital signal processor (DSP) to ensure a good dynamic range for VSI fed induction motors. Dynamic range refers to the maximum possible control level in steady state or during transient. Improved dynamic range has been achieved the algorithm based on closed loop constant V/Hz principle built in DSP. Proposed two sequencing schemes have been implemented using the TMS320C240 DSP of Texas Instrument and generated the same desired sinusoidal output line-to-line voltages but differ in their performance with respect to phase voltages, total harmonic distortion (THD), peak-to-peak ripple in the phase current and switching losses [1,2,6,7,8].

SVM has led to the development of an inherently digital modulation method. Assuming a balanced three-phase three-wire system, SVM is based on representation of the three-phase voltages as voltage vectors. The SVM refers to a special way of determining the switching sequence of the upper switches of VSI shown in Fig.1. The upper and the lower switches of the same leg are driven with two complementary pulsed signals $(Sa, S\bar{a})$. There are eight possible switching states for the output line-to-line voltages $[v_{ab}\ v_{bc}\ v_{ca}]$. Six out of these eight switching states $[(100),(110),(010),(011),(001),(101)]$ produce a non-zero voltage vectors $(V_1,V_2,V_3,V_4,V_5,V_6)$ and the remaining two switching states $[(111),(000)]$ produce zero voltage vectors (V_{z0},V_{z7}). Each switching combination is given a name according to the phase leg connection, where '1' denotes that phase leg is connected to the positive rail of the DC link, and '0' denotes that phase leg is connected to the negative rail of the DC link. Each switching combination results in a set of three phase voltages at the output of the VSI. Those voltage vectors have been shown in Fig. 2.

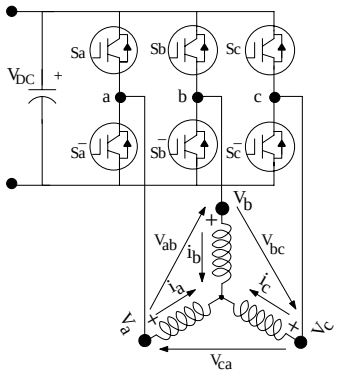


Fig. 1 Voltage Source Inverter.

II. SPACE VECTOR MODULATION

Four steps have been implemented to do the SVM in this study; First, V/Hz profile has been constructed and the reference voltage signals for phase a, b and c have been mapped into the (dq) stationary plane according to V/Hz profile, and have been represented by a reference vector $\vec{v}_{ref}$. Second, voltage vectors have been selected, including non-zero voltage vectors and zero voltage vectors to synthesize the $\vec{v}_{ref}$ vector for one switching cycle (T). Third, the time duration ($T1,T_2$) for all selected non-zero voltage vectors have been calculated. Fourth, the

switching states have been sequenced and dispatched to the compare channels of the DSP. [1,3,5]

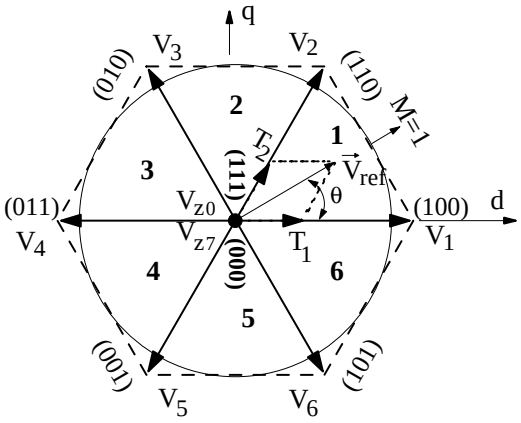


Fig. 2 Forming the hexagon.

The six non-zero voltage vectors form a hexagon. The hexagon can be seen by connecting the end point of all the non-zero voltage vectors. The hexagon defines the controllable region. The zero voltage vectors are at the origin and apply zero voltages to the induction motor (IM) phases that represent the freewheeling states. The hexagon can be further divided into six sectors denoted as 1 through 6. Each sector contains 60^0 region. Two schemes investigated in this paper have been evaluated under input and output voltage ratio which is also named modulation index (M). The inscribed circle of the hexagon, in Fig. 2, is the maximum balanced three-phase sinusoidal output. The radius of the inscribed circle equals 1, indicating that the maximum M is 1 which is 15% more than sinusoidal PWM technique. Peak value of the line-to-line voltage of the balanced three-phase sinusoidal phase voltages determines the modulation index (M) as in (1), and in turn controls the rms value of the output voltage. Changing the M can vary the rms value of the output voltage and significantly improves the total distortion factor (THD). It is always desirable to minimize the THD of the output voltage and current. It may change with the M in a nonlinear curve.

$$M = \frac{v_{1-lp}}{V_{DC}} \qquad (1)$$

III. REFERENCE VECTOR

Under steady state conditions, to get a balanced three-phase sinusoidal voltages, the $\vec{v}_{ref}$ vector must be rotate and the trajectory of the $\vec{v}_{ref}$ vector must draw a circle inside the hexagon. The radius of the circle is less than or equal to one. During transient, when the $\vec{v}_{ref}$ vector points outside the hexagon, the actual attainable $\vec{v}_{ref}$ vector falls on and slides along the boundry of the hexagon. The circle and the hexagon are tangential at exactly one position for each sector. At this point (M=1) the $\vec{v}_{ref}$ vector describes the maximum trajectory.

In the SVM, the modulation scheme is turned into synthezing the $\vec{v}_{ref}$ vector using the voltage vectors. It can be divided into following steps [2,5,6,7,8]:

A.Selection of Switching Vectors

In order to create the required rotating flux vector in the stator of the IM the inverter needs to be driven with the correct switching states (SaSbSc). Positive sequence voltage excitation of the IM. (SaSbSc) corresponds to the rotation of the $\vec{v}_{ref}$ vector the counter clock-wise (CCW) direction. Given a $\vec{v}_{ref}$ vector, it can be synthesized using V_1, V_2 and V_{z0} and/or V_{z7}. It has been proven that using the nearest adjacent non-zero voltage vectors, which defines each sector, and the zero voltage vectors, the circulating energy, current ripple and THD have been minimized.

B.Projection of the V_{REF}

Generating the $\vec{v}_{ref}$ vector requires precise positioning of the $\vec{v}_{ref}$ vector within (dq) plane. This implies accurately controlling the rotational speed and magnitude of this vector. A mean $\vec{v}_{ref}$ vector over a switching period can be defined. Assuming that T is sufficiently small $\vec{v}_{ref}$ vector can be considered approximately constant during this interval. Fig. 2 shows the synthesis of the V_{ref} in sector 1. Non-zero voltage vectors V_1, V_2 and zero voltage vectors V_{z0} and/or V_{z7} have been selected. Therefore, the $\vec{v}_{ref}$ vector has been projected onto the two non-zero voltage vectors. The projection can be expressed as in (2).

$$\vec{v}_{ref} = T_1 \cdot V_1 + T_2 \cdot V_2 \qquad (2)$$

T_1 and T_2 are time durations for the V_1 and V_2 correspodingly. They can be calculated as in (3).

$$\begin{bmatrix} T_1 \\ T_2 \end{bmatrix} = \frac{V_m}{V_{DC}} \cdot \begin{bmatrix} \sin\left(\pi/3 - \theta\right) \\ \sin\theta \end{bmatrix} \qquad (3)$$

where V_m is the length of the $\vec{v}_{ref}$ vector and θ is the angle between V_1 and $\vec{v}_{ref}$ vector. The rest of the time within this switching period will be occupied by the zero voltage vectors. Zero voltage vectors don't affect the $\vec{v}_{ref}$. They help to balance the turn-on and turn-off periods of the switches and their power dissipation. Either one of them or both of them can be used. The selection of the zero voltage vectors is related to the sequencing of the non-zero vectors. T_z is the sum of time durations of zero voltage vectors given as in (4).

$$T_z = 1 - T_1 - T_2 = 1 - \frac{V_m}{V_{DC}} \cdot \cos\left(\pi/6 - \theta\right) \qquad (4)$$

C.Sequencing of Switching Vectors

After selecting the switching states, voltage vectors and knowing their time durations the next step has been done to sequence them. Realization of the switching pattern using PWM outputs; by using the synthsezed form of $\vec{v}_{ref}$ vector appropriate compare values (CMPR1,CMPR2,CMPR3), in Fig. 3 a-b, have been calculated. Although the sequence of the voltage vectors does not change the mean $\vec{v}_{ref}$ vector within a switching period, it has great impact on the power losses and harmonic contents.

IV. EXPERIMENTAL RESULTS

Two sequencing schemes have been investigated. 1)Symmetric sequencing scheme (SSS) uses both of the zero voltage vectors, V_{z0} or V_{z7}. 2)Reverse sequencing scheme (RSS) uses only one of the zero voltage vectors. Those schemes have been shown in Fig. 3.

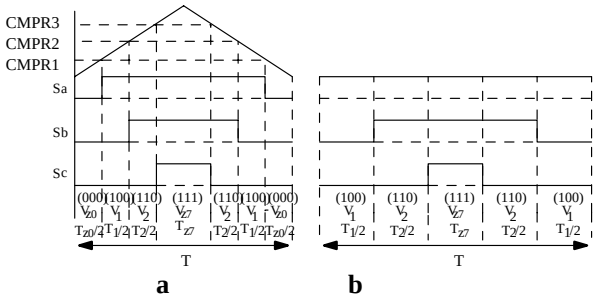


Fig. 3 a-SSS, b-RSS

1)Symmetric sequencing scheme (SSS)

The control signals for upper switches (SaSbSc) for a given $\vec{v}_{ref}$ vector located in sector 1 have been shown Fig. 3-a. There are a total of six switching actions within one T with three switch turn-ons and three switch turn-offs. Fig. 4 a-b shows the control signals of Sa and $S\bar{a}$ for 20 kHz and filtered of waveforms of these signals.

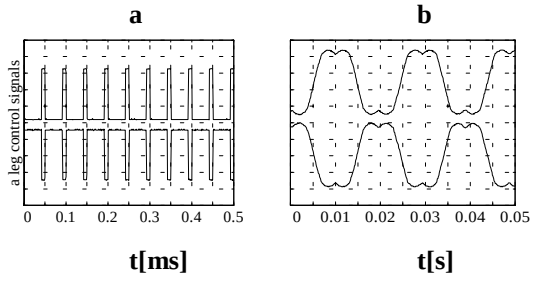


Fig. 4 a-PWM waveforms b-filtered of PWM waveforms.

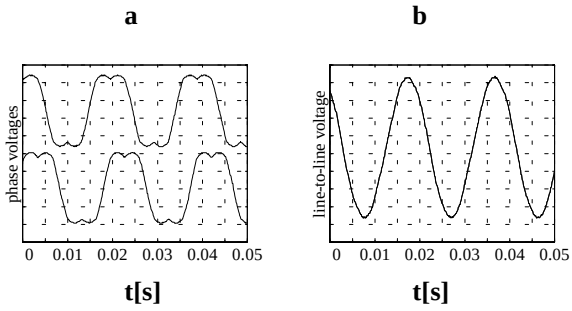


Fig. 5 a-phase voltages b-line-to-line voltages.

Fig. 5-b shows a sinusoidal line-to-line voltage waveform without low-order harmonics have been realized with SSS.

Fig. 6 a-b shows the phase current waveform and electromagnetic torque of IM for 3 Nm load torque. With SSS phase current has been done as sinusoid and the absence of peaks in the phase current the stress has been reduced on the power switches. SSS shows to be effective modulation strategy for increasing motor and inverter efficiency.

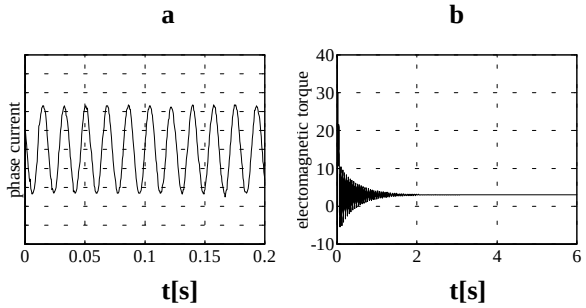


Fig. 6 a-phase current b-electromagnetic torque.

2)Reverse sequencing scheme (RSS)

This scheme is based on the fact that the switching losses are approximately proportional to the magnitude of the current being switched and hence it would be advantageous to avoid switching the inverter leg carrying the highest instantaneous current. Since the IM generally has a lagging power factor during motoring RSS scheme will have lower switching losses because the bus clamping occurs during the points of highest current This is possible in most cases, because all adjacent sectors differ in the state of switches in only one leg. Hence, by using only one of the zero switching states (000) or (111) within a given sector one of the legs does not have to be switched at all, as shown in Fig. 3-b. The performance of the RSS has been improved an optimal zero voltage vector selection routine which is described as follows.

The optimal zero voltage vector selection

The choice of the non-zero switching vectors is based on the $\vec{v}_{ref}$ vector and the phase and magnitude of the phase current are determined by the load. The SVM schemes vary depending on how and when the zero voltage vector is applied. As shown in Fig. 3-b, it is possible to leave one of the phase legs unswitched for the entire T. Since the switching loss is proportional to the amount of current being switched, the choice of the zero voltage vector should always attempt to leave the inverter phase leg carrying the largest current unswitched. In fact this is possible as long as the power factor is greater than or equal to 0.866, which means that the switching losses can be reduced by as much as 50%. For a balanced set of sinusoidal currents, every one-sixth of the fundamental period defines a new maximum magnitude of the three phase currents. If the phase a current is near maximum, the $\vec{v}_{ref}$ is in current sector 1 and phase leg a does not switch. The top switch carries the phase current continuosly because the voltage vector is V_{z7}. If the phase a current is near minimum, $\vec{v}_{ref}$ is in current sector 4 and phase leg a does not switch. The bottom switch carries the phase current continously because the state is V_{zo}. Optimal zero vector selection scheme has been used to down to zero rotor speed. The locked rotor condition is the worst possible case for the switch carrying a large phase current for a long time. The conduction time of the switch has been estimated about 166 ms. Inverter stage must allow for up to 166 ms of continous current conduction if optimal zero vector selection is used down to zero speed. Otherwise, a different zero vector selection routine should be used near zero speed so that the current is more evenly shared by the switch and diode. The one sixth of a period interval define six current sectors rotated away from the voltage reference axis by the power factor angle α. This rotation of the current reference axis is shown in Fig. 7 for forward motoring, which has an abc positive phase sequence. The current sectors identify the maximum phase current areas have been coded. When the $\vec{v}_{ref}$ vector in sector 1 for forward motoring operation the largest current is either i_a or i_c. As long as α does not exceed 30^0 When i_a is the largest current, the zero vector V_{z7} is chosen because the state of the switches for phase a are both '1' for V_1 and V_2. Therefore, the phase a current is not switched when i_a is the largest current. When i_c is the largest current in sector 1, the zero vector V_{z0} is chosen because the state of the switches for phase c are both '0' for V_1 and V_2. Therefore, the phase c current is not switched when i_c is the largest current. If the α is greater than 30^0, i_b can be the largest current in sector 1 and so the larger of either i_a or i_c is used to determine which zero vector is used.

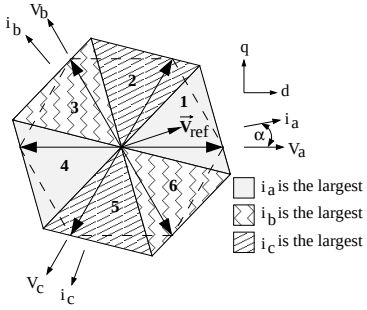


Fig. 7 current sectors for forward motoring.

The zero vector selection logic for sector 1 can be represented in Fig. 8. Similar selection logic is used for the additional sectors.

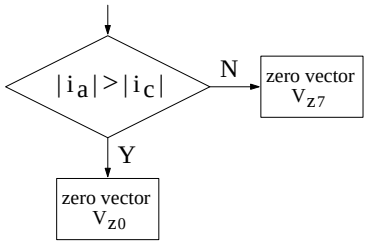


Fig. 8 zero voltage vector selection routine.

Fig. 9 a-b shows the phase voltages and phase current with RSS. The ripple in the phase current has increased. Phase voltages are differ from in Fig.5-a but line-to-line voltage is the sinusoidal as the in Fig. 5-b.

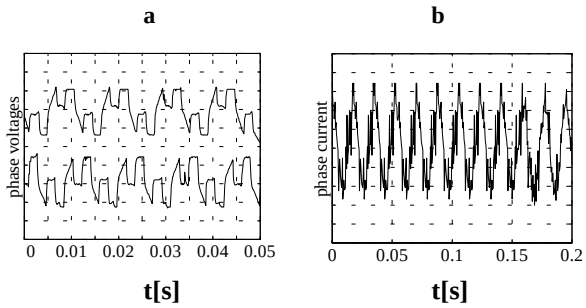
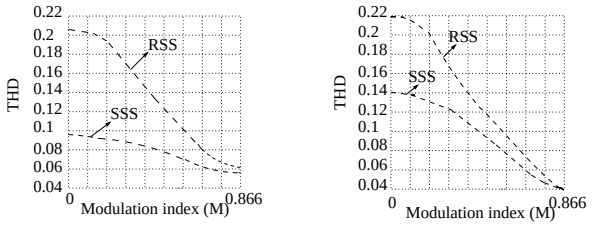


Fig. 9 a-phase voltages b-phase current.

Performance criteria

These modulation schemes have been simulated by using MATLAB and analyzed their relative performance with respect to switching loss, THD and the peak-to-peak current ripple at the output. The analysis has been performed over the entire range of modulation index and over varying load factor angles. THD of phase current and phase voltage for analyzed two sequencing schemes have been shown in Fig. 10. a-b.

THD decreases with increase in M beacuse of the increase in the fundamental component of the voltage/current and the other higher order harmonics being relatively constant.



a **b**

Fig. 10 a-THD of phase current b-THD of phase voltage.

It can bee seen that symmetric sequence has the least THD because of symetry in the switching waveform. By introducing symmetry, the number of voltage pulses in a given T is doubled as compared to the reverse sequencing scheme. This would make the converter look as if it were operating at twice the T. Hence this result in a reduced THD and reduced peak-to-peak ripple in the phase current. The switching losses have been assumed to be proportional to the product of the voltage across the switch and the current through the switch at the instant of switching. Since the voltage across the switch is the bus voltage, it is considered to be a constant. Thus the losses are proportional to the current during switching. The switching ripple has been neglected and the losses have been estimated based on the number of commutations required for each sequencing scheme and the current at the instant of switching. Losses for symmetric sequence are dependent on the load power factor and their loss performance has been optimized using the zero voltage vector selection routineg. Fig. 11 a-b shows the relative loss of performance characteristic of two schemes and relative peak-to-peak value of the current ripple, at maximum value of load current.

a **b**

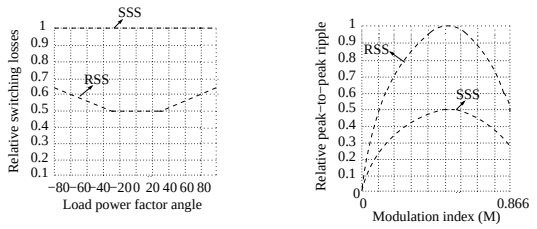


Fig. 11 a-relative switching losses b-relative peak-to-peak ripple.

V. CONCLUSION

Table summarizes the performance of two sequencing schemes. It can be clearly seen that a scheme with high THD has low losses and their characteristics are load dependent. This could be translated as a trade-off to be made between the size of the heat sink and the size of the filters. At low switching frequencies symmetric sequence could be used, since losses are not very critical. At high switching frequencies RSS is preferred, especially at high load power factors due to the 50% reduction in switching losses.

Modulation scheme	***SSS***	***RSS***
No of commutations in T	6	3
No of switching states in T	7	3
Dominant harmonic	f=1/T	f=1/T
Relative losses	1	0.5-0.63*
Relative peak-to-peak ripple	0.5	1
THD at high M	least	highest

*depending on the load power factor

Table. Relative performance of SSS and RSS.

The experimental data shows that using SVM can largely increase the efficiency of the IM. The SSS gives the lowest output distortion and harmonic spectrum. RSS reduce the switching actions by 1/3, and save switching losses by 50% for a load with a unity factor. The saving of the switching losses may vary with the load power factor. The distortion in the current and the harmonic contents are higher than the SSS. The optimization targets a minimum power losses, or combination of power losses, harmonic distortion and modulation index. The SSS is a good compromise between the reduction of power losses and reduction of distortion and harmonic contents.

It is possible to select best sequencing schemes in a real time operation of induction motor according to the M, load condition and to minimize switching losses. For example while regenerative operation RSS should be implemented by changing duty cycles.

SVM with an optimal zero voltage vector selection routine has decreased both the conduction loss of the inverter, due to a reduced THD, and the switching power losses of the inverter, due to decreased switching frequency. Improved inverter efficiency can result in reduced heat sink size and cooling requirements of the semiconductor devices. The reduced cooling requirements are important, for example, for an electric vehicle (EV) because smaller inverter heatsink cooling pumps and fans can be reduced, which is the key issue due to the limited space that is available.

REFERENCES

1. P. Vas, Vector control of AC Machines, Oxford University Press, 1990.
2. D. W. Novotny and T. A. Lipo, Vector Control and Dynamics of AC Drives, Oxford University Press, 1996.
3. Andrzej M. Trzynadlowski, The Field Orientation Principle in Control of Induction Motors, Kluwer Academic Publisher, 1994.
4. Andrzej M. Trzynadlowski, The Control of Induction Motors, Academic Press, 2001.
5. Bimal K. Bose, Power Electronics and Variable Frequency Drives, IEEE Press, 1997.
6. R. Valentine, Motor Control Electronics Handbook, McGraw-Hill Company, 1998.
7. http://www.ti.com
8. http://www.analog.com